PHILIPS

Integrated circuits

Book IC02a 1986

Video and associated systems

Bipolar, MOS

Types MAB8031AH to TDA1521

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VIDEO AND ASSOCIATED SYSTEMS
BIPOLAR, MOS
Types MAB8031AH to TDA1521

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

T1 **Tubes for r.f. heating**

T2a **Transmitting tubes for communications, glass types**

T2b **Transmitting tubes for communications, ceramic types**

T3 **Klystrons**

T4 **Magnetrons for microwave heating**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Müller tubes**

T8 **Colour display systems**
Colour TV picture tubes, colour data graphic display tube assemblies, deflection units

T9 **Photo and electron multipliers**

T10 **Plumbicon camera tubes and accessories**

T11 **Microwave semiconductors and components**

T12 **Vidicon and Newvicon camera tubes**

T13 **Image intensifiers and infrared detectors**

T15 **Dry reed switches**

T16 **Monochrome tubes and deflection units**
Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1 **Diodes**
Small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2a **Power diodes**

S2b **Thyristors and triacs**

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Surface mounted semiconductors**

S8a **Light-emitting diodes**

S8b **Devices for optoelectronics**
Optocouplers, photosensitive diodes and transistors, infrared light-emitting diodes and infrared sensitive devices, laser and fibre-optic components

S9 **Power MOS transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

S11 **Microwave transistors**

S12 **Surface acoustic wave devices**

S13 **Semiconductor sensors**

***S14** **Liquid Crystal Displays**

*To be issued shortly.

INTEGRATED CIRCUITS (PURPLE SERIES)

The NEW SERIES of handbooks is now completed. With effect from the publication date of this handbook the "N" in the handbook code number will be deleted.
Handbooks to be replaced during 1986 are shown below.

The purple series of handbooks comprises:

IC01	**Radio, audio and associated systems** Bipolar, MOS	new issue 1986 IC01N 1985
IC02a/b	**Video and associated systems** Bipolar, MOS	new issue 1986 IC02Na/b 1985
IC03	**Integrated circuits for telephony** Bipolar, MOS	new issue 1986 IC03N 1985
IC04	**HE4000B logic family** CMOS	new issue 1986 IC4 1983
IC05N	**HE4000B logic family — uncased ICs** CMOS	published 1984
IC06N	**High-speed CMOS; PC74HC/HCT/HCU** Logic family	published 1986
IC08	**ECL 10K and 100K logic families**	New issue 1986 IC08N 1984
IC09N	**TTL logic series**	published 1986
IC10	**Memories** MOS, TTL, ECL	new issue 1986 IC7 1982
IC11N	**Linear LSI**	published 1985
Supplement to IC11N	**Linear LSI**	published 1986
IC12	**I^2C-bus compatible ICs**	not yet issued
IC13	**Semi-custom** Programmable Logic Devices (PLD)	new issue 1986 IC13N 1985
IC14N	**Microprocessors, microcontrollers and peripherals** Bipolar, MOS	published 1985
IC15	**FAST TTL logic series**	new issue 1986 IC15N 1985
IC16	**CMOS integrated circuits for clocks and watches**	first issue 1986
IC17	**Integrated Services Digital Networks (ISDN)**	not yet issued
IC18	**Microprocessors and peripherals**	new issue 1986*

* The Microprocessors were included in handbook IC14N 1985, so IC18 will replace that part of IC14N.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

C2	Television tuners, coaxial aerial input assemblies, surface acoustic wave filters
C3	Loudspeakers
C4	Ferroxcube potcores, square cores and cross cores
C5	Ferroxcube for power, audio/video and accelerators
C6	Synchronous motors and gearboxes
C7	Variable capacitors
C8	Variable mains transformers
C9	Piezoelectric quartz devices
C11	Varistors, thermistors and sensors
C12	Potentiometers, encoders and switches
C13	Fixed resistors
C14	Electrolytic and solid capacitors
C15	Ceramic capacitors
C16	Permanent magnet materials
C17	Stepping motors and associated electronics
C18	Direct current motors
C19	Piezoelectric ceramics
C20	Wire-wound components for TVs and monitors
C22	Film capacitors

SELECTION GUIDE

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NUMERICAL INDEX

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MAF8031AHWP	128	–	ROM-less version of MAB8051AH; extended temperature	44-PLCC, SOT-187A	33
MAF80A31AHP	128	–	ROM-less version of MAB8051AH; automotive temperature; reduced frequency	DIL-40, SOT-129	33
MAF80A31AHWP	128	–	ROM-less version of MAB8051AH; automotive temperature; reduced frequency	44-PLCC, SOT-187A	33
MAF8035HLP	64	–	ROM-less version of MAB8048H; extended temperature	DIL-40, SOT-129	37
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MAF8039HLP	128	–	ROM-less version of MAB8049H; extended temperature	DIL-40, SOT-129	37
MAF80A39HLP	128	–	ROM-less version of MAB8049H; automotive temperature; reduced frequency	DIL-40, SOT-129	37
MAF8040HLP	256	–	ROM-less version of MAB8050H; extended temperature	DIL-40, SOT-129	37
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Operating temperature range: 0 to 70 °C.
Extended temperature range: −40 to + 85 °C.
Automotive temperature range: −40 to + 110 °C.

type number	RAM	ROM	description	package code	page
SINGLE-CHIP 8-BIT MICROCONTROLLERS (continued)					
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MAF80A51AHWP	128	4K	like MAB8051AH; automotive temperature; reduced frequency	44-PLCC, SOT-187A	33
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MAF84A11P	64	1K	plus 8-bit LED driver; automotive temperature; reduced frequency	DIL-28, SOT-117D	41
MAF8421P	64	2K	plus 8-bit LED driver and extended temperature	DIL-28, SOT-117D	41
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MAF84A61P	128	6K	plus 8-bit LED driver; automotive temperature; reduced frequency	DIL-28, SOT-117D	41
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PCB80C31WP	128	–	ROM-less version of PCB80C51	44-PLCC, SOT-187A	45
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Operating temperature range: 0 to 70 °C.
Extended temperature range: −40 to + 85 °C.
Automotive temperature range: −40 to + 110 °C.

type number	description	package code	page
PCB8582	256 x 8-bit EEPROM with I²C bus interface	DIL-8, SOT-97A	49
PCF2100P	LCD duplex driver; 40 segments	DIL-28, SOT-117D	57
PCF2100T	LCD duplex driver; 40 segments	SO-28, SOT-136A	57
PCF2110P	LCD duplex driver; 60 segments and 2 LEDs	DIL-40, SOT-129	67
PCF2110T	LCD duplex driver; 60 segments and 2 LEDs	VSO-40, SOT-158A	67
PCF2111P	LCD duplex driver; 64 segments	DIL-40, SOT-129	77
PCF2111T	LCD duplex driver; 64 segments	VSO-40, SOT-158A	77
PCF2112P	LCD driver; 32 segments	DIL-40, SOT-129	87
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PCF84C40D	128	4K		DIL-28, SOT-135A	95
PCF84C40P	128	4K		DIL-28, SOT-117D	95
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PCF8571P	128 x 8-bit static RAM with I²C interface			DIL-8, SOT-97A	111
PCF8571T	128 x 8-bit static RAM with I²C interface			SO-8L, SOT-176	111
PCF8573P	clock/calendar with serial I/O (I²C bus)			DIL-16, SOT-38	123
PCF8573T	clock/calendar with serial I/O (I²C bus)			SO-16L, SOT-162A	123
PCF8574P	remote 8-bit I/O with I²C bus interface			DIL-16, SOT-38	141
PCF8574T	remote 8-bit I/O with I²C bus interface			SO-16L, SOT-162A	141
PCF8576T	universal LCD driver for low MUX rates (1 : 1 to 1 : 4); I²C bus interface			VSO-56, SOT-190	155
PCF8576U	universal LCD driver for low MUX rates (1 : 1 to 1 : 4); I²C bus interface			uncased in tray	155
PCF8577P	LCD direct (32 segments) or duplex (64 segments) driver with I²C bus interface			DIL-40, SOT-129	191
PCF8577AP	LCD direct (32 segments) or duplex (64 segments) driver with I²C bus interface; different slave address			DIL-40, SOT-129	191

type number	description	package code	page
PCF8577T	LCD direct (32 segments) or duplex (64 segments) driver with I^2C bus interface	VSO-40, SOT-158A	191
PCF8577AT	LCD direct (32 segments) or duplex (64 segments) driver with I^2C bus interface; different slave address	VSO-40, SOT-158A	191
PNA7509	7-bit, 22 MHz, 3-state output, A/D converter	DIL-24, SOT-101	207
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SAA1060	LED display/interface circuit	DIL-24, SOT-101A	255
SAA1061	LED driver/output port expander	DIL-24, SOT-101A	261
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SAA1300	tuner switching unit	SIL-9, SOT-142B	289
SAA3004P	remote control transmitter for infrared operation	DIL-20, SOT-146C1	293
SAA3004T	remote control transmitter for infrared operation	SO-20, SOT-163A	293
SAA3006	low voltage infrared remote control transmitter (RC-5)	DIL-28, SOT-117	303
SAA3028	infrared remote control transcoder (RC-5); I^2C bus compatible	DIL-16, SOT-38Z	317
SAA5020	teletext timing chain circuit (625 lines)	DIL-24, SOT-101A	325
SAA5025D	teletext timing chain for USA 525 line system (USTIC); 40 characters per row, 24 rows (8 TV lines per row)	DIL-28, SOT-117D	335
SAA5030	teletext video processor	DIL-24, SOT-101A	353
SAA5040A	Teletext Acquisition and Control (TAC) circuit; giving status box	DIL-28, SOT-117	363
SAA5040B	TAC, without giving status box	DIL-28, SOT-117	363
SAA5040C	TAC, giving different status box	DIL-28, SOT-117	363
SAA5041	TAC, different remote control commands	DIL-28, SOT-117	363
SAA5042	TAC, different remote control commands	DIL-28, SOT-117	363
SAA5043	TAC, boxed channel information display	DIL-28, SOT-117	363
SAA5045	Gearing and Address Logic Array (GALA) for USA teletext; 525 line system	DIL-28, SOT-117D	383
SAA5050	teletext character generator (English)	DIL-28, SOT-117	391
SAA5051	teletext character generator (German)	DIL-28, SOT-117	391
SAA5052	teletext character generator (Swedish)	DIL-28, SOT-117	391
SAA5053	teletext character generator (Italian)	DIL-28, SOT-117	391
SAA5054	teletext character generator (Belgian)	DIL-28, SOT-117	391
SAA5055	teletext character generator (US ASCII)	DIL-28, SOT-117	391
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MAINTENANCE TYPE LIST

PNA7507; A	7-bit A/D converter	
SAA1056P	PLL frequency synthesizer	
SAA1082P	remote transmitter	
SAA3027	infrared remote control transmitter	
SAB3034	analogue and timing circuit (A & T)	
SAF3019	clock/timer with serial I/O; μC controlled	
TBA540	reference combination	
TBA750C; CQ	limiter/amplifier	
TDA2502	tacho motor speed controller	
TDA2503	track sensing amplifier for VCR	
TDA3571B	sync combination with transmitter identification	
TDA3576B	sync combination with transmitter identification	
TDA3590	SECAM processor circuit	(successor TDA3590A)
TDA3591	SECAM processor circuit	
TDA3591A	SECAM processor circuit	
TDA3650	vertical deflection circuit	
TDA3701	PAL sync processor for VCR	
TDA3710	chrominance signal/mixer for VCR	
TDA3720	SECAM processor for VCR	(successor TDA3725)
TDB2033	preamplifier for infrared remote control transmission	
TEA1002	PAL colour encoder and video summer	(successor TEA2000)

GENERAL

Type designation
Rating systems
Handling MOS devices

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic type number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits (see note 3).

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer / Central processing unit }
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.
3. The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added (e.g. SH for Bubble-memories).

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line
W : Lead chip-carrier (LCC)
X : Leadless chip-carrier (LLCC)
Y : Pin grid array (PGA)

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

DEVICE DATA

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB8051AH family of single-chip 8-bit microcontrollers is manufactured in an advanced 2 μ NMOS process. The family consists of the following members:

- MAB8031AH: ROM-less version of the MAB8051AH
- MAB8051AH: 4 K bytes mask-programmable ROM, 128 bytes RAM

Both types are available in 8, 10 and 12 MHz versions and 15 MHz for the MAB8031AH. In the following, the generic term "MAB8051AH" is used to refer to both family members.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 K bytes of program memory and/or up to 64 K bytes of data storage.

The MAB8051AH contains a non-volatile 4 K x 8 read-only program memory (not ROM-less version); a volatile 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/event counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O power for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and timing circuits. For systems that require extra capability, the MAB8051AH can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of 255 instructions; 44% one-byte, 41% two-byte and 15% three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs. Multiply, divide, subtract and compare are among the many instructions added to the standard MAB8048H instruction set.
For further detailed information see Users Manual 'Single-chip microcomputer'.

Features

- 4 K x 8 ROM (8051AH only), 128 x 8 RAM
- Four 8-bit ports, 31 I/O lines
- Two 16-bit timer/event counters
- Full duplex serial port
- External memory expandable to 128 K
- Boolean processing
- 218 bit-addressable locations
- On-chip oscillator
- Five-source interrupt structure with two priority levels
- 58% of instructions executed in 1 μs; multiply and divide in 4 μs (at 12 MHz clock)
- Enhanced architecture with:
  - non-page-oreinted instructions
  - direct addressing
  - four 8-bit register banks
  - stack depth up to 128-bytes
  - multiply, divide, subtract and compare
- Available with extended temperature range: −40 to + 85 °C (MAF8031/51AH)
- Available with automotive temperature range: −40 to + 100 °C (MAF80A31/51AH)

PACKAGE OUTLINES

MAB8031/51AHP; MAF8031/51AHP; MAF80A31/51AHP: 40-lead DIL; plastic (SOT-129).
MAB8031/51AHWP; MAF8031/51AHWP; MAF80A31/51AHWP: 44-lead, plastic leaded-chip-carrier (PLCC); SOT-187A.

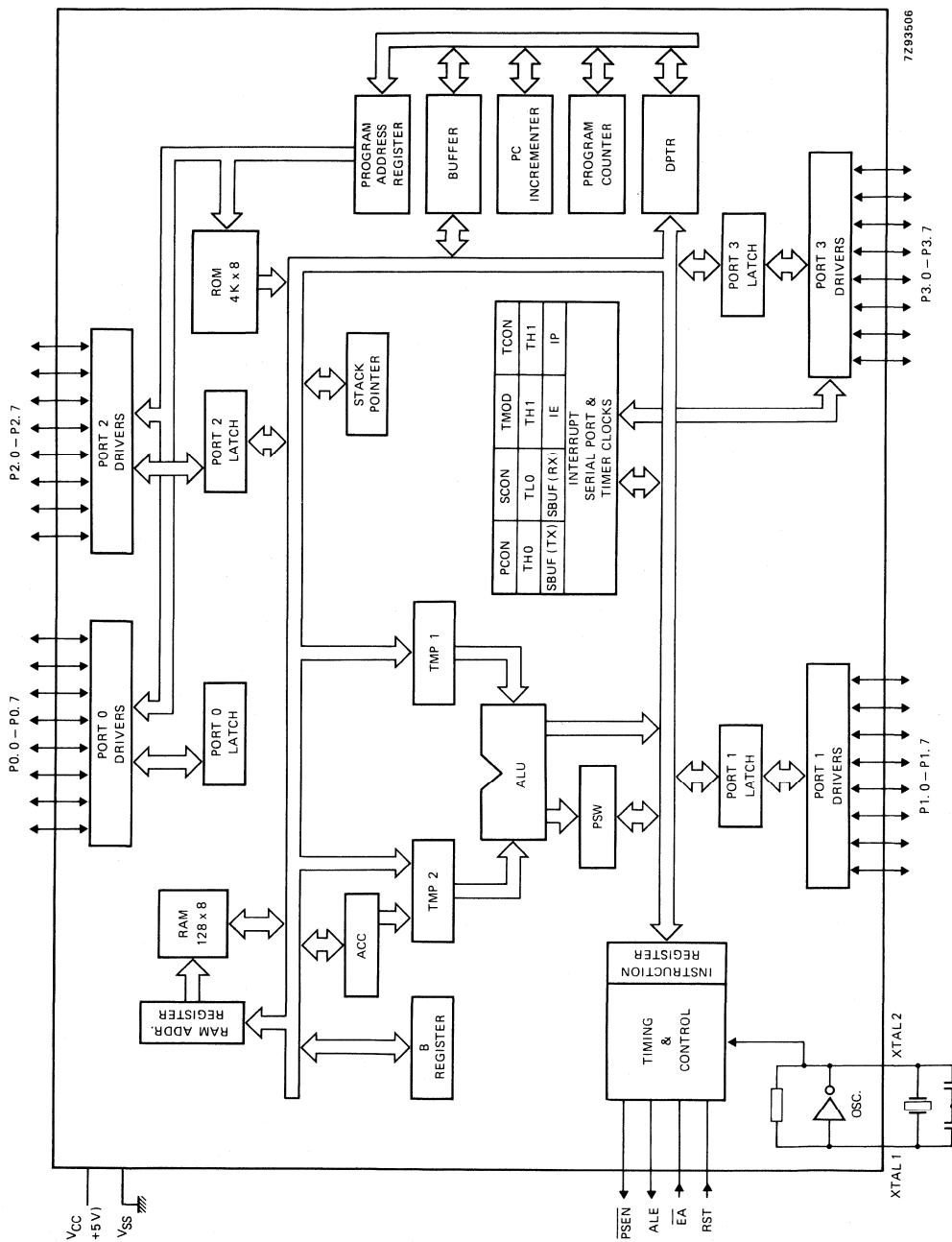


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB8052AH is a member of the MAB8051AH family with a higher performance. This single-chip 8-bit microcontroller is manufactured in an advanced 2 μ NMOS process. For this version the following members exist:

- MAB8032AH: ROM-less version of the MAB8052AH
- MAB8052AH: 8 K bytes mask programmable ROM, 256 bytes RAM

Both types are available in 12 MHz versions. In the following, the generic term "MAB8052AH" is used to refer to both family members.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 K bytes of program memory and/or up to 64 K bytes of data storage.

The MAB8052AH contains a non-volatile 8 K x 8 read-only program memory (not ROM-less version); a volatile 256 x 8 read/write data memory; 32 I/O lines; three 16-bit timer/event counters; a six-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and timing circuits. For systems that require extra capability, the MAB8052AH can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of 255 instructions; 44% one-byte, 41% two-byte and 15% three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.
For further detailed information see users manual 'single-chip microcomputer', chapter 8051.

Features

- 8 K x 8 ROM (8052AH only), 256 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- Full-duplex serial port
- External memory expandable to 128 K
- Boolean processing
- 218 bit-addressable locations
- On-chip oscillator
- Six-source interrupt structure with two priority levels
- 58% of instructions executed in 1 μs; multiply and divide in 4 μs
- Enhanced architecture with:
  - non-page-oriented instructions
  - direct addressing
  - four 8-bit register banks
  - stack depth up to 128-bytes
  - multiply, divide, substract and compare
- Upward compatible with 8031AH/8051AH
- Extended temperature range (−40 to +100 °C) in preparation

PACKAGE OUTLINES

MAB8032/52AHP: 40-lead DIL, plastic (SOT-129).
MAB8032/52AHWP: 44-lead plastic leaded chip-carrier (PLCC); SOT-187A.

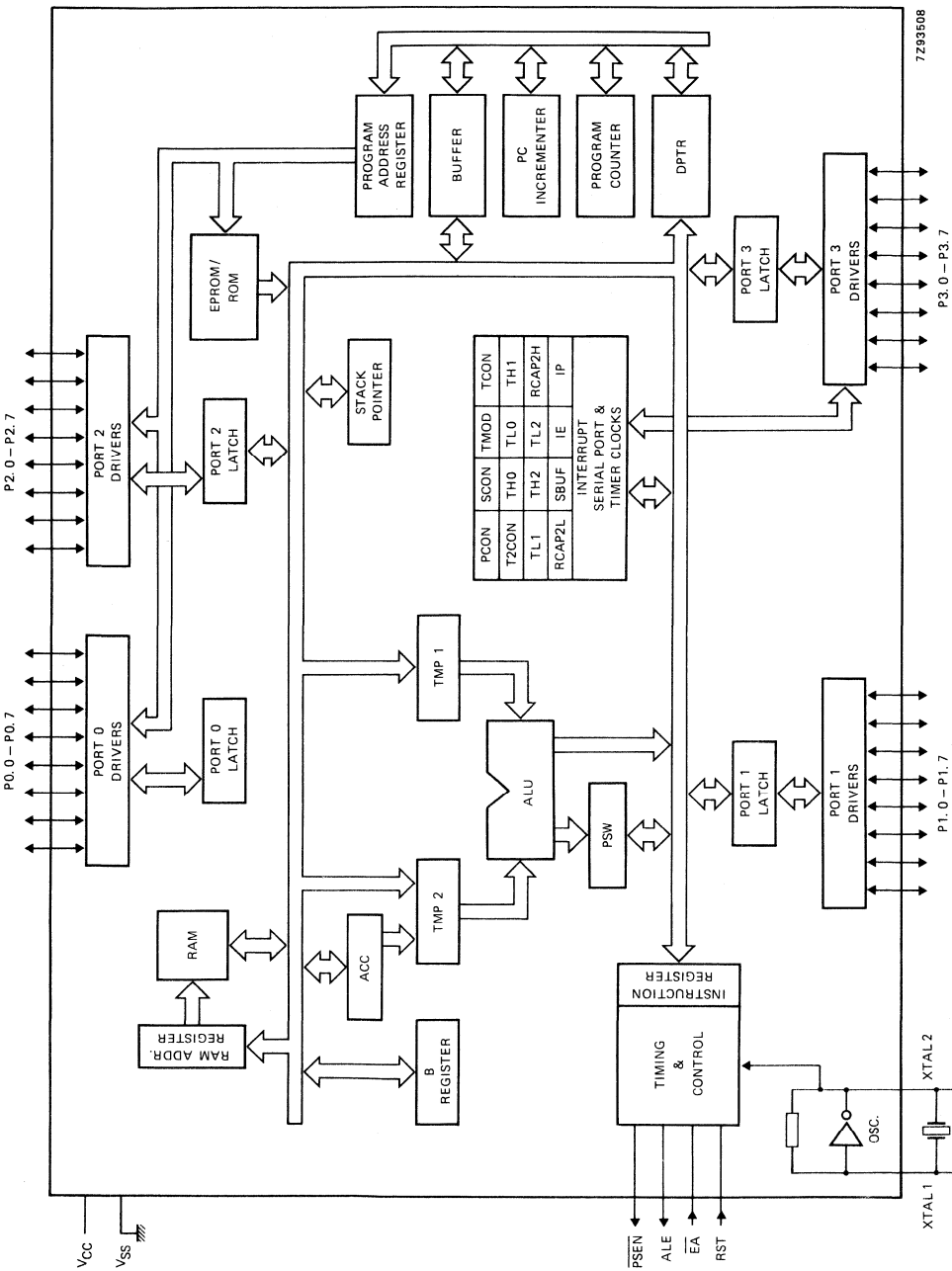


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The MAB80XXH family of single-chip 8-bit microcontrollers are fabricated in NMOS.
Three interchangeable (pin compatible) versions are available:

- MAB8048H with resident mask-programmed 1 K x 8 ROM, 64 x 8 RAM
- MAB8035HL without resident program memory for use with external EPROM/ROM
- MAB8049H with resident mask-programmed 2 K x 8 ROM, 128 x 8 RAM
- MAB8039HL without resident program memory for use with external EPROM/ROM
- MAB8050H with resident mask-programmed 4 K x 8 ROM, 256 x 8 RAM
- MAB8040HL without resident program memory for use with external EPROM/ROM

The MAB80XXH family are designed to be efficient control processors as well as arithmetic processors. Their instruction set allows the user to directly set and reset individual I/O lines as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions enable efficient implementation of standard logic functions. Code efficiency is high; over 70% of the instructions are single byte; all others are two byte.

An on-chip 8-bit counter is provided, which can count either machine cycles (÷ 32) or external events. The counter can be programmed to cause an interrupt to the processor.
Program and data memories plus input/output capabilities can be expanded using standard devices. For details see users manual 'single-chip microcomputer'.

Features

- 8-bit CPU, ROM, RAM and I/O
- Internal counter/timer
- Internal oscillator, clock driver
- Single-level interrupts: external and counter/timer
- 17 internal registers: accumulator, 16 addressable registers
- Over 90 instructions: 70% single byte
- All instructions 1 or 2 cycles
- Easily expandable memory and 27 I/O lines
- TTL compatible inputs and outputs
- Single 5 V supply
- Standard and extended temperature range (see Table 1 next page)

Applications

- Peripheral interfaces and controllers
- Test and measuring instruments
- Sequencers
- Modems and data enciphering
- Environmental control systems
- Audio/video systems

PACKAGE OUTLINES

All versions: with type no. suffix P (see Table 1 next page): 40-lead DIL; plastic (SOT-129).
MAB80XXH/HLWP: 44-lead plastic leaded chip-carrier (PLCC); SOT-187A.

Table 1 MAB80XXH versions

version	internal memory		RAM st/by.	frequency (MHz) min.	frequency (MHz) max.	temperature range (°C)
MAB8048H	1 K x 8 ROM	64 byte RAM	yes	1,0	11,0	0 to + 70
MAB8035HL	none	64 byte RAM	yes	1,0	11,0	0 to + 70
MAF8048H	1 K x 8 ROM	64 byte RAM	yes	1,0	11,0	−40 to + 85
MAF8035HL	none	64 byte RAM	yes	1,0	11,0	−40 to + 85
MAF80A48H	1 K x 8 ROM	64 byte RAM	yes	1,0	10,0	−40 to + 110
MAF80A35HL	none	64 byte RAM	yes	1,0	10,0	−40 to + 110
MAB8049H	2 K x 8 ROM	128 byte RAM	yes	1,0	11,0	0 to + 70
MAB8039HL	none	128 byte RAM	yes	1,0	11,0	0 to + 70
MAF8049H	2 K x 8 ROM	128 byte RAM	yes	1,0	11,0	−40 to + 85
MAF8039HL	none	128 byte RAM	yes	1,0	11,0	−40 to + 85
MAF80A49H	2 K x 8 ROM	128 byte RAM	yes	1,0	10,0	−40 to + 110
MAF80A39HL	none	128 byte RAM	yes	1,0	10,0	−40 to + 110
MAB8050H	4 K x 8 ROM	256 byte RAM	yes	1,0	6,0	0 to + 70
MAB8040HL	none	256 byte RAM	yes	1,0	6,0	0 to + 70
MAF8050H	4 K x 8 ROM	256 byte RAM	yes	1,0	6,0	−40 to + 85
MAF8040HL	none	256 byte RAM	yes	1,0	6,0	−40 to + 85
MAF80A50H	4 K x 8 ROM	256 byte RAM	yes	1,0	6,0	−40 to + 110
MAF80A40HL	none	256 byte RAM	yes	1,0	6,0	−40 to + 110

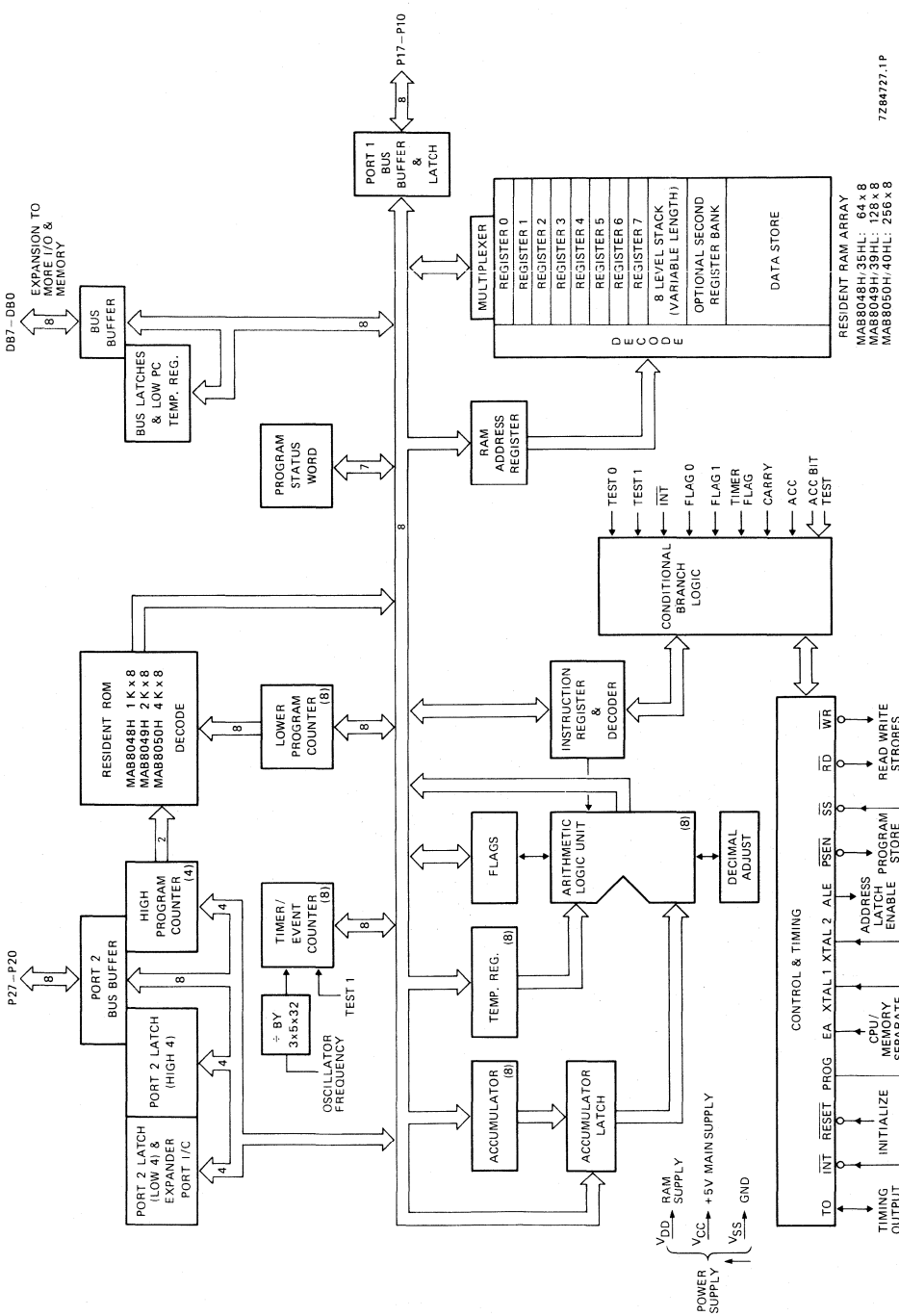


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB84XX family of microcontrollers is fabricated in NMOS. The family consists of the following devices:

- MAB8401 – 128 RAM bytes, external program memory plus 8-bit LED-driver (10 mA), emulation of MAB/F8422/42* possible
- MAB/F8411 – 1K ROM/ 64 RAM bytes plus 8-bit LED-driver
- MAB/F8421 – 2K ROM/ 64 RAM bytes plus 8-bit LED-driver
- MAB/F8441 – 4K ROM/128 RAM bytes plus 8-bit LED-driver
- MAB/F8461 – 6K ROM/128 RAM bytes plus 8-bit LED-driver

Each version has 20 quasi-bidirectional I/O port lines, one serial I/O line, one single-level vectored interrupt, an 8-bit timer event counter and on-board clock oscillator and clock circuits. Two 20-pin versions, MAB/F8422 and MAB/F8442* are also available.

This microcontroller family is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048. The microcontrollers have extensive bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the "Users manual Single-chip microcomputers" (supplied upon request).

* See data sheet on MAB/F8422/42.

Features

- 8-bit: CPU, ROM, RAM and I/O in a single 28-lead DIL package
- 1K, 2K, 4K or 6K ROM bytes plus a ROM-less version
- 64 or 128 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two testable inputs: one of which can be used to detect zero cross-over, the other is also the external interrupt input
- Single level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O that can be used in single or multi-master systems (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single 5 V power supply (± 10%)
- Operating temperature ranges:

0 to + 70 °C	MAB84XX	family
−40 to + 85 °C	MAF84XX	family (extended temperature)
−40 to + 110 °C	MAF84AXX	family (automotive temperature)

PACKAGE OUTLINES

MAB8401B: 28-lead 'Piggy-back' package (with up to 28-pin EPROM on top).
MAB8401WP: 68-lead plastic leaded chip-carrier (PLCC) (SOT-188A).
MAB/F8411/21/41/61P: 28-lead DIL; plastic (SOT-117D).
MAF84A11/A21/A41/A61P: 28-lead DIL; plastic (SOT-117D).
MAB8411/21/41/61T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

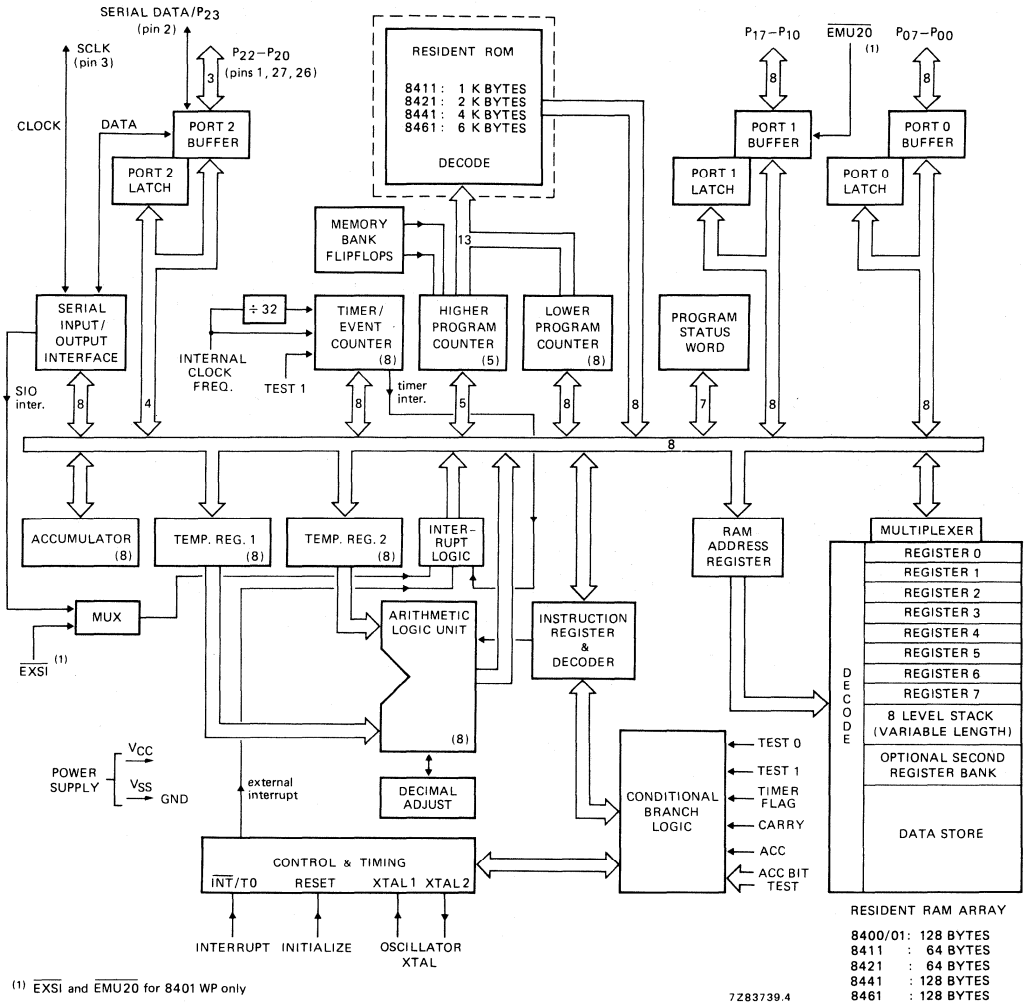


Fig. 4(a) Block diagram of the MAB84XX family.

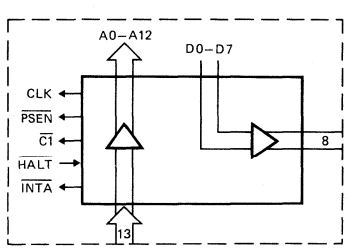


Fig. 4(b) Replacement for dotted part in Fig. 4(a) for the MAB8401WP bond-out version.

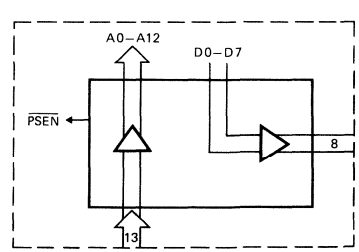


Fig. 4(c) Replacement of dotted part in Fig. 4(a) for the MAB8401B 'Piggy-back' version.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

The MAB8422/8442 is a high-performance microcontroller incorporating dedicated hardware, memory capacity and I/O lines. This dedication means a microcontroller can be economically installed in high-volume products where its main function is control.

The MAB8422/8442 is a 20 pin, single-chip 8-bit microcontroller that has been developed from the 28 pin MAB8421/8441 microcontrollers. The versions are:

- MAB8422 - 2K ROM/64 RAM bytes plus 8-bit LED-driver
- MAB8442 - 4K ROM/128 RAM bytes plus 8-bit LED-driver

Each version has 15 I/O port lines comprising one 8-bit parallel port (P0), one 2-bit parallel port (P10 and P11 that are shared with the serial I/O lines SDA and SCL), one 3-bit parallel port (P20-P22) and two input lines ($\overline{INT}$/T0 and T1).

The serial I/O interface is I^2C compatible and therefore the MAB8422/8442 can operate as a slave or a master in single and multi-master systems. Conversion from parallel to serial data when transmitting, and vice versa when receiving, is done mainly in software. There is a minimum of hardware for the serial I/O implemented. This hardware is controlled by the status of the SDA and SCL lines and can be read or written under software control. Standard software for I^2C-bus control is available on request.

Features

- 8-bit: CPU, ROM, RAM and I/O
- 20 pin package
- MAB8422: 2K ROM/64 RAM bytes
- MAB8442: 4K ROM/128 RAM bytes
- 13 quasi-bidirectional I/O port lines
- Two testable inputs $\overline{INT}$/T0 and T1
- High current output on P0 (I_{OL} = 10 mA at V_{OL} = 1 V)
- One interrupt line combined with the testable input line $\overline{INT}$/T0
- Single-level interrupts: external, timer/event counter, serial I/O
- I^2C-compatible serial I/O that can be used in single or multi-master systems (serial I/O data and clock via P10 and P11 port lines, respectively)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles, cycle time dependent on oscillator frequency
- Single 5 V power supply
- 0 to 70 °C operating temperature range, also versions for −40 to 85 °C (extended temperature range) and −40 to 110 °C (automotive temperature range)

PACKAGE OUTLINES

MAB/F8422/42P: 20-lead DIL; plastic (SOT-146).
MAF84A22/A42P: 20-lead DIL; plastic (SOT-146).

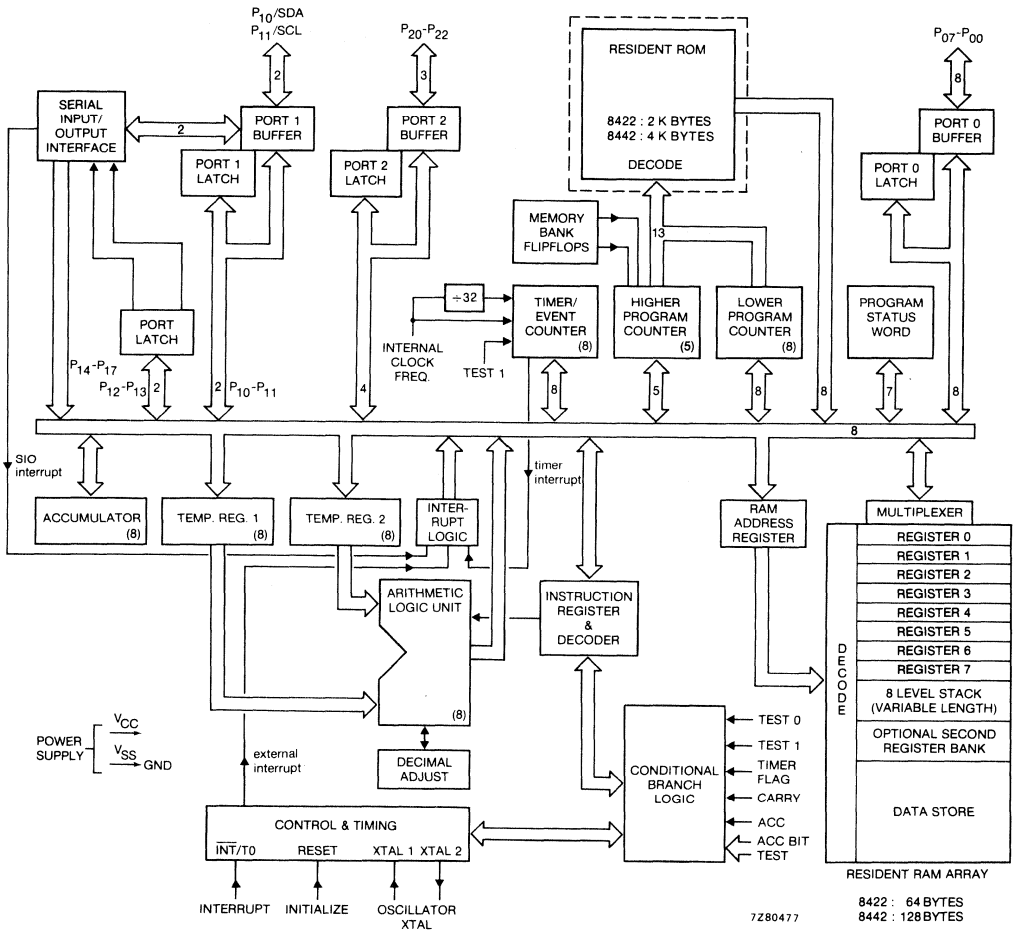


Fig. 1 Block diagram of the MAB8422/8442.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The PCB80C51 family of single-chip 8-bit microcontrollers is manufactured in an advanced CMOS process. The family consists of the following members:

- PCB80C31: ROM-less version of the PCB80C51
- PCB80C51: 4 K bytes mask-programmable ROM, 128 bytes RAM

In the following, the generic term "PCB80C51" is used to refer to both family members.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 K bytes of program memory and/or up to 64 K bytes of data storage.

The PCB80C51 contains a non-volatile 4 K x 8 read-only program memory (not ROM-less version); a volatile 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/event counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB80C51 can be expanded using standard TTL compatible memories and logic.

The PCB80C31/80C51 has two software selectable modes of reduced activity for further power reduction – Idle and Power Down.
The Idle modes freezes the CPU while allowing the RAM, timers, serial port and interrupt system to continue functioning.
The Power Down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

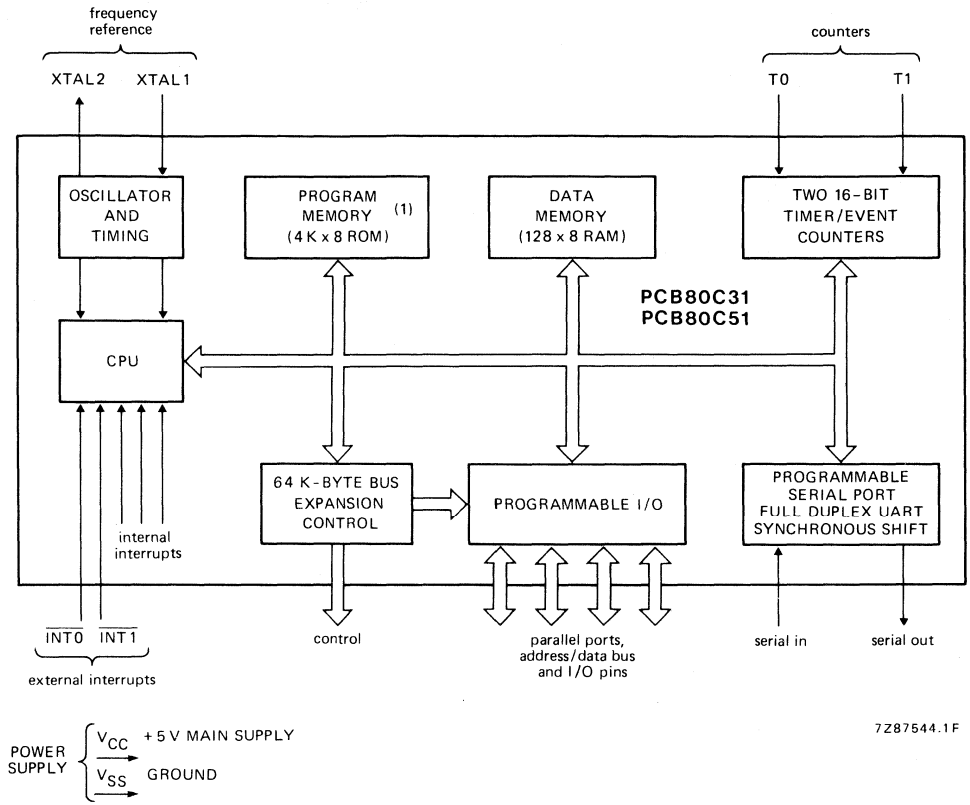
The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of 255 instructions; 44% one-byte, 41% two-byte and 15% three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs. Multiply, divide, subtract and compare are among the many instructions added to the standard PCB80C48 instruction set.
Software development to be announced: PCB85C51 in piggy-back and 84 pin PLCC.

Features

- 4 K x 8 ROM (80C51 only), 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- Full-duplex serial port
- External memory expandable to 128 K, external ROM up to 64 K and/or external RAM up to 64 K
- Boolean processing
- 218 bit-addressable locations
- On-chip oscillator
- Five-source interrupt structure with two priority levels
- 58% of instructions executed in 1 μs; multiply and divide in 4 μs; all others executed in 2 μs (at 12 MHz clock)
- Enhanced architecture with:
  - non-page-oriented-instructions
  - direct addressing
  - four 8-byte + 1 byte register banks
  - stack depth up to 128-bytes
  - multiply, divide, subtract and compare instructions.

PACKAGE OUTLINES

PCB80C31/51P: 40-lead DIL; plastic (SOT-129).
PCB80C31/51WP: 44-lead PLCC; plastic, leaded-chip-carrier (SOT-187A).



(1) PCB80C51 only.

Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT CMOS MICROCONTROLLER

DESCRIPTION

The PC80CXX family of single-chip 8-bit CMOS microcontrollers consists of:

- The PCB80C49 with resident mask programmed ROM.
- The PCB80C39 without resident program memory for use with external EPROM/ROM.

All versions are pin and function compatible to their NMOS counter parts but with additional features and high performance.

The PC80CXX family are designed to be efficient control processors as well as arithmetic processors. Their instruction set allows the user to directly set and reset individual I/O lines as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions enable efficient implementation of standard logic functions. Code efficiency is high; over 70% of the instructions are single byte; all others are two byte.

An on-chip 8-bit counter is provided, which can count either machine cycles (÷ 32) or external events. The counter can be programmed to cause an interrupt to the processor.
Program and data memories can be expanded using standard devices. Input/output capabilities can be expanded using standard devices.
The family has low power consumption and in addition a power down mode is provided.

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 40-pin package
- PCB80C49: 2K x 8 ROM, 128 x 8 RAM
- Internal counter/timer
- Internal oscillator, clock driver
- Single-level interrupts: external and counter/timer
- 17 internal registers: accumulator, 16 addressable registers
- Over 90 instructions: 70% single byte
- All instructions: 1 or 2 cycles
- Easily expandable memory and I/O
- TTL compatible inputs and outputs
- Single 5 V supply
- Wide frequency operating range
- Low current consumption
- Also available with extended temperature range;
  PCF 80CXX = −40 °C to + 85 °C

APPLICATIONS

- Peripheral interfaces and controllers
- Test and measurement instruments
- Sequencers
- Audio/video systems
- Environmental control systems
- Modems and data enciphering

PACKAGE OUTLINES

PCB/F80C39/C49P: 40-lead DIL; plastic (SOT-129).
PCB80C39/C49WP: 44-lead plastic leaded chip-carrier (PLCC); SOT-187A.

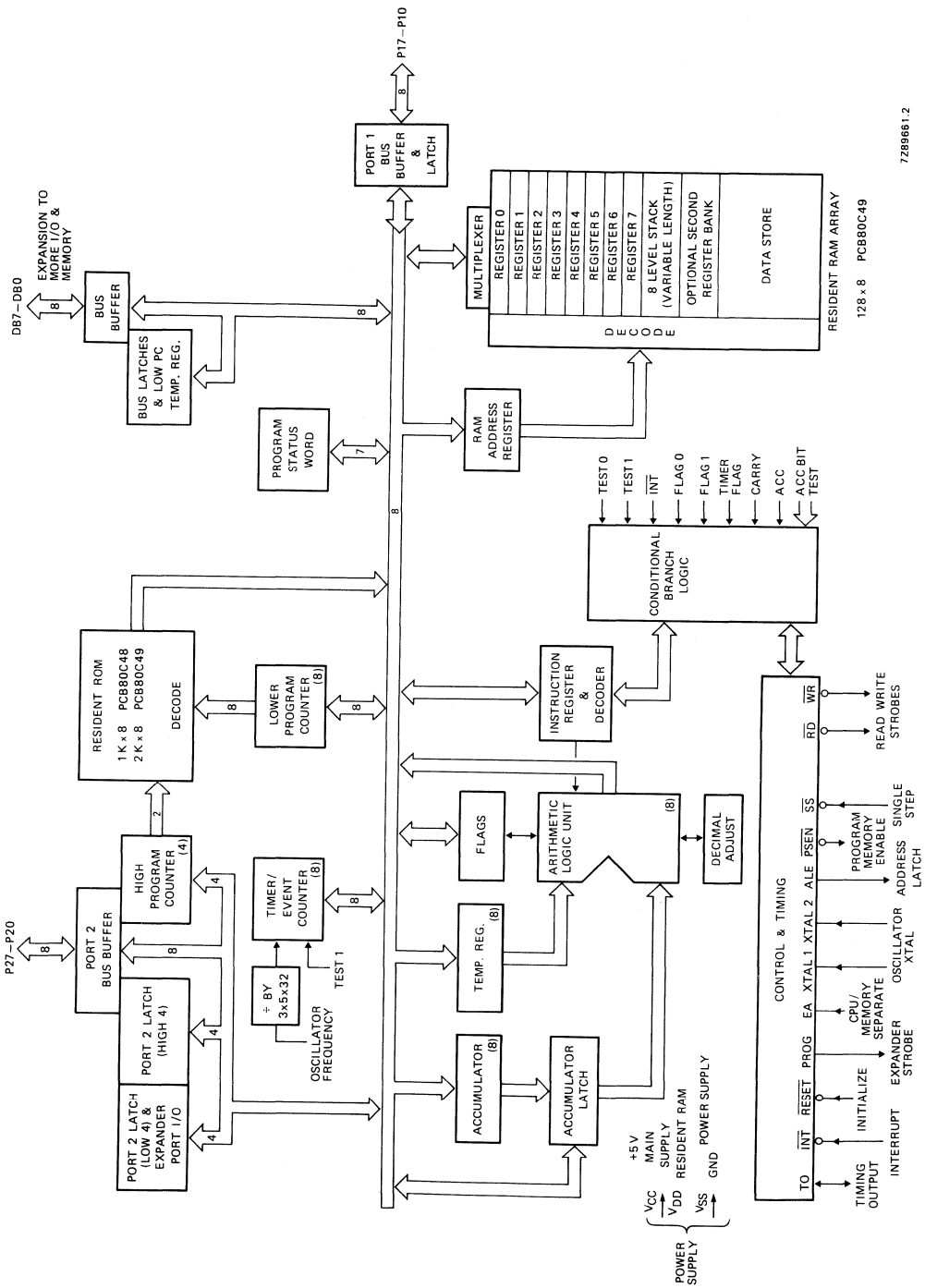


Fig. 1 Block diagram.

STATIC CMOS EEPROM (256 x 8 BIT)

GENERAL DESCRIPTION

The PCB8582 is a 2K-bit 5 V electrically erasable programmable read only memory (EEPROM) organized as 256 by 8 bits. It is designed in a floating gate CMOS technology.

As data bytes are received and transmitted via the serial I^2C bus, an eight pin DIL package is sufficient. Up to eight PCB8582 devices may be connected to the I^2C bus.

Chip select is accomplished by three address inputs.

Features

- Non-volatile storage of 2K-bit organized as 256 x 8
- Only one power supply required (5 V)
- On chip voltage multiplier for erase/write
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- Power on reset
- 10 000 erase/write cycles per byte
- 10 years non-volatile data retention
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571 and PCD8572 ←

PACKAGE OUTLINE

PCB8582P: 8-lead DIL; plastic (SOT-97A).

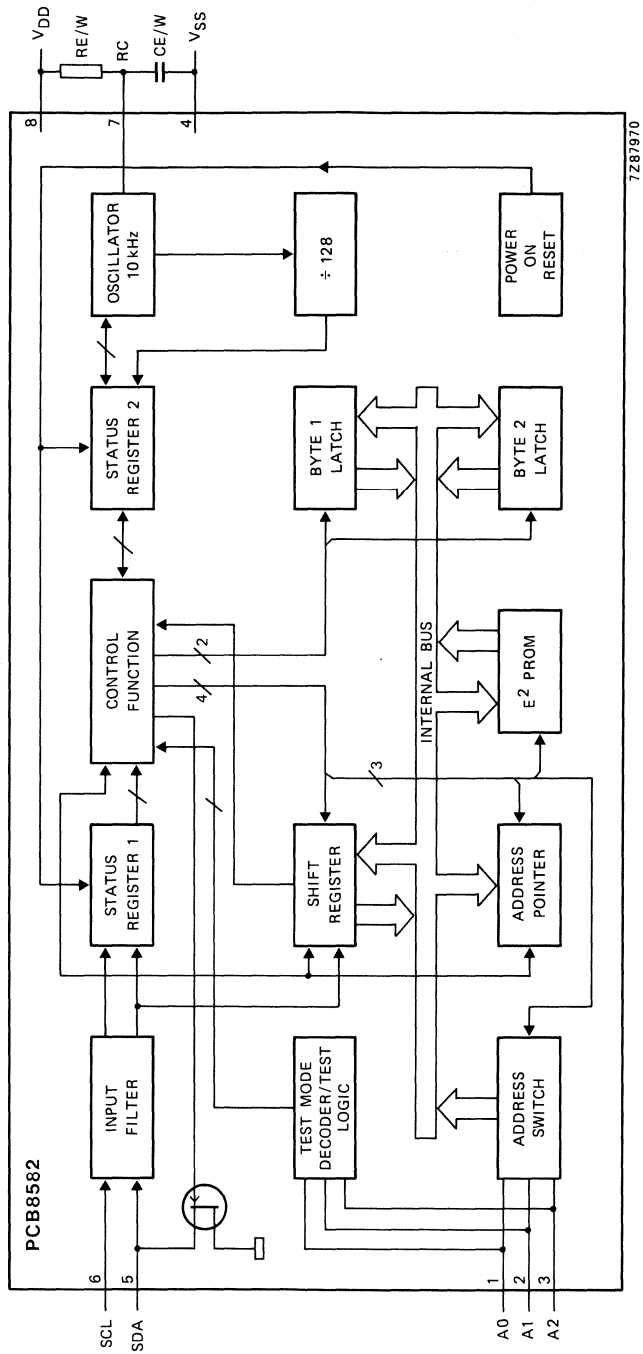


Fig. 1 Block diagram.

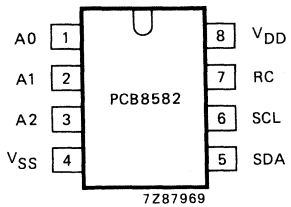


Fig. 2 Pinning diagram.

1 A0
2 A1 address inputs/test
3 A2 mode select
4 V_{SS} ground
5 SDA, 6 SCL: I^2C bus lines
7 RC input for timer constant
8 V_{DD} positive supply

FUNCTIONAL DESCRIPTION

Characteristics of the I^2C bus

The I^2C bus is intended for communication between different ICs. The serial bus consists of two bi-directional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:
Data transfer may be initiated only when the bus is not busy.
During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:
Bus not busy: both data and clock lines remain HIGH.
Start data transfer: a change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines the start condition.
Stop data transfer: a change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the stop condition.
Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transfered between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I^2C bus specifications a low-speed mode (2 kHz clock rate) and a high-speed mode (100 kHz clock rate) are defined. The PCB8582 works in both modes.
By definition a device that gives out a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse.
Set-up-and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

DEVELOPMENT DATA

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

I²C bus protocol

The I²C bus configuration for different READ and WRITE cycles of the PCB8582 are shown in Fig. 3, (a) and (b).

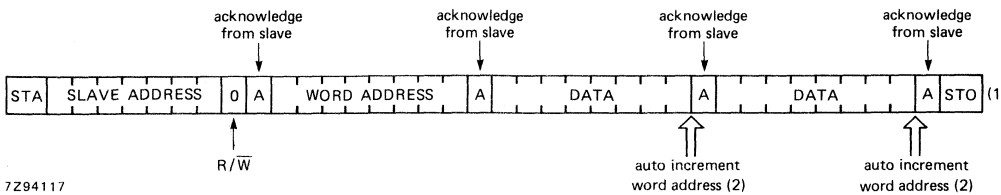


Fig. 3(a) Slave receiver ERASE/WRITE mode.

1. After this stop condition the erase/write cycle starts and the bus is free for another transmission; the duration of the erase/write cycle is approximatly 20 ms if only one byte is written, and 40 ms, if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via I²C bus.
2. The second data byte is voluntary. Trying to erase/write more than two bytes is not allowed.

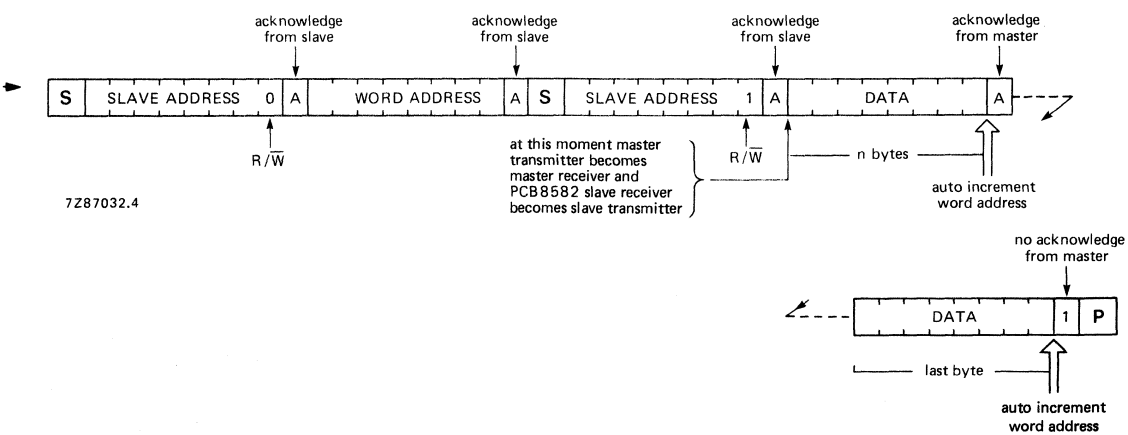


Fig. 3(b) Master reads PCB8582 slave after setting word address. (WRITE word address; READ data).

→ **Note:** The slave address is defined in accordance with the I²C bus specification as:

1	0	1	0	A2	A1	A0	R/W

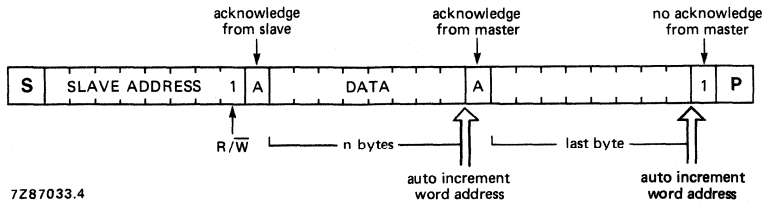


Fig. 3(c) Master reads PCB8582 slave immediately after first byte (READ mode).

I²C bus timing

Fig. 4 shows the I²C bus timing.

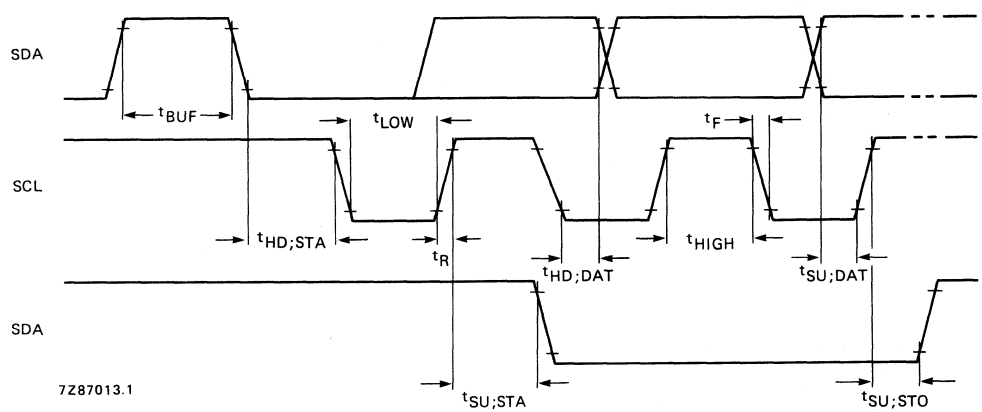


Fig. 4 Timing requirements for the I²C bus.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 7	V
Voltage, on any input pin (input impedance 500 Ω)	V_I	V_{SS}−0,8 to V_{DD} +0,8	V
Operating temperature range	T_{amb}	0 to +70	°C
Storage temperature range	T_{stg}	−65 to +150	°C
Current into any input pin	I_I	1	mA
Output current	I_O	10	mA

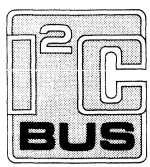
CHARACTERISTICS

→ V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 0 to + 70 °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	4,5	5	5,5	V
Operating supply current, READ (f_{SLC} = 100 kHz)	I_{DDR}	–	0,1	–	mA
Operating supply current, WRITE/ERASE	I_{DDW}	–	1	–	mA
Standby supply current (V_{DD} = 5 V)	I_{DDO}	–	5	–	μA
Input SCL					
Input/output SDA:					
Input voltage LOW	V_{IL}	–0,3	–	1,5	V
Input voltage HIGH	V_{IH}	3	–	V_{DD}+0,8	V
Output voltage LOW (I_{OL} = 3 mA, V_{DD} = 4,5 V)	V_{OL}	–	–	0,4	V
Output leakage current HIGH (V_{OH} = V_{DD})	I_{OH}	–	–	1	μA
Input leakage current (A0,A1,A2, SCL), (note 1)	$\pm I_{IN}$	–	–	1	μA
Clock frequency	f_{SCL}	0	–	100	kHz
Input capacity (SCL,SDA)	C_I	–	–	7	pF
Noise suppression time constant at SCL and SDA input	t_I	0,25	0,5	1	μs
Time the bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Hold time start condition. After this period the first clock pulse is generated	$t_{HD;STA}$	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
Set-up time for start condition (only relevent for a repeated start condition)	$t_{SU;STA}$	4,7	–	–	μs
Hold time DATA for:					
CBUS compatible masters	$t_{HD;DAT}$	5	–	–	μs
I^2C devices (note 2)	$t_{HD;DAT}$	0	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Rise time for both SDA and SCL lines	t_R	–	–	1	μs
Fall time for both SDA and SCL lines	t_F	–	–	300	ns
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Erase/write timer constant (note 3)					
Erase/write cycle time	$t_{E/W}$	20	–	100	ms
Erase/write timing capacitor for erase/write cycle of 30 ms	$C_{E/W}$	–	3,3	–	nF
Erase/write timing resistor for erase/write cycle of 30 ms	$R_{E/W}$	–	56	–	kΩ
Data retention time	t_S	10	–	–	years

Notes to the characteristics

1. Selection of the chip address is done by connecting the A0, A1, and A2 inputs either to V_{SS} or V_{DD}.
2. A transmitter must internally provide a hold time to bridge the undefined region (maximum 300 ns) of the falling edge of SCL.
3. Endurance (number of erase/write cycles), NE/W, is 10^4 E/W cycles.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

DEVELOPMENT DATA

LCD DUPLEX DRIVER

GENERAL DESCRIPTION

The PCF2100 is a single chip, silicon gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 40 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- 40 LCD-segment drive capability
- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility

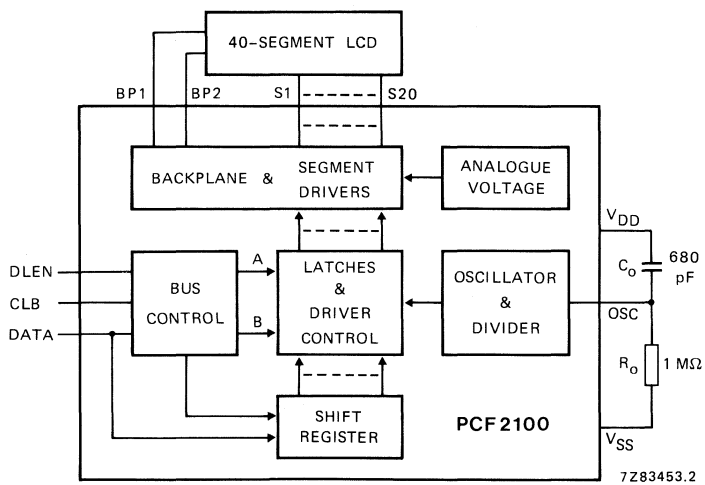


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF2100P: 28-lead DIL; plastic (SOT-117D).
PCF2100T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_n	V_{SS} −0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−40 to + 85 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,25 to 6,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; R_o = 1 MΩ; C_o = 680 pF; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply current	no external load	I_{DD}	–	10	50	μA
Supply current	no external load; T_{amb} = −25 to + 85 °C	I_{DD}	–	–	30	μA
Display frequency	see Fig. 8; T = 680 μs	f_{LCD}	60	80	100	Hz
D.C. component of LCD drive	with respect to V_{SX}	V_{BP}	–	± 10	–	mV
Load on each segment driver			–	–	10	MΩ
			–	–	500	pF
Load on each backplane driver			–	–	1	MΩ
			–	–	5	nF
Input voltage HIGH	see Fig. 9	V_{IH}	2	–	–	V
Input voltage LOW	see Fig. 9	V_{IL}	–	–	0,6	V
Rise time V_{BP} to V_{SX}	max. load	t_r	–	20	–	μs
Inputs CLB, DATA, DLEN	see note on next page					
Rise and fall times	see Fig. 2	t_r, t_f	–	–	10	μs
CLB pulse width HIGH	see Fig. 2	t_{WH}	1	–	–	μs
CLB pulse width LOW	see Fig. 2	t_{WL}	9	–	–	μs

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Data set-up time DATA → CLB	see Fig. 2	t_{SUDA}	8	–	–	μs
Data hold time DATA → CLB	see Fig. 2	t_{HDDA}	8	–	–	μs
Enable set-up time DLEN → CLB	see Fig. 2	t_{SUEN}	1	–	–	μs
Disable set-up time CLB → DLEN	see Fig. 2	t_{SUDI}	8	–	–	μs
Set-up time (load pulse) DLEN → CLB	see Fig. 2	t_{SULD}	8	–	–	μs
Busy-time from load pulse to next start of transmission	see Fig. 2	t_{BUSY}	8	–	–	μs
Set-up time (leading zero) DATA → CLB	see Fig. 2	t_{SULZ}	8	–	–	μs

Note

All timing values are referred to $V_{IH\,min}$ and $V_{IL\,max}$* (see Fig. 2). If external resistors are used in the bus lines (see Fig. 9), the extra time constant has to be added.

* With an input voltage swing of V_{ILmax} – 0,1 V to V_{IHmin} + 0,1 V.

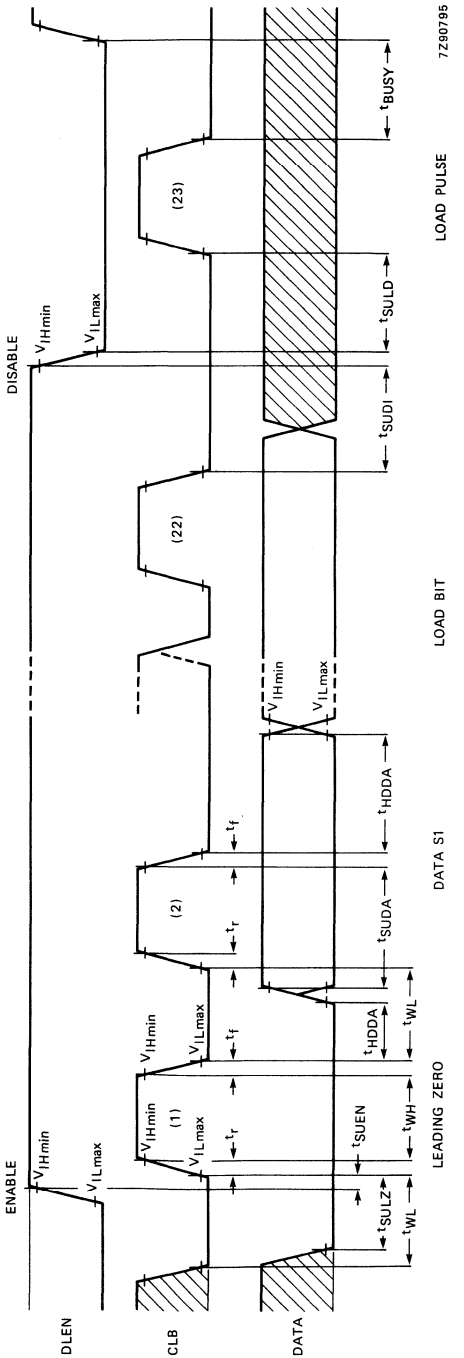


Fig. 2 CBUS timing.

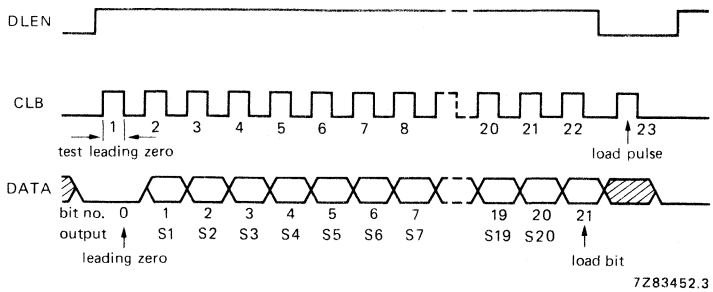


Fig. 3 CBUS data format.

Notes to Fig. 3

An LCD segment is activated when the corresponding DATA-bit is HIGH.

When DATA-bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 21 LOW, the B-latches (BP2) are loaded.
CLB-pulse 23 transfers data from shift register to selected latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load conditions (load pulse width DLEN is LOW) and the driver is ready to receive new data.

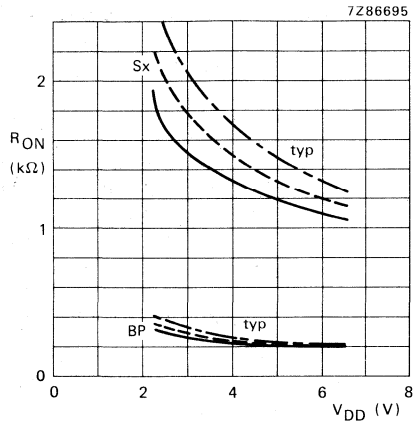


Fig. 4 Output resistance of backplane and segments.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

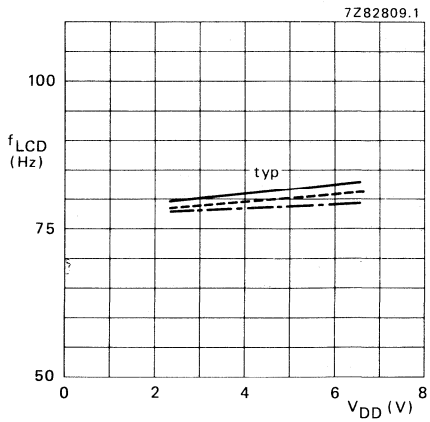


Fig. 5 Display frequency as a function of supply voltage; R_oC_o = 680 μs.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

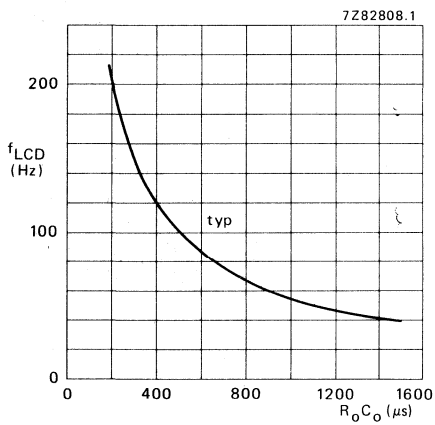


Fig. 6 Display frequency as a function of R_o x C_o time; T_{amb} = 25 °C.

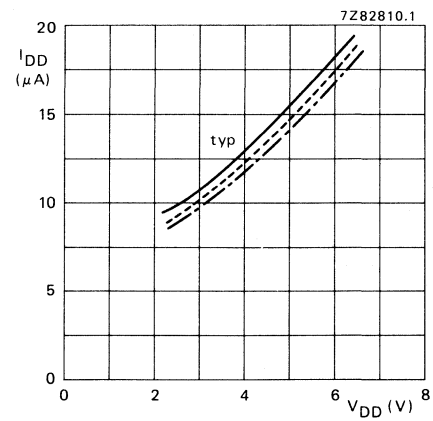


Fig. 7 Supply current as a function of supply voltage.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

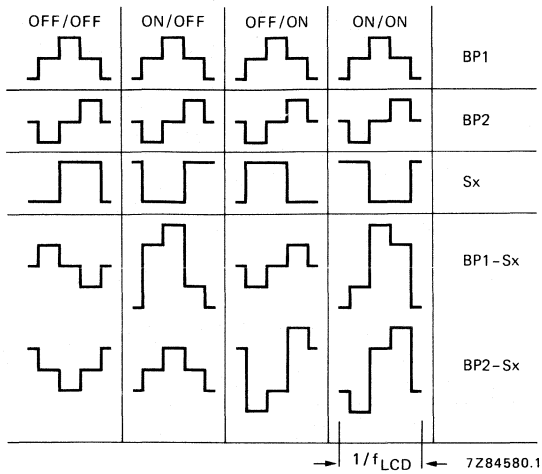


Fig. 8 Timing diagram.

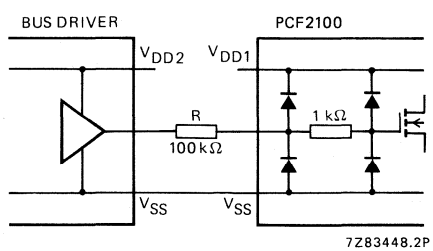
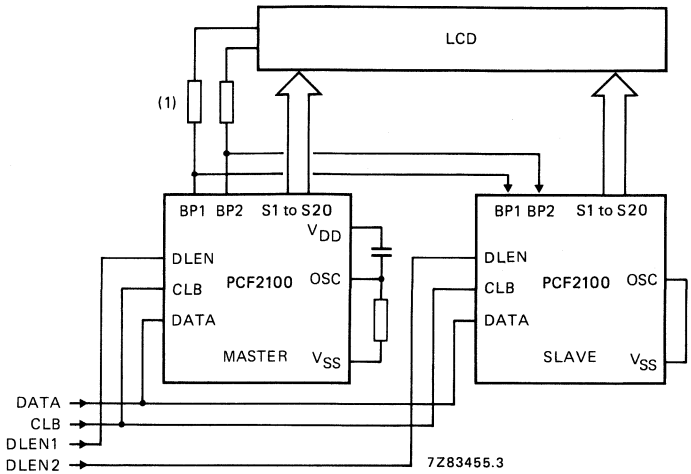


Fig. 9 Input circuitry.

Note to Fig. 9

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current $\leqslant 40\ \mu A$.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2100 and the backplane of the LCD must be $> 2{,}7\ k\Omega$. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 10 Diagram showing expansion possibility.

Note to Fig. 10

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2111, PCF2110 and PCF2100 ICs up to the BP drive capability of the master.

PCF2111 is a 64 LCD-segment driver.
PCF2110 is a 60 LCD-segment driver plus 2 LED driver outputs.

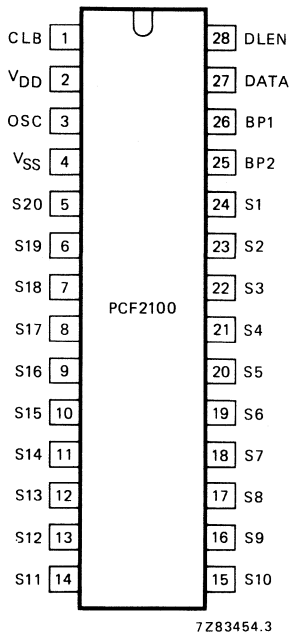


Fig. 11 Pinning diagram.

PINNING

Supply

2	V_{DD}	Positive supply
4	V_{SS}	Negative supply

Inputs

3	OSC	Oscillator input	
27	DATA	Data line	CBUS
28	DLEN	Data line enable	CBUS
1	CLB	Clock burst	CBUS

Outputs

26	BP1	Backplane drivers (common of LCD)
25	BP2	Backplane drivers (common of LCD)
S1 to S20		LCD driver outputs

LCD DUPLEX DRIVER

GENERAL DESCRIPTION

The PCF2110 is a single chip, silicon gate CMOS circuit designed to drive 2 LEDs (Light Emitting Diodes) and an LCD (Liquid Crystal Display) with up to 60 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- 60 LCD-segment drive capability
- Two LED-driver outputs
- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility

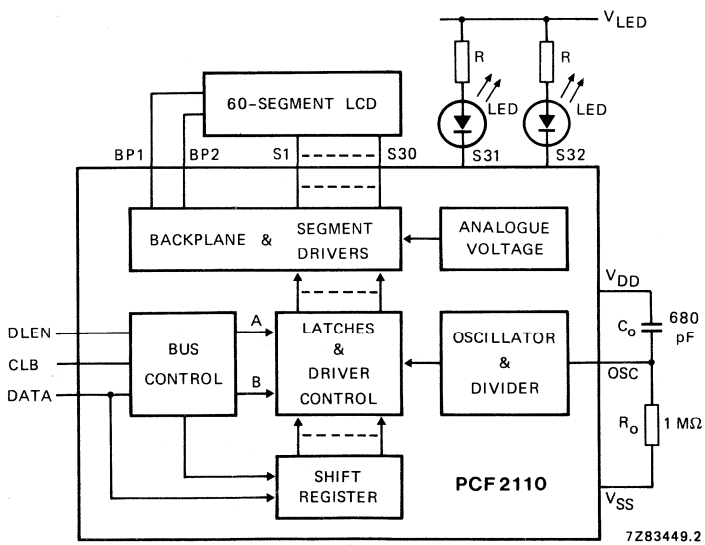


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF2110P: 40-lead DIL; plastic (SOT-129).
PCF2110T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{DD}		−0,3 to 8 V
Voltage on any pin	V_n	V_{SS}	−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}		−40 to + 85 °C
Storage temperature range	T_{stg}		−55 to + 125 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,25 to 6,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; R_o = 1 MΩ; C_o = 680 pF; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply current	no external load	I_{DD}	–	10	50	μA
Supply current	no external load; T_{amb} = −25 to + 85 °C	I_{DD}	–	–	30	μA
Display frequency	see Fig. 9; T = 680 μs	f_{LCD}	60	80	100	Hz
D.C. component of LCD drive	with respect to V_{SX}	V_{BP}	–	± 10	–	mV
Load on each segment driver			–	–	10	MΩ
			–	–	500	pF
Load on each backplane driver			–	–	1	MΩ
			–	–	5	nF
Input voltage HIGH	see Fig. 10	V_{IH}	2	–	–	V
Input voltage LOW	see Fig. 10	V_{IL}	–	–	0,6	V
Rise time V_{BP} to V_{SX}	max. load	t_r	–	20	–	μs
LED outputs S31, S32	V_{DD} = 3 V; T_{amb} = 25 °C					
Output resistance	V_{OL} = 0,2 V; see Fig. 4	R_{out}	–	–	25	Ω
Drain voltage	N-channel OFF	V_{LED}	–	–	8	V
Drain current	maximum value	I_{LEDmax}	–	–	50	mA
Total power dissipation		P_{tot}	–	–	400	mW
Inputs CLB, DATA, DLEN	see note on next page					
Input capacitance	for SOT-129 package	C_{IN}	–	–	10	pF
	for SOT-158A package	C_{IN}	–	–	5	pF
Rise and fall times	see Fig. 2	t_r, t_f	–	–	10	μs
CLB pulse width HIGH	see Fig. 2	t_{WH}	1	–	–	μs
CLB pulse width LOW	see Fig. 2	t_{WL}	9	–	–	μs

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Data set-up time DATA → CLB	see Fig. 2	t_{SUDA}	8	–	–	μs
Data hold time DATA → CLB	see Fig. 2	t_{HDDA}	8	–	–	μs
Enable set-up time DLEN → CLB	see Fig. 2	t_{SUEN}	1	–	–	μs
Disable set-up time CLB → DLEN	see Fig. 2	t_{SUDI}	8	–	–	μs
Set-up time (load pulse) DLEN → CLB	see Fig. 2	t_{SULD}	8	–	–	μs
Busy-time from load pulse to next start of transmission	see Fig. 2	t_{BUSY}	8	–	–	μs
Set-up time (leading zero) DATA → CLB	see Fig. 2	t_{SULZ}	8	–	–	μs

Note

All timing values are referred to $V_{IH\,min}$ and $V_{IL\,max}$*(see Fig. 2). If external resistors are used in the bus lines (see Fig. 10), the extra time constant has to be added.

* With an input voltage swing of $V_{IL\,max}$–0,1 V to V_{IHmin} + 0,1 V.

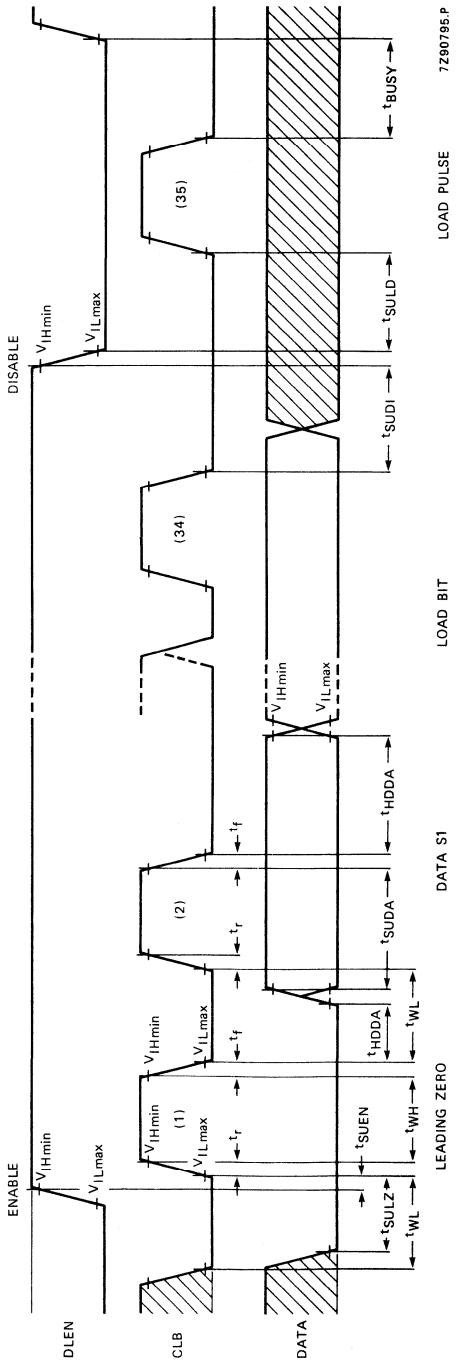


Fig. 2 CBUS timing.

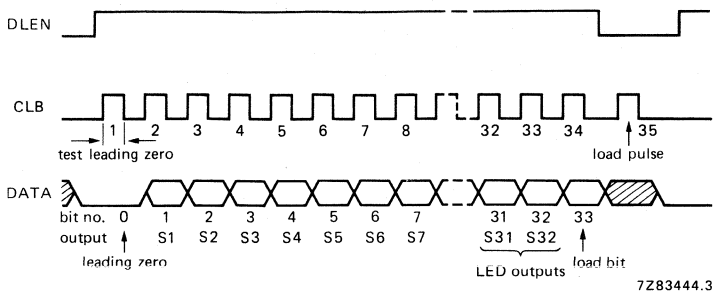


Fig. 3 CBUS data format.

Notes to Fig. 3

An LCD segment is activated when the corresponding DATA-bit is HIGH.

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. Bits 31 and 32 contain the LED output information. With DATA-bit 33 LOW, the B-latches (BP2) are loaded and bits 31 and 32 are ignored. CLB-pulse 35 transfers data from shift register to selected latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN is LOW) and the driver is ready to receive new data.

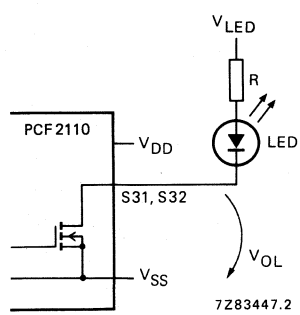


Fig. 4 LED driver circuitry.

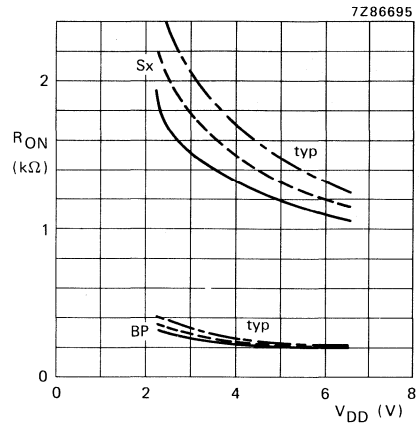


Fig. 5 Output resistance of backplane and segments.
——— T_{amb} = −40 °C; − − − T_{amb} = + 25 °C; −·−· T_{amb} = +85 °C.

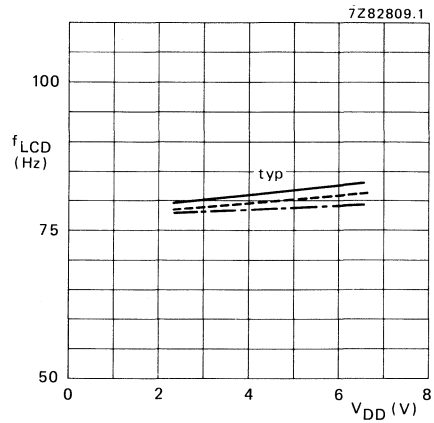


Fig. 6 Display frequency as a function of supply voltage; R_oC_o = 680 μs.
——— T_{amb} = −40 °C; − − − T_{amb} = + 25 °C; −·−· T_{amb} = +85 °C.

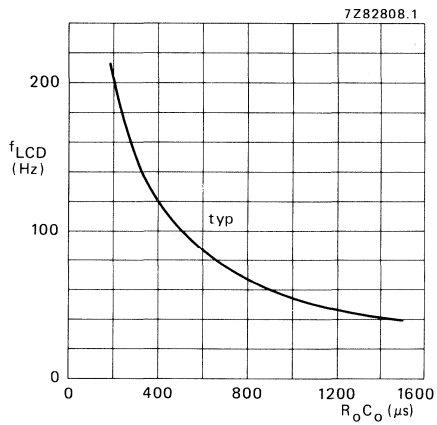


Fig. 7 Display frequency as a function of R_o x C_o time; T_{amb} = 25 °C.

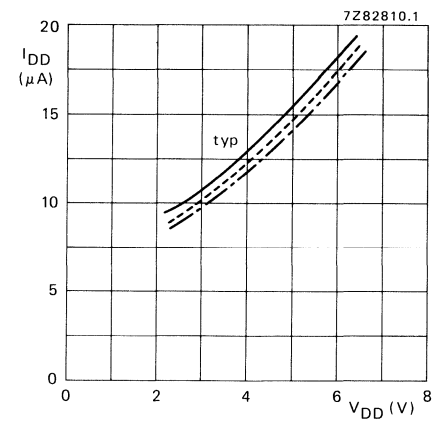


Fig. 8 Supply current as a function of supply voltage.
——— T_{amb} = −40 °C; − − − T_{amb} = + 25 °C; −·−· T_{amb} = +85 °C.

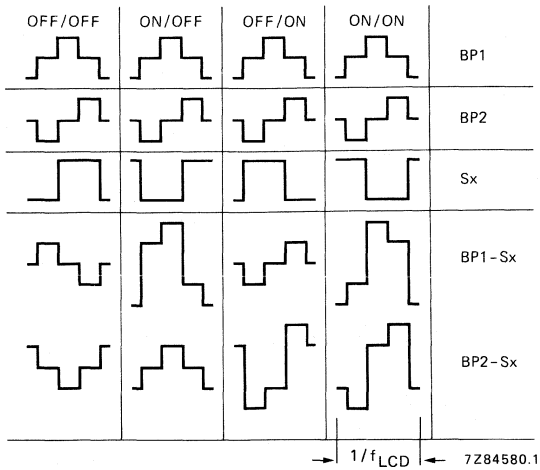


Fig. 9 Timing diagram.

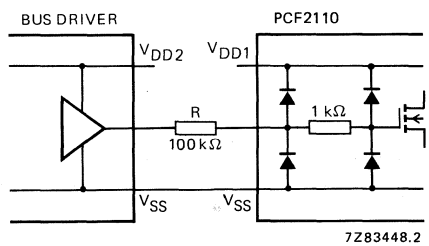
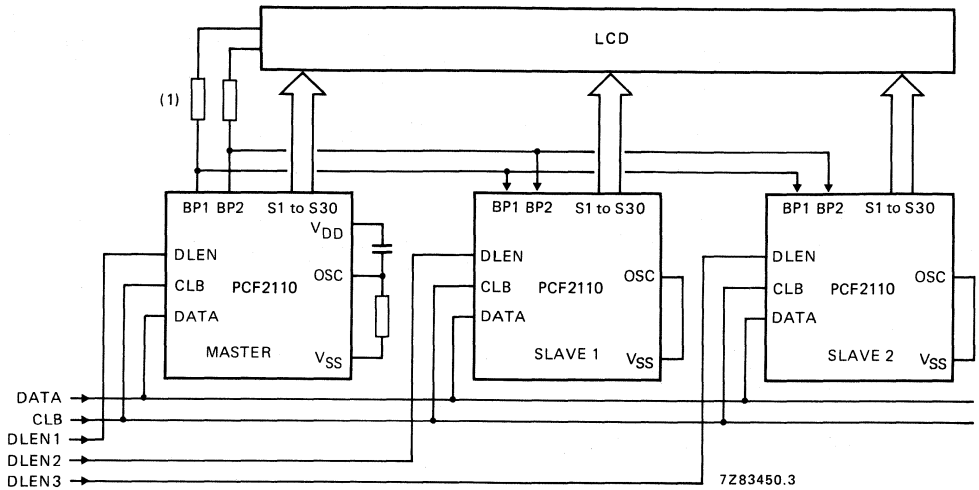


Fig. 10 Input circuitry.

Note to Fig. 10

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current $\leq 40\ \mu A$.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2110 and the backplane of the LCD must be $> 2{,}7\ k\Omega$. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 11 Diagram showing expansion possibility.

Note to Fig. 11

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2100, PCF2110 and PCF2111 ICs up to the BP drive capability of the master.

PCF2100 is a 40 LCD-segment driver.
PCF2111 is a 64 LCD-segment driver.

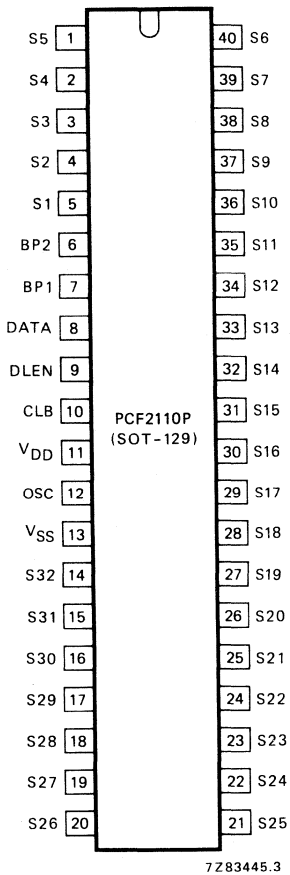


Fig. 12 Pinning diagram for SOT-129 package.

PINNING

Supply

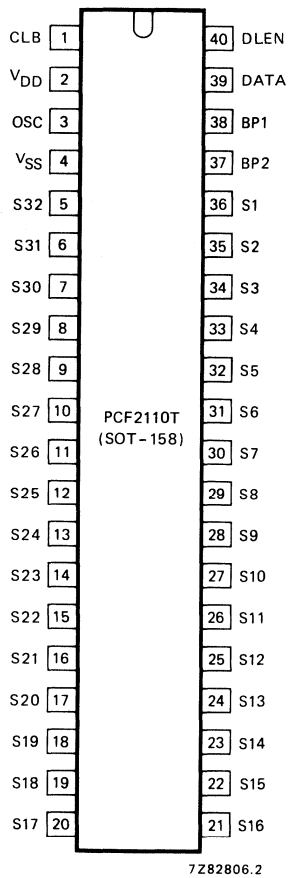
11	V_{DD}	Positive supply
13	V_{SS}	Negative supply

Inputs

12	OSC	Oscillator input	
8	DATA	Data line	CBUS
9	DLEN	Data line enable	CBUS
10	CLB	Clock burst	CBUS

Outputs

7	BP1	Backplane drivers (common of LCD)
6	BP2	Backplane drivers (common of LCD)
S1 to S30		LCD driver outputs
S31, S32		LED driver outputs



PINNING

Supply

2	V_{DD}	Positive supply
4	V_{SS}	Negative supply

Inputs

3	OSC	Oscillator input	
39	DATA	Data line	CBUS
40	DLEN	Data line enable	CBUS
1	CLB	Clock burst	CBUS

Outputs

38	BP1	Backplane drivers (common of LCD)
37	BP2	Backplane drivers (common of LCD)
S1 to S30		LCD driver outputs
S31, S32		LED driver outputs

Fig. 13 Pinning diagram for VSO-40; SOT-158A package.

LCD DUPLEX DRIVER

GENERAL DESCRIPTION

The PCF2111 is a single chip, silicon gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 64 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- 64 LCD-segment drive capability
- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possiblity

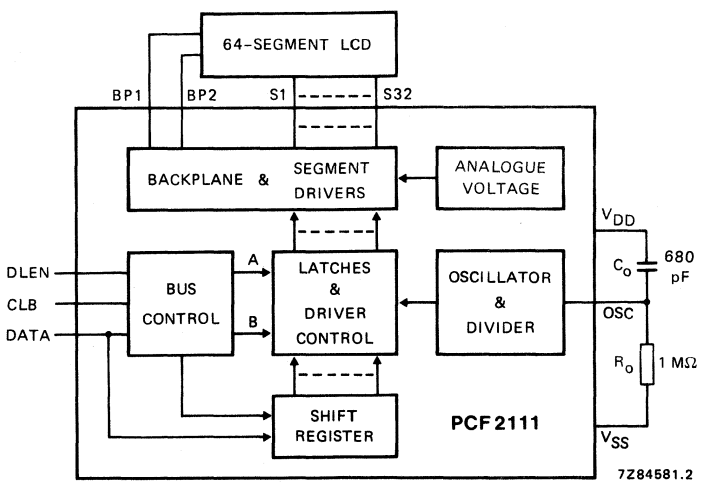


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF2111P: 40-lead DIL; plastic (SOT-129).
PCF2111T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{DD}		−0,3 to 8 V
Voltage on any pin	V_n	V_{SS}	−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}		−40 to + 85 °C
Storage temperature range	T_{stg}		−55 to + 125 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,25 to 6,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; R_o = 1 MΩ; C_o = 680 pF; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply current	no external load	I_{DD}	—	10	50	μA
Supply current	no external load; T_{amb} = −25 to + 85 °C	I_{DD}	—	—	30	μA
Display frequency	see Fig. 8; T = 680 μs	f_{LCD}	60	80	100	Hz
D.C. component of LCD drive	with respect to V_{SX}	V_{BP}	—	± 10	—	mV
Load on each segment driver			—	—	10	MΩ
			—	—	500	pF
Load on each backplane driver			—	—	1	MΩ
			—	—	5	nF
Input voltage HIGH	see Fig. 9	V_{IH}	2	—	—	V
Input voltage LOW	see Fig. 9	V_{IL}	—	—	0,6	V
Rise time V_{BP} to V_{SX}	max. load	t_r	—	20	—	μs
Inputs CLB, DATA, DLEN	see note on next page					
Input capacitance	for SOT-129 package	C_{IN}	—	—	10	pF
	for SOT-158A package	C_{IN}	—	—	5	pF
Rise and fall times	see Fig. 2	t_r, t_f	—	—	10	μs
CLB pulse width HIGH	see Fig. 2	t_{WH}	1	—	—	μs
CLB pulse width LOW	see Fig. 2	t_{WL}	9	—	—	μs

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Data set-up time DATA → CLB	see Fig. 2	t_{SUDA}	8	–	–	μs
Data hold time DATA → CLB	see Fig. 2	t_{HDDA}	8	–	–	μs
Enable set-up time DLEN → CLB	see Fig. 2	t_{SUEN}	1	–	–	μs
Disable set-up time CLB → DLEN	see Fig. 2	t_{SUDI}	8	–	–	μs
Set-up time (load pulse) DLEN → CLB	see Fig. 2	t_{SULD}	8	–	–	μs
Busy-time from load pulse to next start of transmission	see Fig. 2	t_{BUSY}	8	–	–	μs
Set-up time (leading zero) DATA → CLB	see Fig. 2	t_{SULZ}	8	–	–	μs

Note

All timing values are referred to $V_{IH\ min}$ and $V_{IL\ max}$* (see Fig. 2). If external resistors are used in the bus lines (see Fig. 9), the extra time constant has to be added.

* With an input voltage swing of $V_{IL\ max}$–0,1 V to V_{IHmin} + 0,1 V.

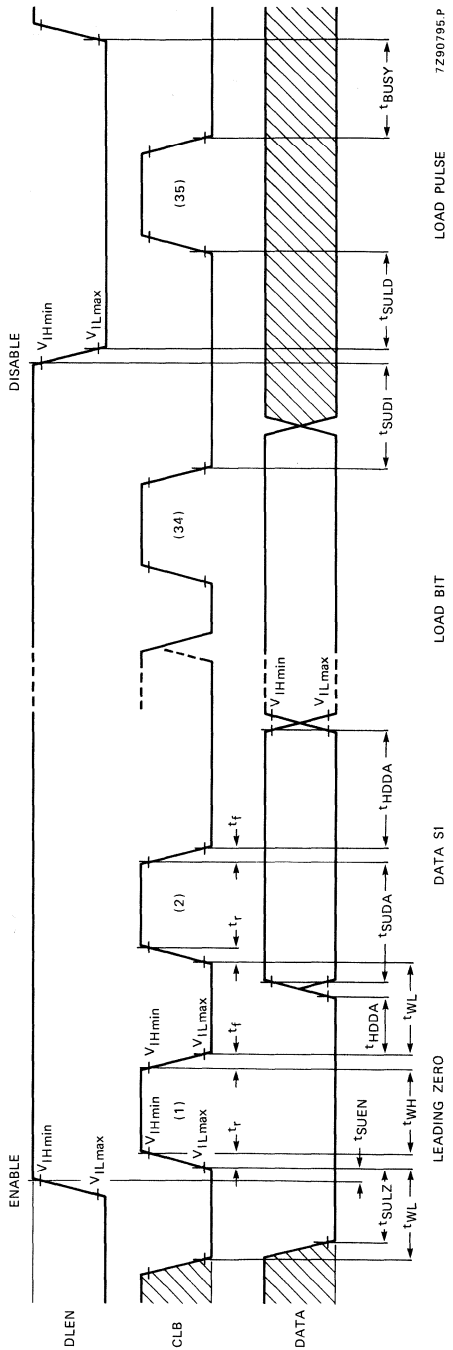


Fig. 2 CBUS timing.

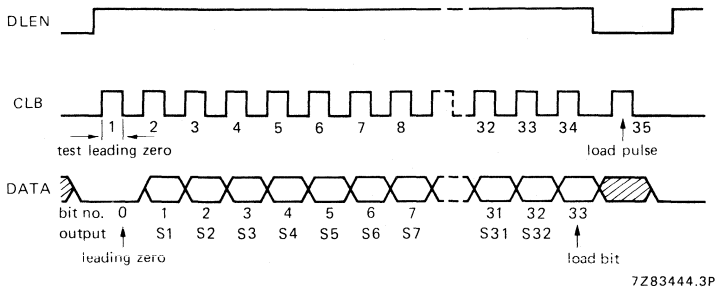


Fig. 3 CBUS data format.

Notes to Fig. 3

An LCD segment is activated when the corresponding DATA-bit is HIGH.
When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from shift register to selected latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN is LOW) and the driver is ready to receive new data.

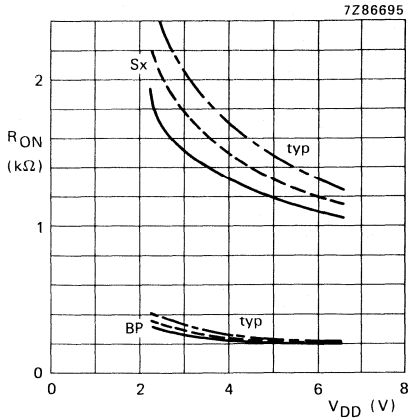


Fig. 4 Output resistance of backplane and segments.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

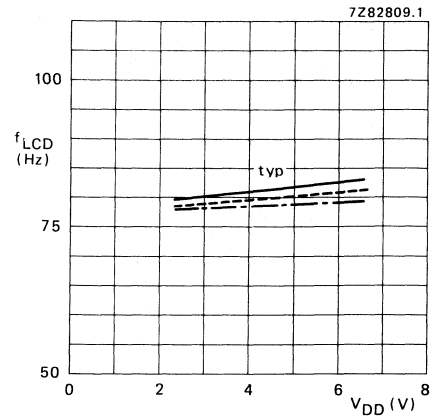


Fig. 5 Display frequency as a function of supply voltage; R_oC_o = 680 μs.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

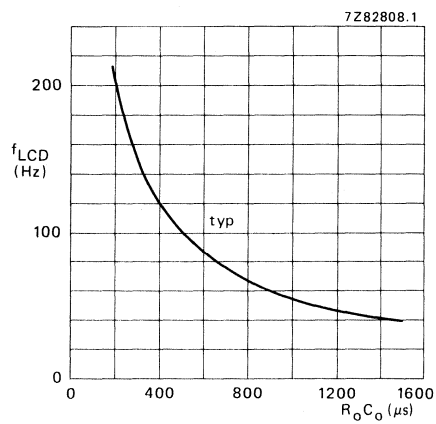


Fig. 6 Display frequency as a function of R_o x C_o time; T_{amb} = 25 °C.

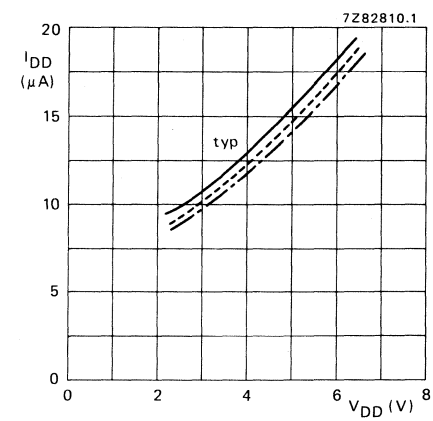


Fig. 7 Supply current as a function of supply voltage.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

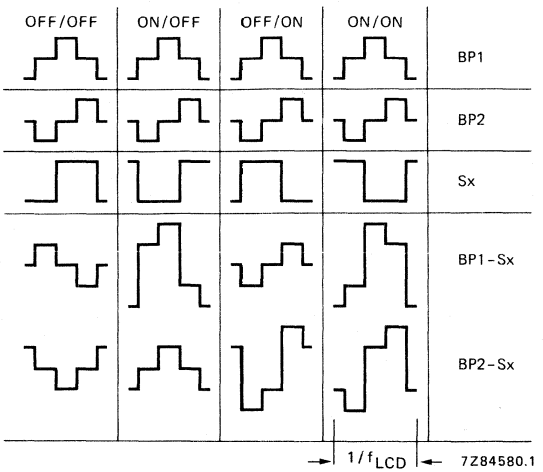


Fig. 8 Timing diagram.

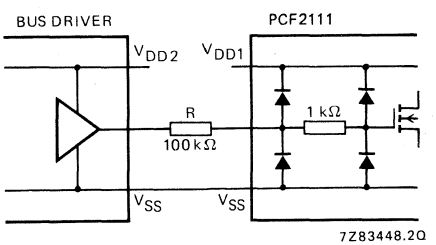
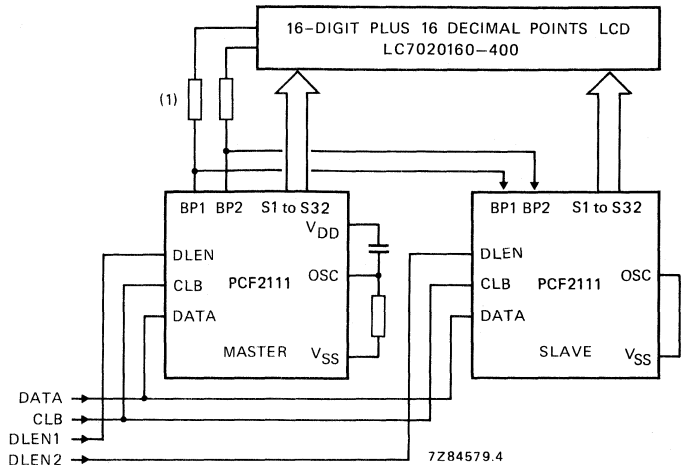


Fig. 9 Input circuitry.

Note to Fig. 9

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1}$ + 0,5 V, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current $\leq$ 40 μA.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2111 and the backplane of the LCD must be $> 2{,}7\ k\Omega$. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 10 Diagram showing expansion possibility for a 16-digit plus 16 decimal points LCD.

Note to Fig. 10

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2111, PCF2110 and PCF2100 ICs up to the BP drive capability of the master.

PCF2100 is a 40 LCD-segment driver; PCF2110 is a 60 LCD-segment driver plus 2 LED driver outputs.

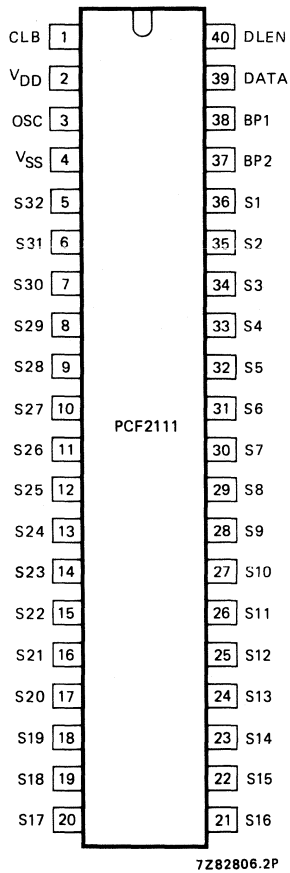


Fig. 11 Pinning diagram.

PINNING

Supply

2	V_{DD}	Positive supply
4	V_{SS}	Negative supply

Inputs

3	OSC	Oscillator input	
39	DATA	Data line	CBUS
40	DLEN	Data line enable	CBUS
1	CLB	Clock burst	CBUS

Outputs

38	BP1	Backplane drivers (common of LCD)
37	BP2	Backplane drivers (common of LCD)
S1 to S32		LCD driver outputs

LCD DRIVER

GENERAL DESCRIPTION

The PCF2112 is a single chip, silicon gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 32 segments in direct drive; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- 32 LCD-segment drive capability.
- Supply voltage 2,25 to 6,5 V.
- Low current consumption.
- Serial data input.
- CBUS control.
- One-point built-in oscillator.
- Expansion possibility.

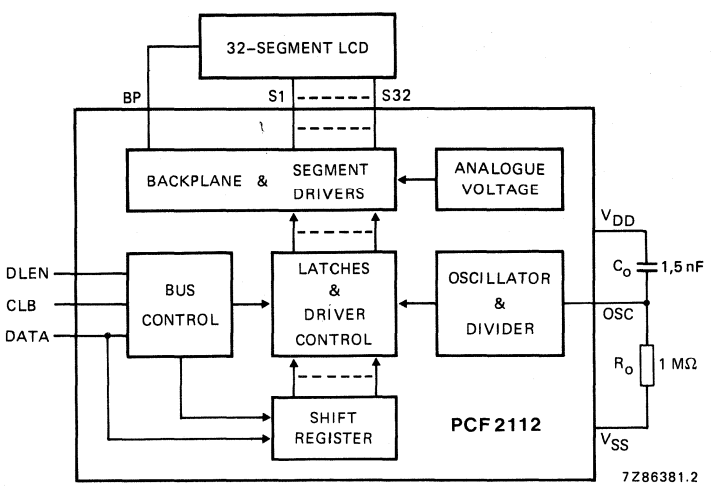


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF2112P : 40-lead DIL; plastic (SOT-129).
PCF2112T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{DD}	−0,3 to 8	V
Voltage on any pin	V_n	V_{SS}−0,3 to V_{DD} + 0,3	V
Operating ambient temperature range	T_{amb}	−40 to + 85	°C
Storage temperature range	T_{stg}	−55 to + 125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,25 to 6,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; R_o = 1 MΩ; C_o = 1,5 nF; unless otherwise specified.

parameter	condition	symbol	min.	typ.	max.	unit
Supply current	no external load	I_{DD}	–	10	50	μA
Supply current	no external load; T_{amb} = −25 to +85 °C	I_{DD}	–	–	30	μA
Display frequency	T = 1,5 ms	f_{LCD}	30	40	50	Hz
Output resistance of each segment	I_o = 10 μA	R_S	–	–	10	kΩ
Output resistance of backplane	I_o = 10 μA	R_{BP}	–	–	2	kΩ
Input voltage HIGH	see Fig. 8	V_{IH}	2	–	–	V
Input voltage LOW	see Fig. 8	V_{IL}	–	–	0,6	V
Inputs CLB,DATA,DLEN	see note on next page					
Input capacitance	for SOT-129 package	C_{IN}	–	–	10	pF
	for SOT-158A package	C_{IN}	–	–	5	pF
Rise and fall times	see Fig. 2	t_r, t_f	–	–	10	μs
CLB pulse width HIGH	see Fig. 2	t_{WH}	1	–	–	μs
CLB pulse width LOW	see Fig. 2	t_{WL}	9	–	–	μs

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Data set-up time DATA → CLB	see Fig. 2	t_{SUDA}	8	–	–	μs
Data hold time DATA → CLB	see Fig. 2	t_{HDDA}	8	–	–	μs
Enable set-up time DLEN → CLB	see Fig. 2	t_{SUEN}	1	–	–	μs
Disable set-up time CLB → DLEN	see Fig. 2	t_{SUDI}	8	–	–	μs
Set-up time (load pulse) DLEN → CLB	see Fig. 2	t_{SULD}	8	–	–	μs
Busy-time from load pulse to next start of transmission	see Fig. 2	t_{BUSY}	8	–	–	μs
Set-up time (leading zero) DATA → CLB	see Fig. 2	t_{SULZ}	8	–	–	μs

Note

All timing values are referred to V_{IHmin} and V_{ILmax}*(see Fig. 2). If external resistors are used in the bus lines (see Fig. 8), an extra time constant has to be added.

* With an input voltage swing of V_{ILmax}–0,1 V to V_{IHmin} + 0,1 V.

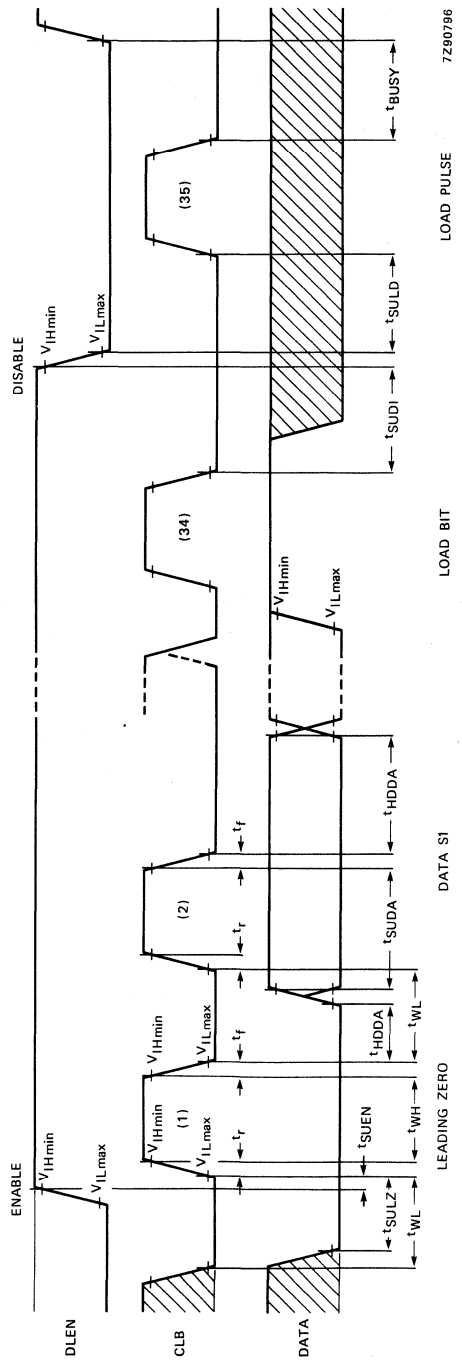


Fig. 2 CBUS timing.

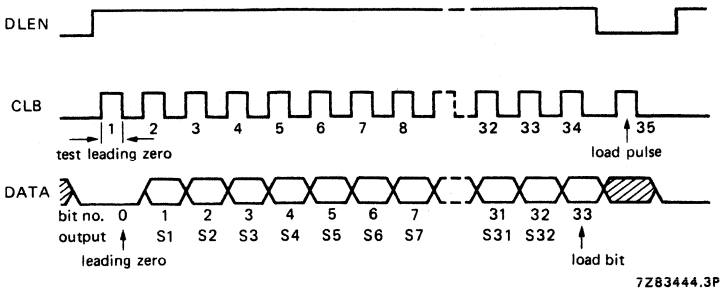


Fig. 3 Data format.

Notes to Fig. 3

An LCD segment is activated when the corresponding DATA-bit is HIGH.
When DATA-bit 33 is HIGH, the latches are loaded. CLB-pulse 35 transfers data from shift register to latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN is LOW) and the driver is ready to receive new data.

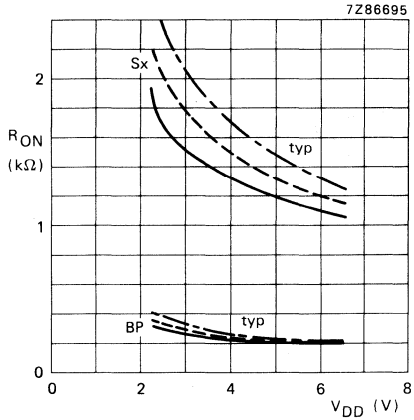


Fig. 4 Output resistance of backplane and segments.
——— T_{amb} = −40 °C; – – – T_{amb} = + 25 °C; – · – T_{amb} = + 85 °C.

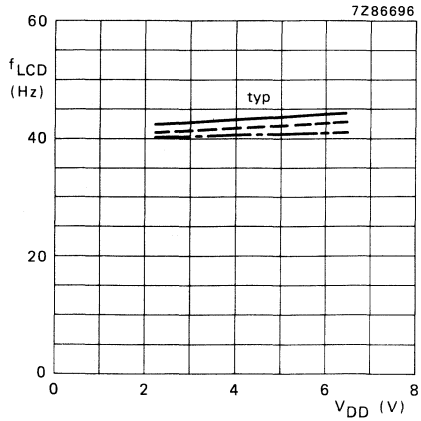


Fig. 5 Display frequency as a function of supply voltage; R_oC_o = 1,5 ms.
——— T_{amb} = −40 °C; – – – T_{amb} = + 25 °C; – · – T_{amb} = + 85 °C.

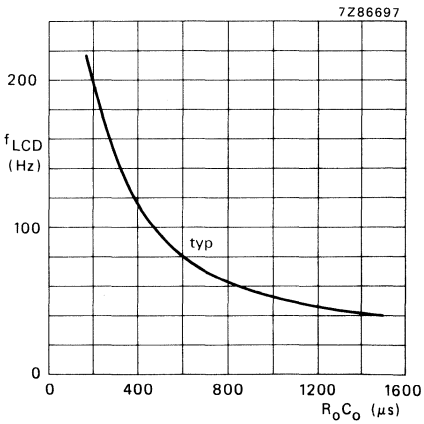


Fig. 6 Display frequency as a function of R_o x C_o time; T_{amb} = 25 °C.

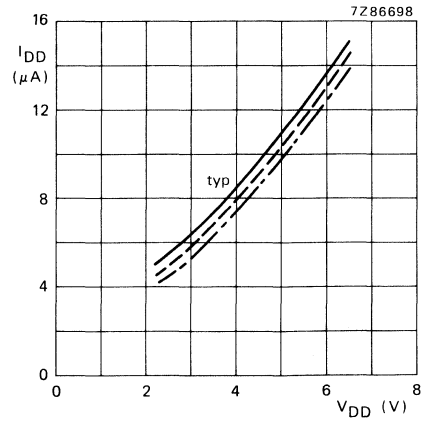


Fig. 7 Supply current as a function of supply voltage.
——— T_{amb} = −40 °C; – – – T_{amb} = + 25 °C; – · – T_{amb} = + 85 °C.

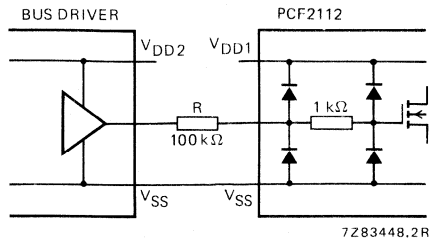
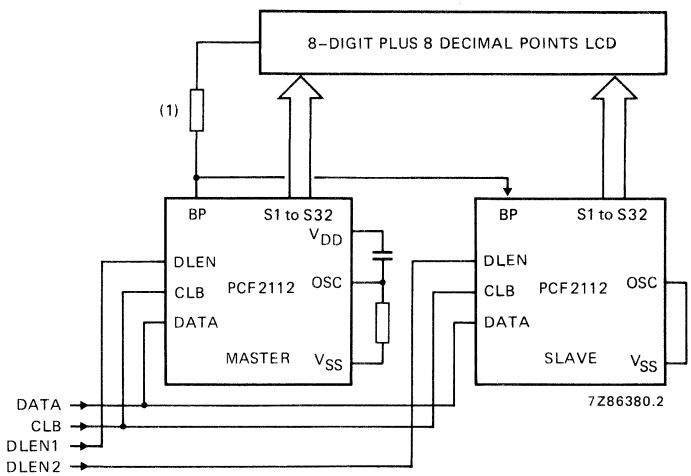


Fig. 8 Input circuitry.

Note to Fig. 8

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current $\leqslant 40\ \mu A$.



(1) In the slave mode, the serial resistor between BP of the PCF2112 and the backplane of the LCD must be $> 2{,}7$ kΩ. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 9 Diagram showing expansion possibility for an 8-digit plus 8 decimal points LCD.

Note to Fig. 9

By connecting OSC to V_{SS} the BP-pin becomes input and generates signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2112 ICs up to the BP drive capability of the master.

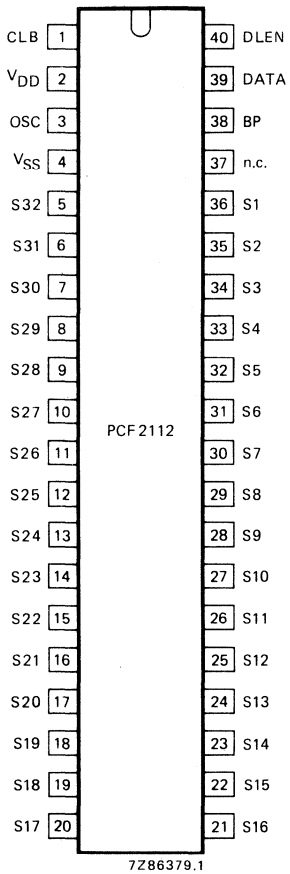


Fig. 10 Pinning diagram.

PINNING

Supply

2	V_{DD}	Positive supply
4	V_{SS}	Negative supply

Inputs

3	OSC	Oscillator input	
39	DATA	Data line	CBUS
40	DLEN	Data line enable	CBUS
1	CLB	Clock burst	CBUS

Outputs

38	BP	Back plane driver (common of LCD)
S1 to S32		LCD driver outputs
37	n.c.	not connected

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The PCF84CXX family of microcontrollers is manufactured in CMOS technology. The family consists of the following devices:

- PCF84C00 – 256 RAM bytes, external program memory
- PCF84C20 – 2 K ROM/64 RAM bytes
- PCF84C40 – 4 K ROM/128 RAM bytes

I/O port lines, one serial I/O line, one single-level vectored interrupt, an 8-bit timer event counter and on-board clock oscillator and clock circuits.

This microcontroller family is an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048 and is pin- and instruction set compatible with the MAB8400 family. The microcontrollers have extensive bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the "User manual Single-chip microcomputer".

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 2 K or 4 K ROM bytes plus a ROM-less version
- 64 or 128 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O which can be used in single or multi-master systems (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V
- STOP and IDLE mode
- Power-on-reset circuit and low supply voltage detection
- Operating temperature range: −40 to + 85 °C

PACKAGE OUTLINES

PCF84C20/40P : 28-lead DIL; plastic (SOT-117D).
PCF84C20/40D : 28-lead DIL; ceramic (CERDIP) (SOT-135A).
PCF84C20/40T : 28-lead mini-pack; plastic (SO-28; SOT-136A).
PCF84C00B : 28-lead 'Piggy-back' package (with up to 28-pin EPROM on top).
PCF84C00WP : 68-lead plastic leaded chip-carrier (PLCC) (SOT-188A).
PCF84C00T : 56-lead mini-pack; plastic (VSO-56; SOT-190).

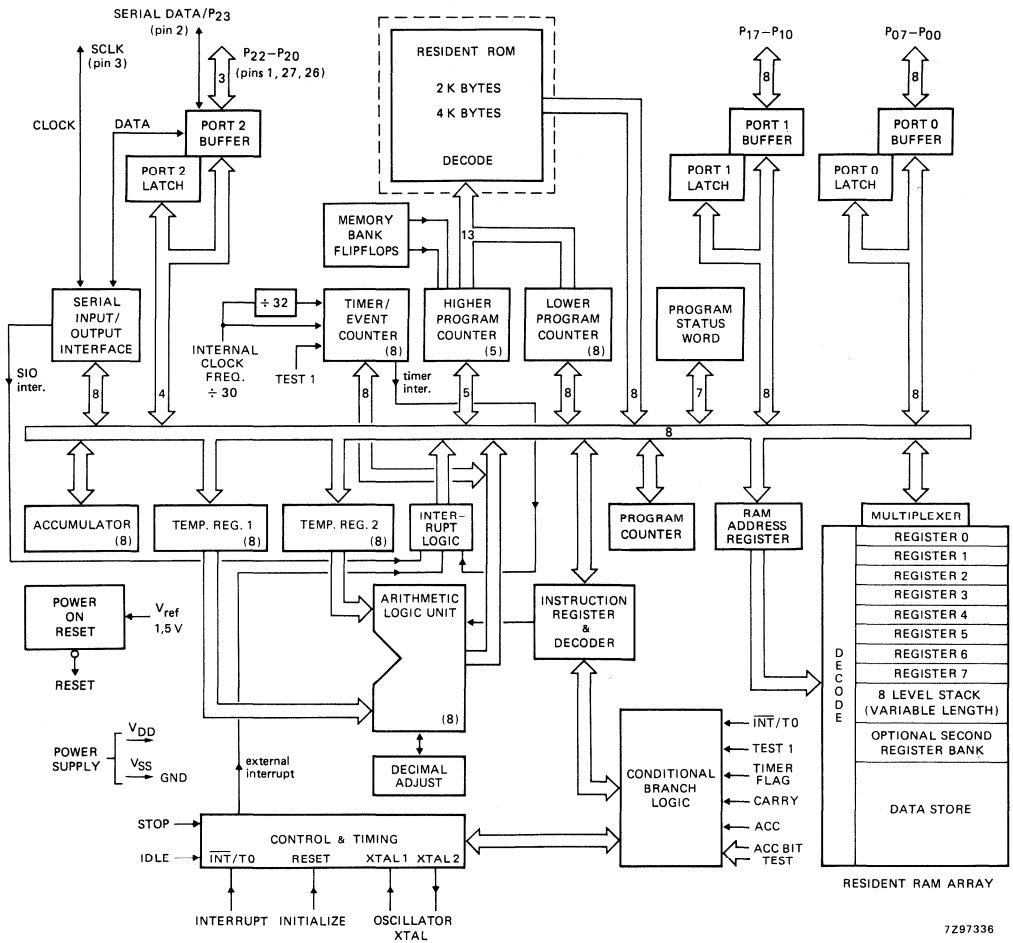
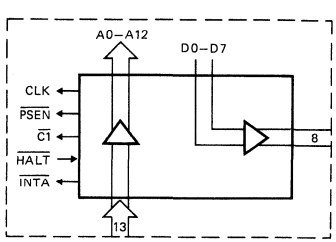
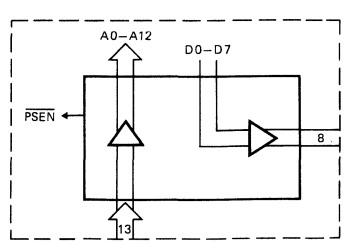


Fig. 1 Block diagram; PCF84CXX.



(a)

Fig. 1a Replacement of dotted part in Fig. 1, for the PCF8400WP bond-out version.



(b)

Fig. 1b Replacement of dotted part in Fig. 1, for the PCF84C00B 'Piggy-back' version.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The PCF84C12 microcontroller is manufactured in CMOS technology.
It has 13 quasi-bidirectional I/O port lines, one single-level vectored interrupt, an 8-bit timer event counter and on-board clock oscillator and clock circuits.

This microcontroller is an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048 and is pin- and instruction set compatible with the MAB8400 family. The PCF84C12 has extensive bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the "User manual Single-chip microcomputer"

Features

- 8-bit CPU, ROM, RAM, I/O in a single 20-lead DIL or SO package
- 1 K ROM bytes
- 64 RAM bytes
- 13 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external and timer/event counter
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V
- STOP and IDLE mode
- Power-on-reset circuit and low supply voltage detection
- Operating temperature range: −40 to + 85 °C

PACKAGE OUTLINES

PCF84C12P: 20-lead DIL; plastic (SOT-146).
PCF84C12T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

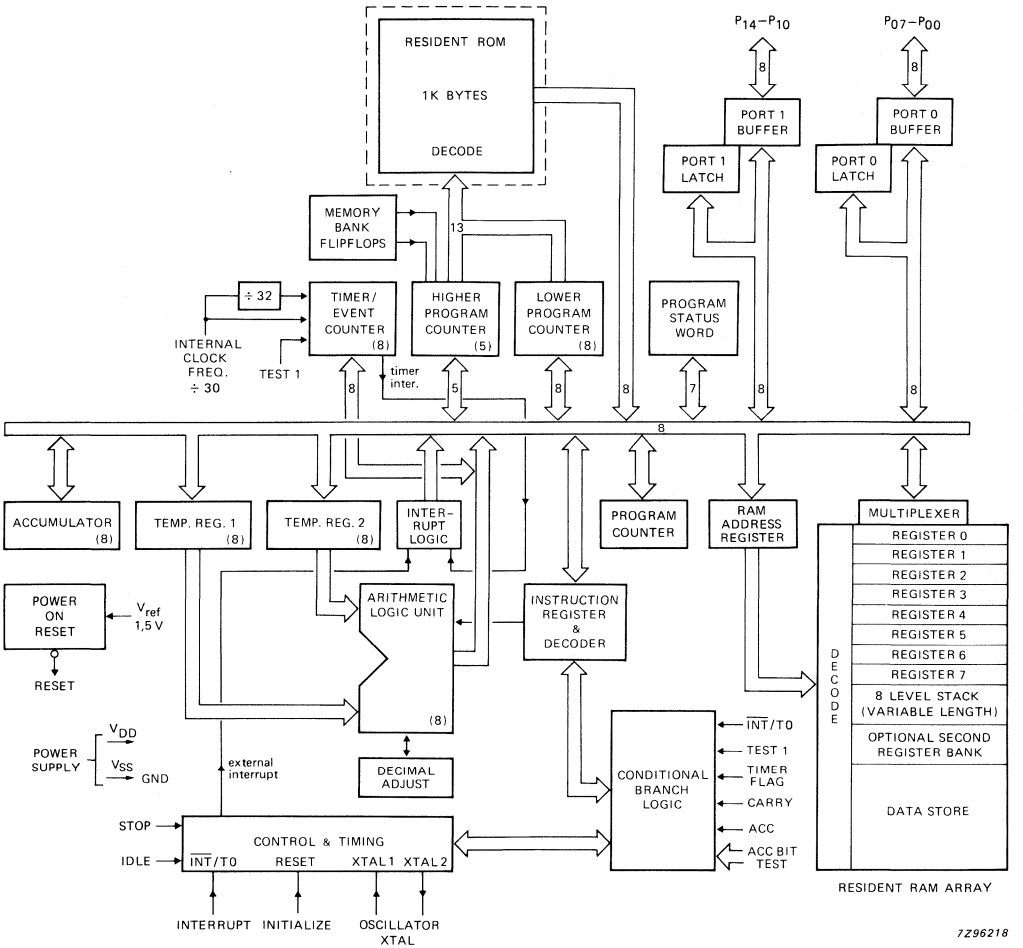


Fig. 1 Block diagram.

256 x 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8570 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1, A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I^2C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony
- Radio and television
- Video cassette recorder
- General purpose

RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
channel presets

RAM expansion for the microcontroller families MAB8400 and PCF84C00

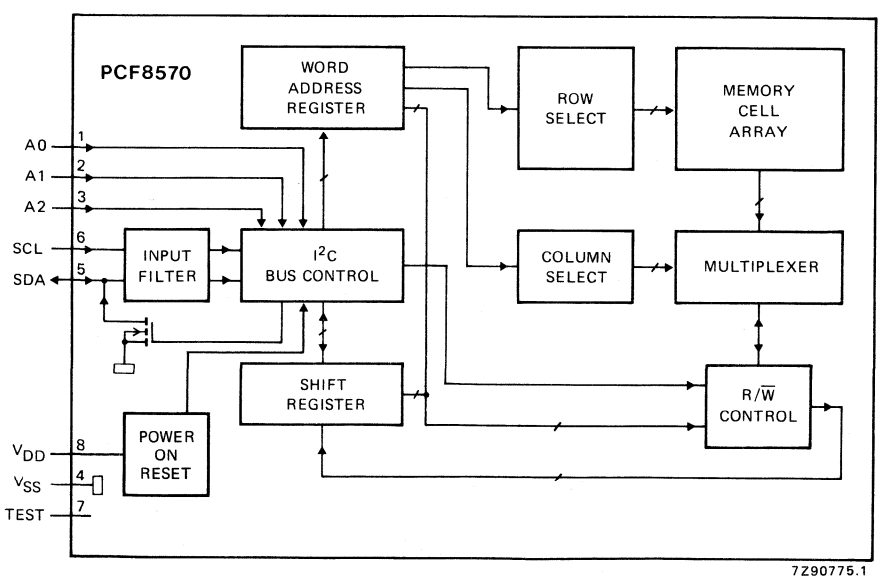


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8570P: 8-lead DIL; plastic (SOT-97A).
PCF8570T: 8-lead mini-pack plastic (SO-8L; SOT-176).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line (I²C bus)
6	SCL	serial clock line (I²C bus)
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 14 and 15)
8	V_{DD}	positive supply

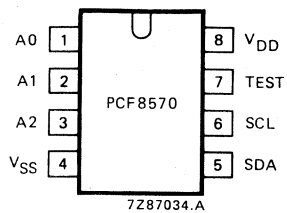


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}		−0,8 to + 8,0	V
Voltage range on any input	V_I		−0,8 to V_{DD} + 0,8	V
D.C. input current (any input)	$\pm I_I$	max.	10	mA
D.C. output current (any output)	$\pm I_O$	max.	10	mA
Supply current (pin 4 or pin 8)	$\pm I_{DD}$; I_{SS}	max.	50	mA
Power dissipation per package	P_{tot}	max.	300	mW
Power dissipation per output	P	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−40 to + 85	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current at $V_I = V_{SS}$ or V_{DD}					
operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
standby at f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
standby at T_{amb} = −25 to + 70 °C	I_{DDO}	–	–	5	μA
Power-on reset voltage level*	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = −25 to + 70 °C	I_{DDR}	–	–	2	μA
Power saving mode (Figs 14 and 15)					
Supply current at T_{amb} = 25 °C; TEST = V_{DDR}	I_{DDR}	–	50	400	nA

* The power-on reset circuit resets the I^2C bus logic when $V_{DD} < V_{POR}$.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0,5 mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

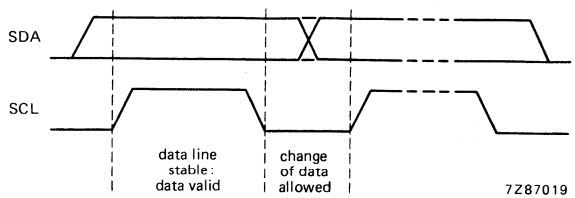


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

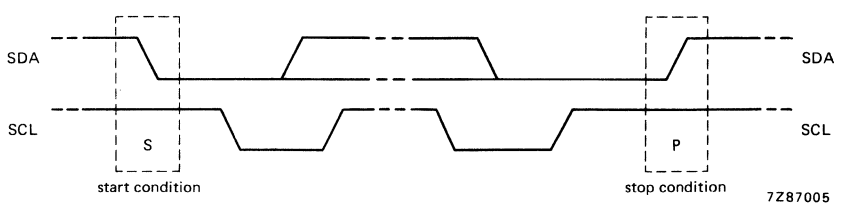


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

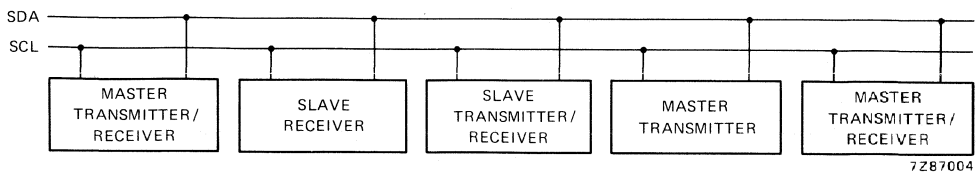


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

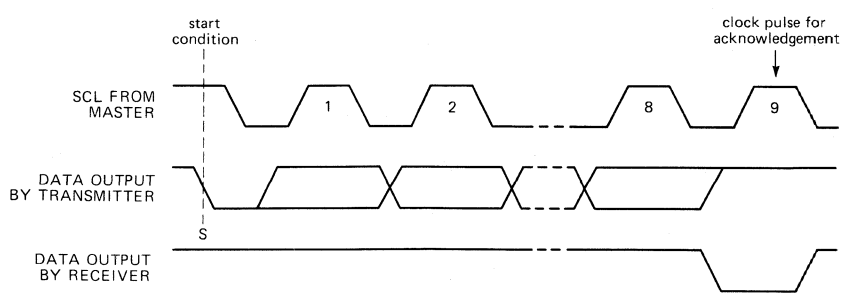


Fig. 6 Acknowledgement on the I^2C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The device operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

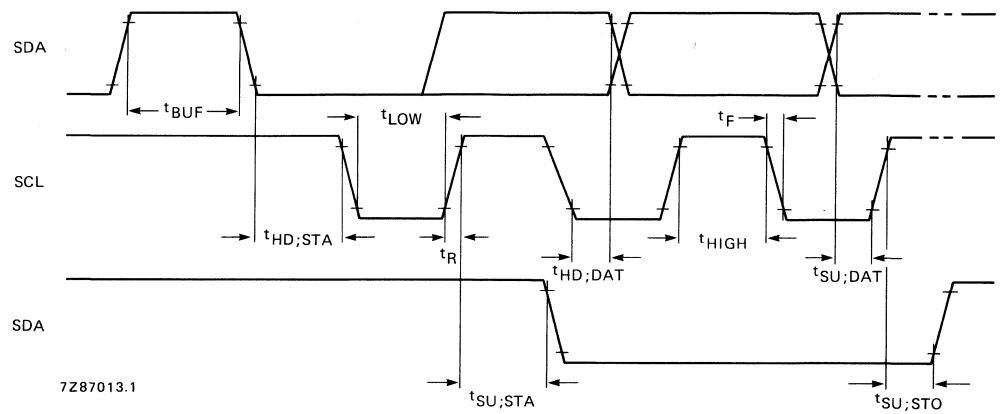


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

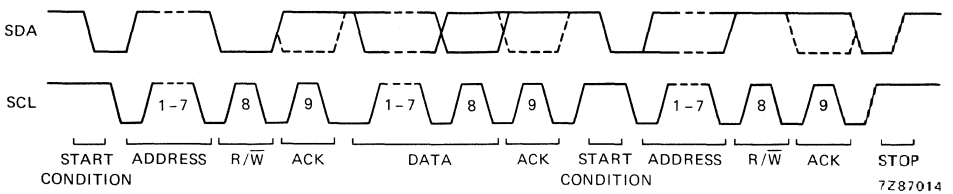


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

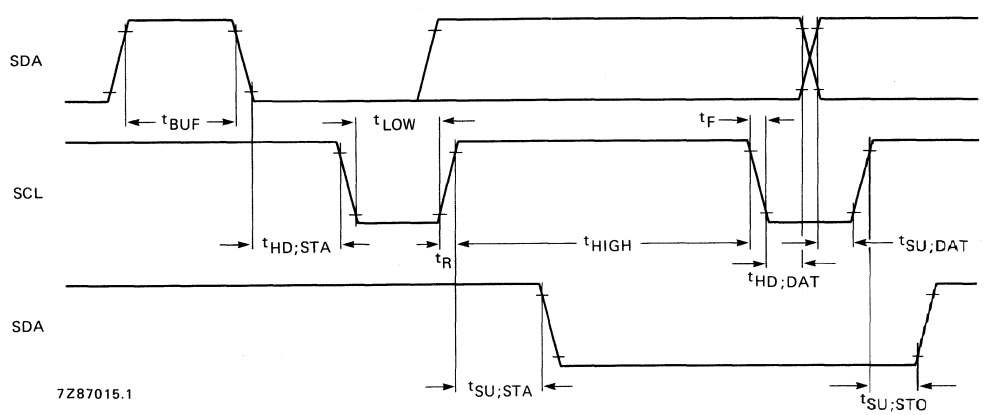


Fig. 9 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

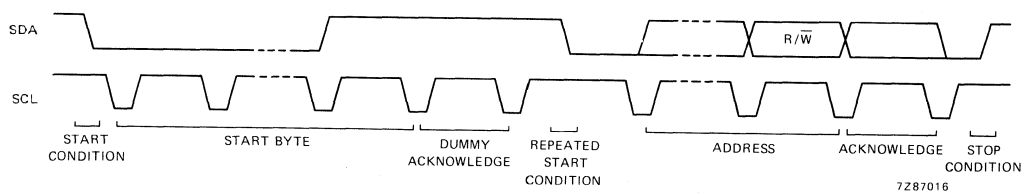


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8570 READ and WRITE cycles is shown in Fig. 11.

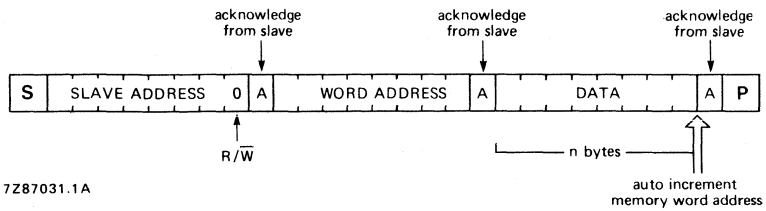


Fig. 11(a) Master transmits to slave receiver (WRITE mode).

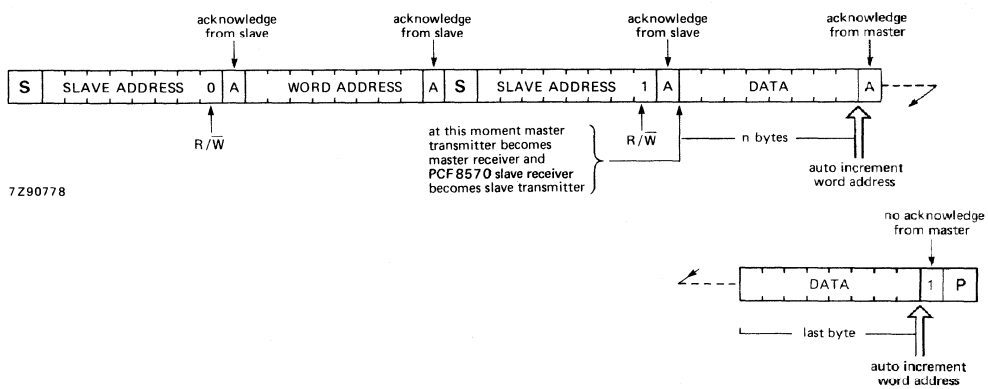


Fig. 11(b) Master reads after setting word address (WRITE word address; READ data).

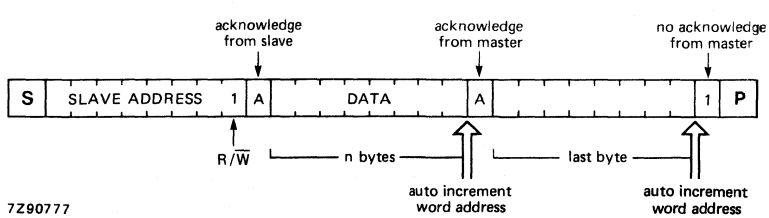


Fig. 11(c) Master reads slave immediately after first byte (READ mode).

APPLICATION INFORMATION

The PCF8570 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

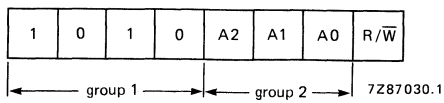


Fig. 12 PCF8570 address.

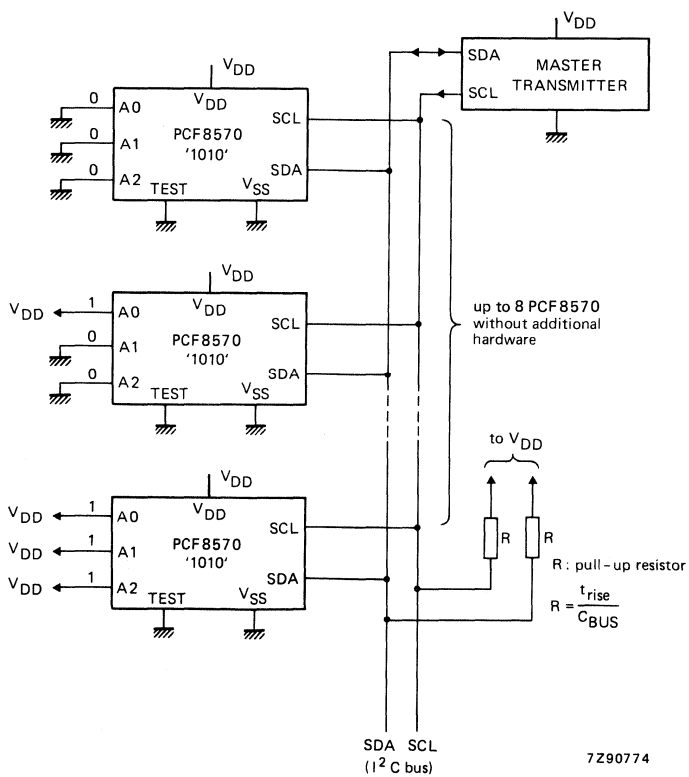


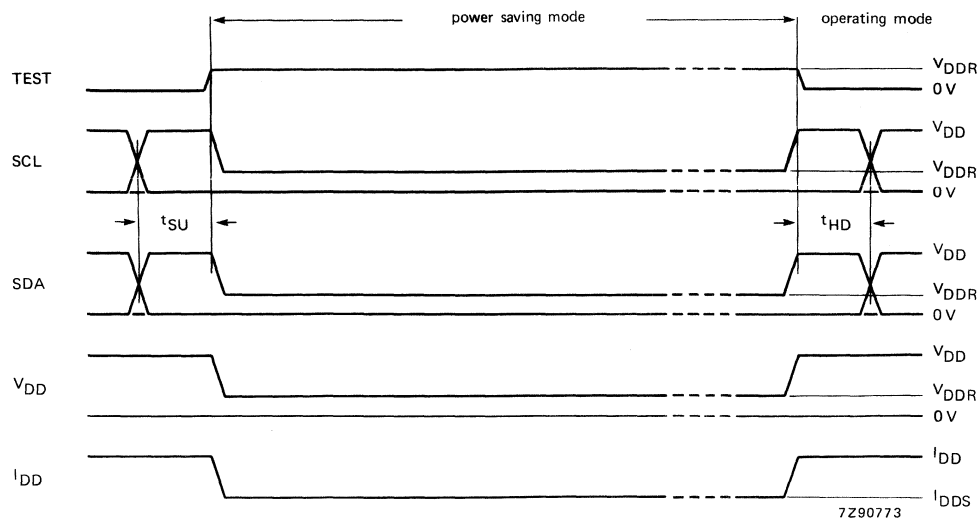
Fig. 13 PCF8570 application diagram.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

POWER SAVING MODE

With the condition TEST = V_{DDR}, the PCF8570 goes into the power saving mode and the I^2C bus logic is reset.



Where:
$t_{SU} \geqslant 4\ \mu s$
$t_{HD} \geqslant 4\ \mu s$

Fig. 14 Timing for power saving mode.

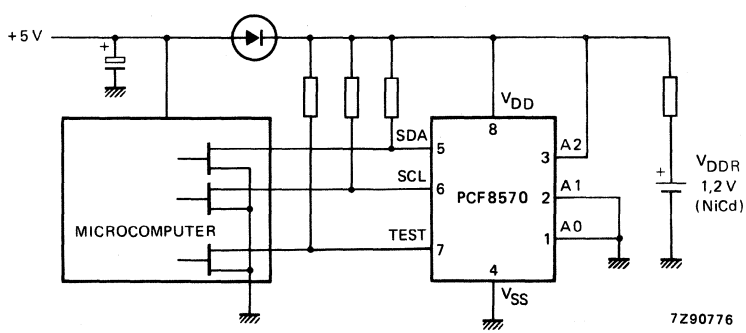
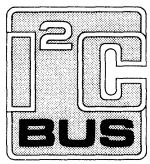


Fig. 15 Application example for power saving mode.

Note to Fig. 15

1. In the operating mode, TEST = 0.
2. In the power saving mode, TEST = V_{DDR}.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specification defined by Philips.

128 x 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8571 is a low power 1024-bit static CMOS RAM organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1, A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 5 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I^2C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony
- Radio and television
- Video cassette recorder
- General purpose

RAM expansion for stored numbers in repertory dialling (e.g. PCD3340 applications)
channel presets

RAM expansion for the microcomputer families MAB8400 and PCF84C00

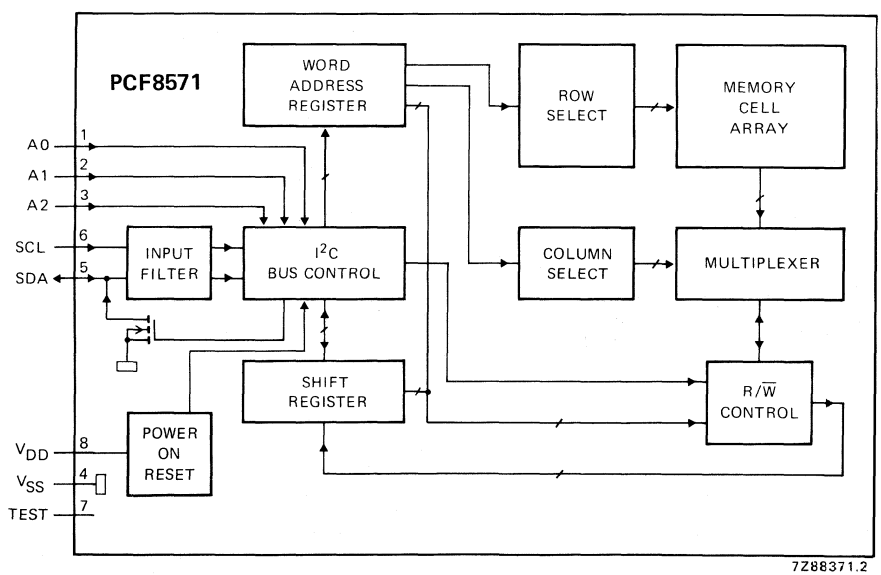


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8571P : 8-lead DIL; plastic (SOT-97A).
PCF8571T : 8-lead mini-pack (SO-8L; SOT-176).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line (I²C bus)
6	SCL	serial clock line (I²C bus)
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Fig. 14 and 15)
8	V_{DD}	positive supply

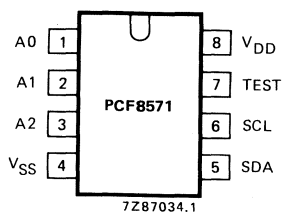


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}		−0,8 to + 8,0 V
Voltage range on any input	V_I		−0,8 to V_{DD} + 0,8 V
D.C. input current (any input)	$\pm I_I$	max.	10 mA
D.C. output current (any output)	$\pm I_O$	max.	10 mA
Supply current (pin 4 or pin 8)	$\pm I_{DD}; I_{SS}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	50 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating temperature range	T_{amb}		−40 to + 85 °C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current					
$V_I = V_{SS}$ or V_{DD}					
operating at f_{SCL} = 100 kHz;	I_{DD}	–	–	200	μA
standby at f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
standby at T_{amb} = −25 to 70 °C	I_{DDO}	–	–	5	μA
Power-on reset voltage level					
at $V_{SCL} = V_{SDA} = V_{DD}$	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW					
at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH					
at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
Input leakage current					
at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA)					
at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V;					
T_{amb} = −25 to 70 °C	I_{DDR}	–	–	2	μA
Power saving mode (Fig. 14)					
Supply current at T_{amb} = 25 °C;					
TEST = V_{DDR}	I_{DDS}	–	50	200	nA

* The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0,5 mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

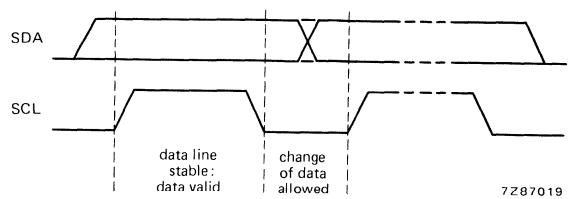


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

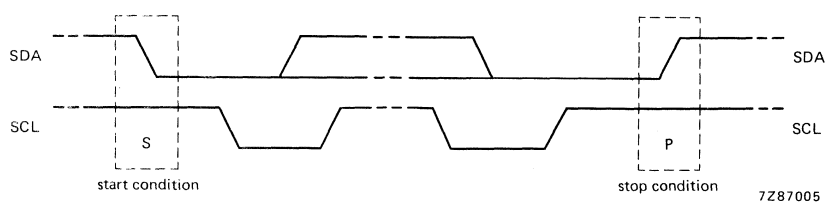


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

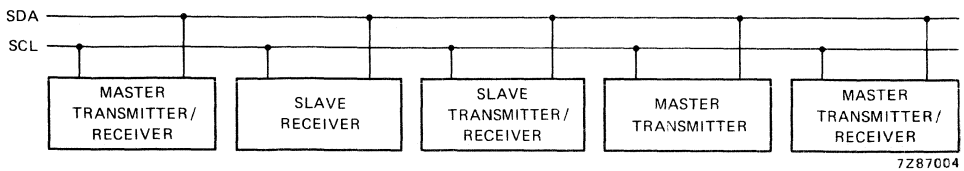


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

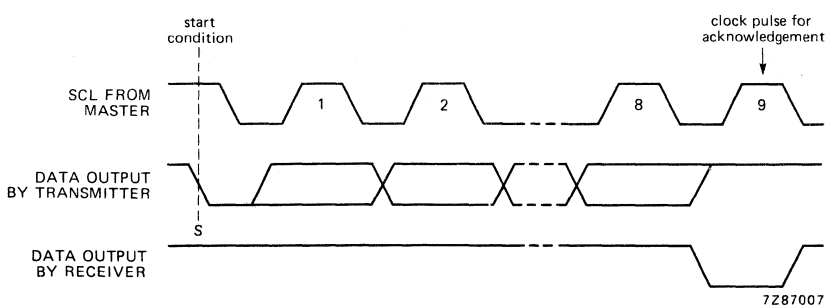


Fig. 6 Acknowledgement on the I^2C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8571 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

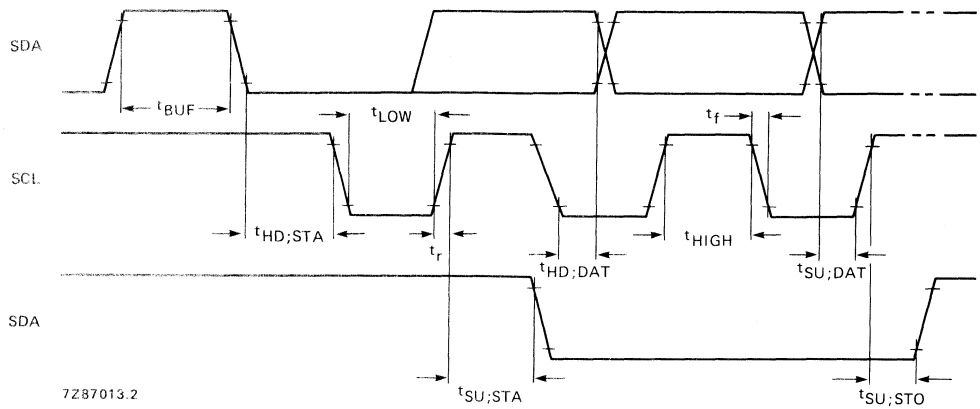


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

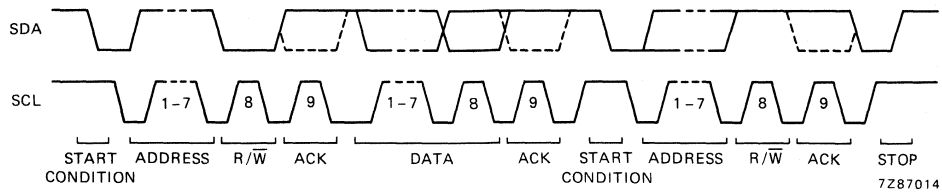


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

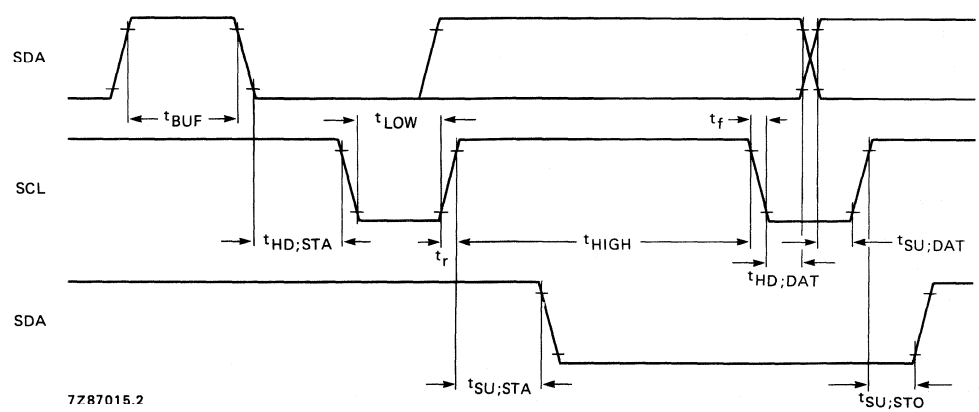


Fig. 9 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_r	$t \leqslant 1\ \mu s$
t_f	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

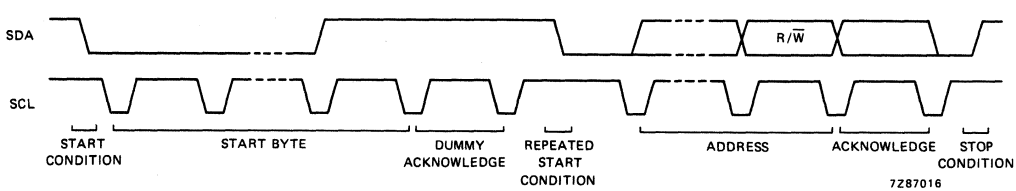


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8571 READ and WRITE cycles is shown in Fig. 11.

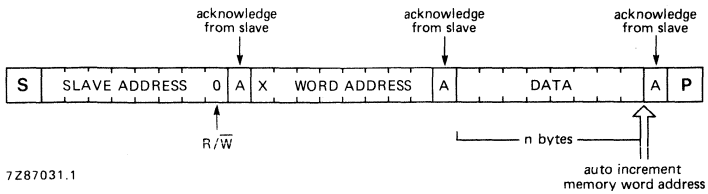


Fig. 11(a) Master transmits to slave receiver (WRITE mode).

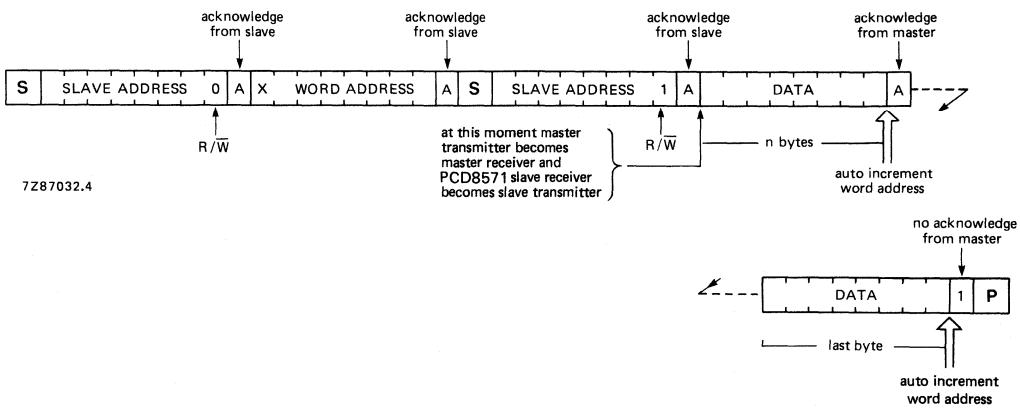


Fig. 11(b) Master reads after setting word address (WRITE word address; READ data).

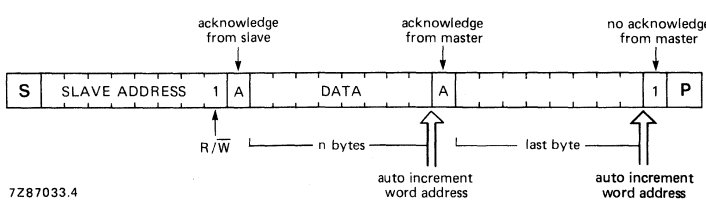


Fig. 11(c) Master reads slave immediately after first byte (READ mode).

Note

X = don't care bit.

APPLICATION INFORMATION

The PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

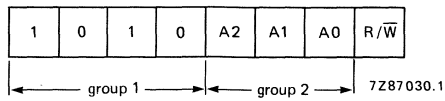


Fig. 12 PCF8571 address.

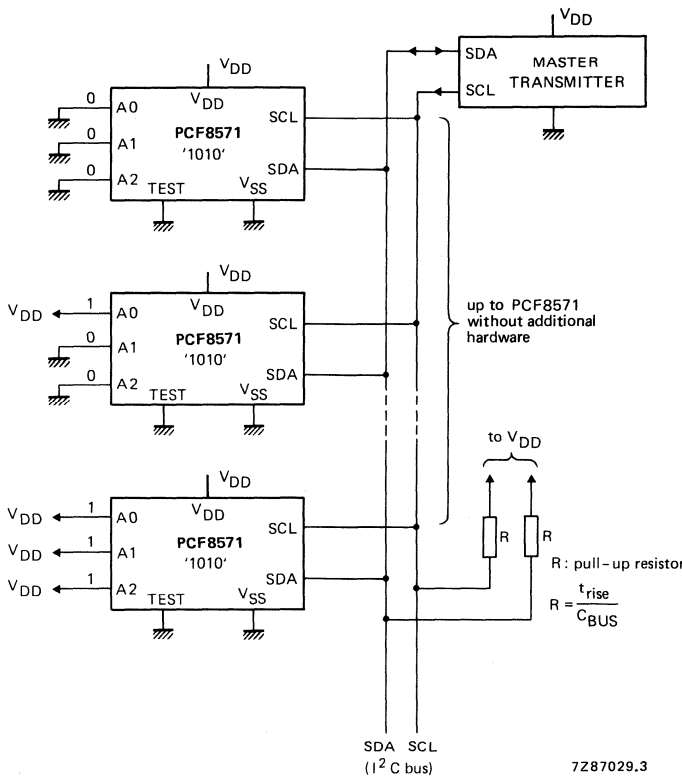


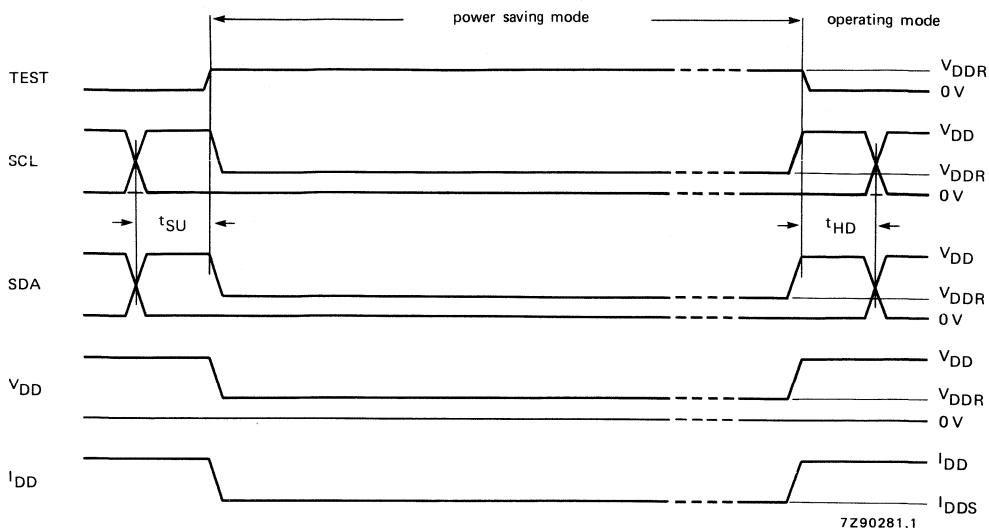
Fig. 13 PCF8571 application diagram.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

POWER SAVING MODE

With the condition TEST = V_{DDR}, the PCF8571 goes into the power saving mode and I^2C bus logic is reset.



Where:
$t_{SU} \geqslant 4\ \mu s$
$t_{HD} \geqslant 4\ \mu s$

Fig. 14 Timing for power saving mode.

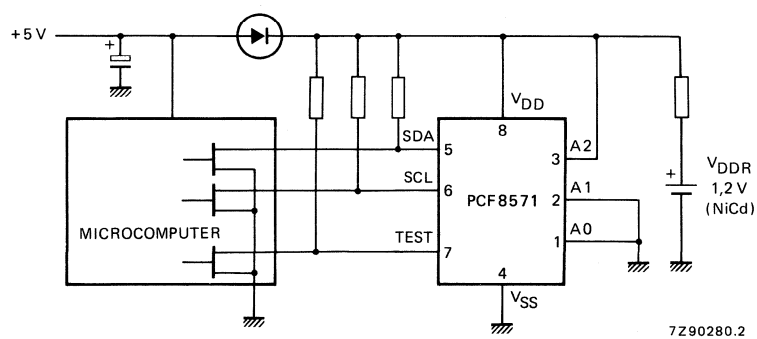
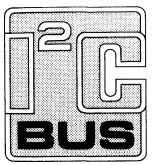


Fig. 15 Application example for power saving mode.

Note

1. In the operating mode, TEST = 0.
2. In the power saving mode, TEST = V_{DDR}.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS circuit that functions as a real time clock/calendar in the Inter IC (I^2C) bus-oriented microcomputer systems. The device includes an addressable time counter and an addressable alarm register, both for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred serially via a two line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1,2 V nickel cadmium battery. The time base is generated from a 32,768 kHz crystal-controlled oscillator.

Features

- Serial input/output bus (I^2C) interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32,768 kHz)

QUICK REFERENCE DATA

Supply voltage range (clock)	$V_{DD}-V_{SS1}$		1,1 to 6,0 V
Supply voltage range (I^2C interface)	$V_{DD}-V_{SS2}$		2,5 to 6,0 V
Crystal oscillator frequency	f_{osc}	typ.	32,768 kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT-38).
PCF8573T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

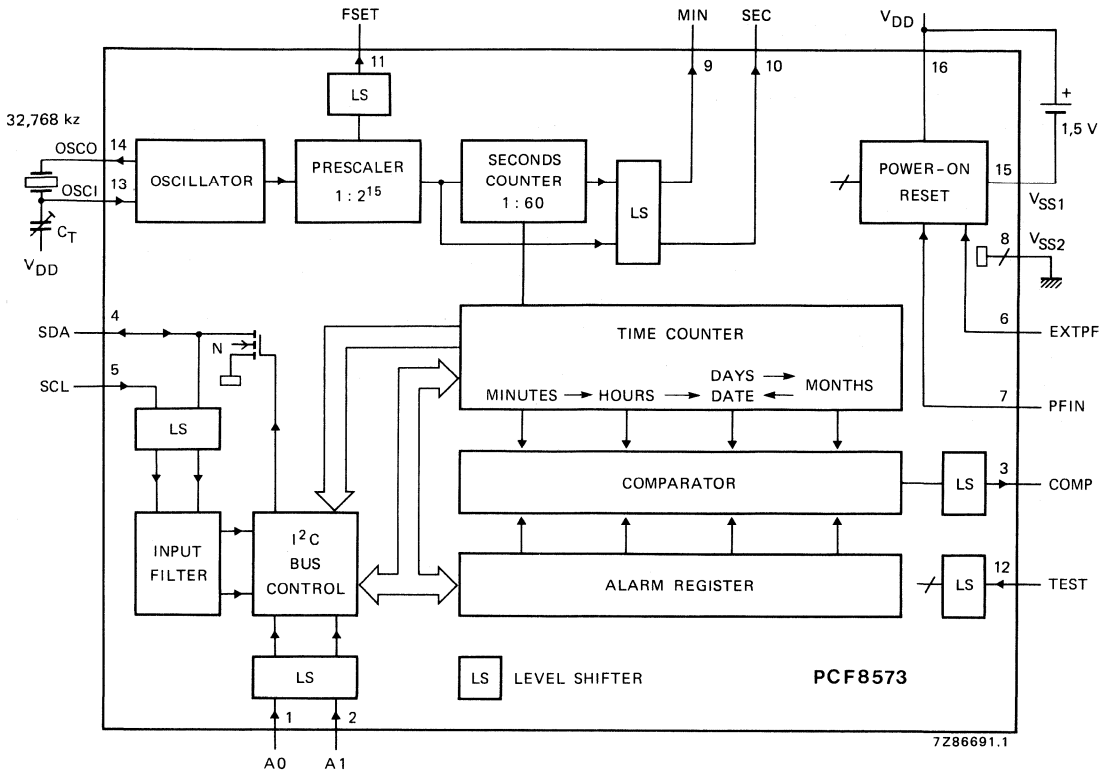


Fig. 1 Block diagram.

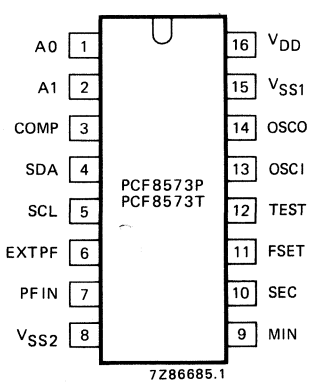


Fig. 2 Pinning diagram.

PINNING

1	A0	address input
2	A1	address input
3	COMP	comparator output
4	SDA	serial data line (I^2C bus)
5	SCL	serial clock line (I^2C bus)
6	EXTPF	enable power fail flag input
7	PFIN	power fail flag input
8	V_{SS2}	negative supply 2 (I^2C interface)
9	MIN	one pulse per minute output
10	SEC	one pulse per second output
11	FSET	oscillator tuning output
12	TEST	test input; must be connected to V_{SS2} when not in use
13	OSCI	oscillator input
14	OSCO	oscillator input/output
15	V_{SS1}	negative supply 1 (clock)
16	V_{DD}	common positive supply

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32,768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I^2C bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (see note)
			or 29 → 01	
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note: Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power on reset for the I^2C bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig. 3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

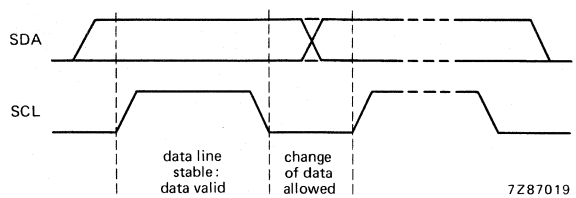


Fig. 3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

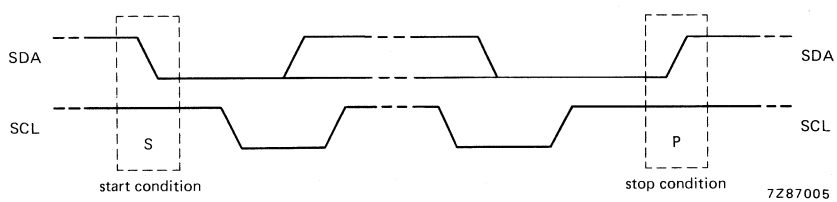


Fig. 4 Definition of start and stop conditions.

System configuration (see Fig. 5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

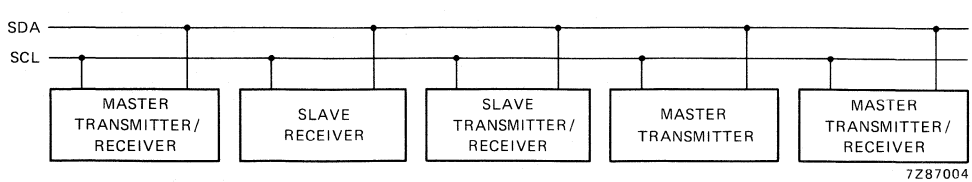


Fig. 5 System configuration.

CHARACTERISTICS OF THE I²C bus (continued)

Acknowledge (see Fig. 6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig. 13 and Fig. 14.)

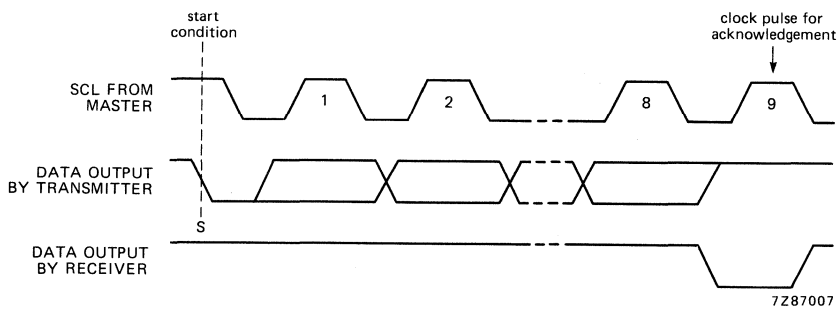


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8573 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

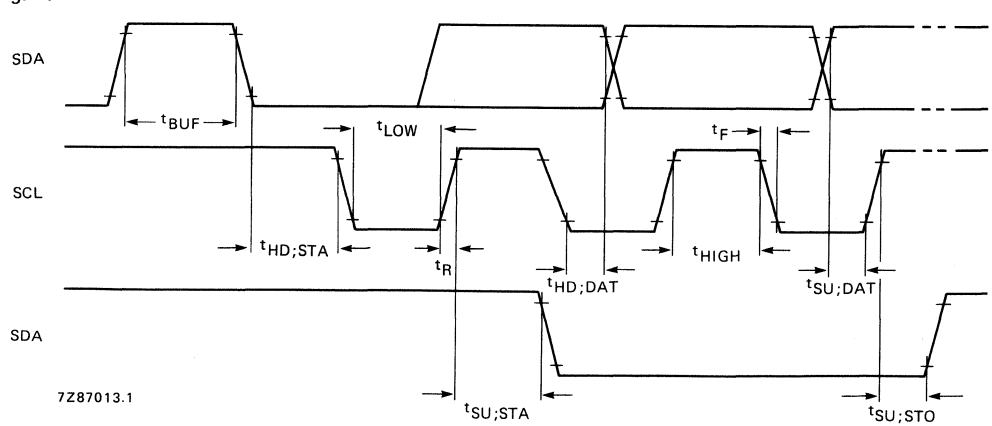


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}.

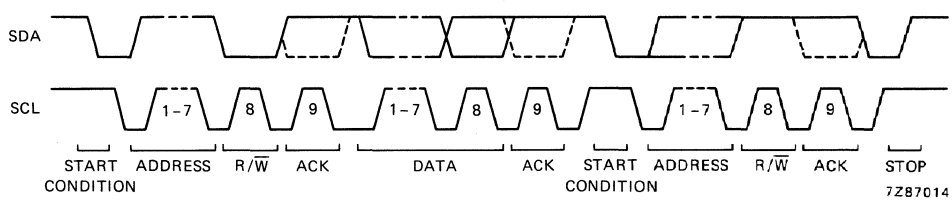


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

CHARACTERISTICS OF THE I²C BUS (continued)

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

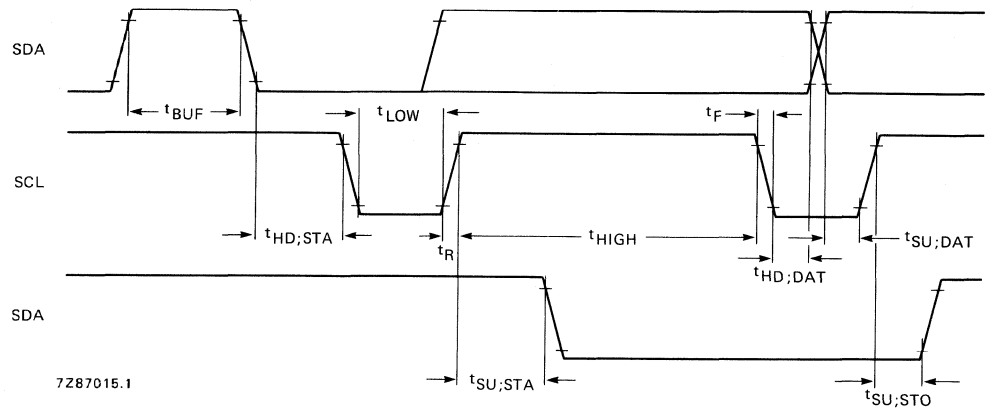


Fig. 9 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}, for definitions see high-speed mode.

* Only valid for repeated start code.

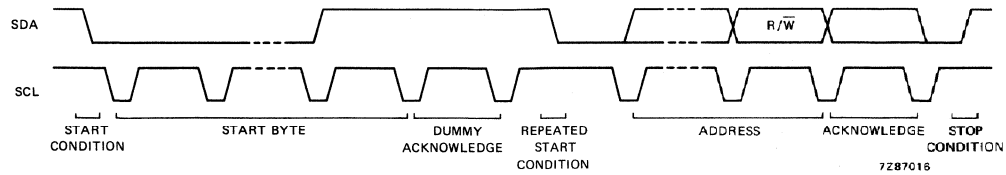


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

ADDRESSING

Before any data is transmitted on the I^2C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig. 11.

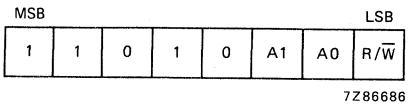


Fig. 11 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I^2C bus configuration for different clock/calendar READ and WRITE cycles is shown in Fig. 12 and Fig. 13.

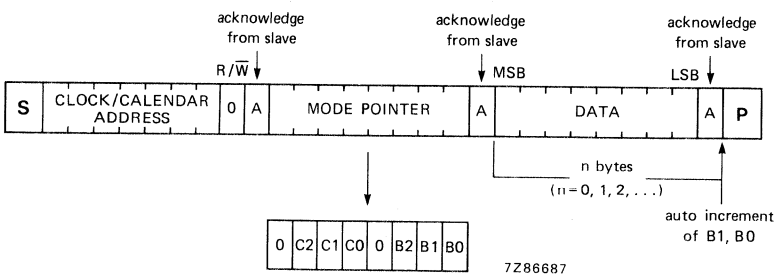


Fig. 12 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nibble is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

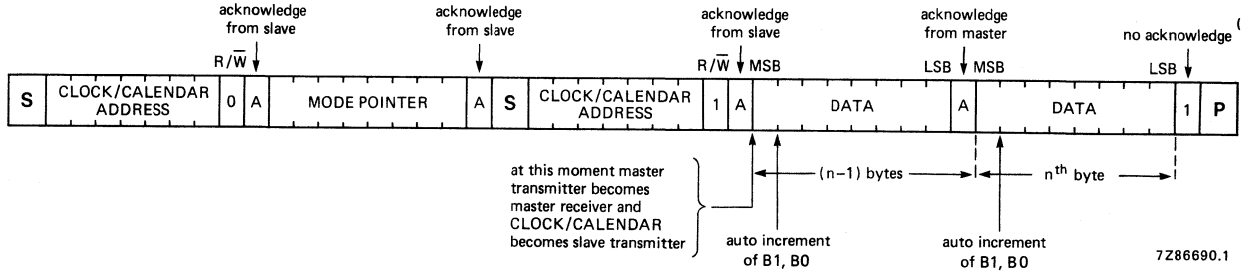
Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB				DATA			LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where "X" is the don't care bit and "D" is the data bit.

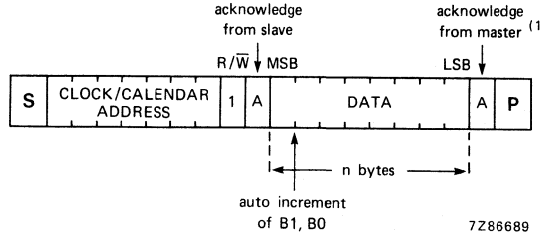
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 13 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 14 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where "X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where: "D" is the data bit.
* = minutes.
** = seconds.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges	$V_{DD}-V_{SS1}$		−0,3 to + 8	V
	$V_{DD}-V_{SS2}$		−0,3 to + 8	V
Voltage on pins 4 and 5		V_{SS2}	−0,8 to V_{DD} + 0,8	V*
Voltage on pins 6, 7, 13 and 14		V_{SS1}	−0,6 to V_{DD} + 0,6	V
Voltage on any other pin		V_{SS2}	−0,6 to V_{DD} + 0,6	V
Input current	I_I	max.	10	mA
Output current	I_O	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}		−40 to + 85	°C
Storage temperature range	T_{stg}		−55 to + 125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* Impedance min. 500 Ω.

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified. Typical values at T_{amb} = + 25 °C

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (I^2C interface)	$V_{DD}-V_{SS2}$	2,5	5	6,0	V
Supply voltage (clock)	$V_{DD}-V_{SS1}$	1,1	1,5	$(V_{DD}-V_{SS2})$	V
Supply current V_{SS1}					
at $V_{DD}-V_{SS1}$ = 1,5 V	$-I_{SS1}$	–	3	10	μA
at $V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
Supply current V_{SS2}					
at $V_{DD}-V_{SS2}$ = 5 V (I_O = 0 mA on all outputs)	$-I_{SS2}$	–	–	50	μA
Inputs SCL, SDA, A0, A1, TEST					
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW	V_{IL}	–	–	0,3 x V_{DD}	V
Input leakage current at V_I = V_{SS2} to V_{DD}	$\pm I_I$	–	–	1	μA
Inputs EXTPF, PFIN					
Input voltage HIGH	$V_{IH}-V_{SS1}$	0,7 x $(V_{DD}-V_{SS1})$	–	–	V
Input voltage LOW	$V_{IL}-V_{SS1}$	0	–	0,3 x $(V_{DD}-V_{SS1})$	V
Input leakage current					
at V_I = V_{SS1} to V_{DD}	$\pm I_I$	–	–	1	μA
at T_{amb} = 25 °C; V_I = V_{SS1} to V_{DD}	$\pm I_I$	–	–	0,1	μA
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)					
Output voltage HIGH					
at $V_{DD}-V_{SS2}$ = 2,5 V; $-I_O$ = 0,1 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
at $V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0,5 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
Output voltage LOW					
at $V_{DD}-V_{SS2}$ = 2,5 V; I_O = 0,3 mA	V_{OL}	–	–	0,4	V
at $V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1,6 mA	V_{OL}	–	–	0,4	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Output SDA (N-channel open drain)					
Output "ON": I_O = 3 mA at $V_{DD}-V_{SS2}$ = 2,5 to 6 V	V_{OL}	–	–	0,4	V
Output "OFF" (leakage current) at $V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	I_O	–	–	1	μA
Internal threshold voltage					
Power failure detection	V_{TH1}	1	1,2	1,4	V
Power "ON" reset at $V_{SCL} = V_{SDA} = V_{DD}$	V_{TH2}	1,5	2,0	2,5	V
Rise and fall times of input signals					
Input EXTPF	t_r, t_f	–	–	1	μs
Input PFIN	t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels					
rise time	t_r	–	–	1	μs
fall time	t_f	–	–	0,3	μs
Frequency at SCL					
at $V_{DD}-V_{SS2}$ = 4 to 6 V					
Pulse width LOW (see Figs 7 and 9)	t_{LOW}	4,7	–	–	μs
Pulse width HIGH (see Figs 7 and 9)	t_{HIGH}	4	–	–	μs
Noise suppression time constant at SCL and SDA input	T_I	0,25	1	2,5	μs
Input capacitance (SCL, SDA)	C_I	–	–	7	pF
Oscillator					
Integrated oscillator capacitance	C_{out}	–	40	–	pF
Oscillator feedback resistance	R_f	–	3	–	MΩ
Oscillator stability for: $\Delta(V_{DD}-V_{SS1})$ = 100 mV at $V_{DD}-V_{SS1}$ = 1,55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-6}	–	–
Quartz crystal parameters					
Frequency = 32,768 kHz					
Series resistance	R_S	–	–	40	kΩ
Parallel capacitance	C_L	–	9	–	pF
Trimmer capacitance	C_T	5	–	25	pF

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

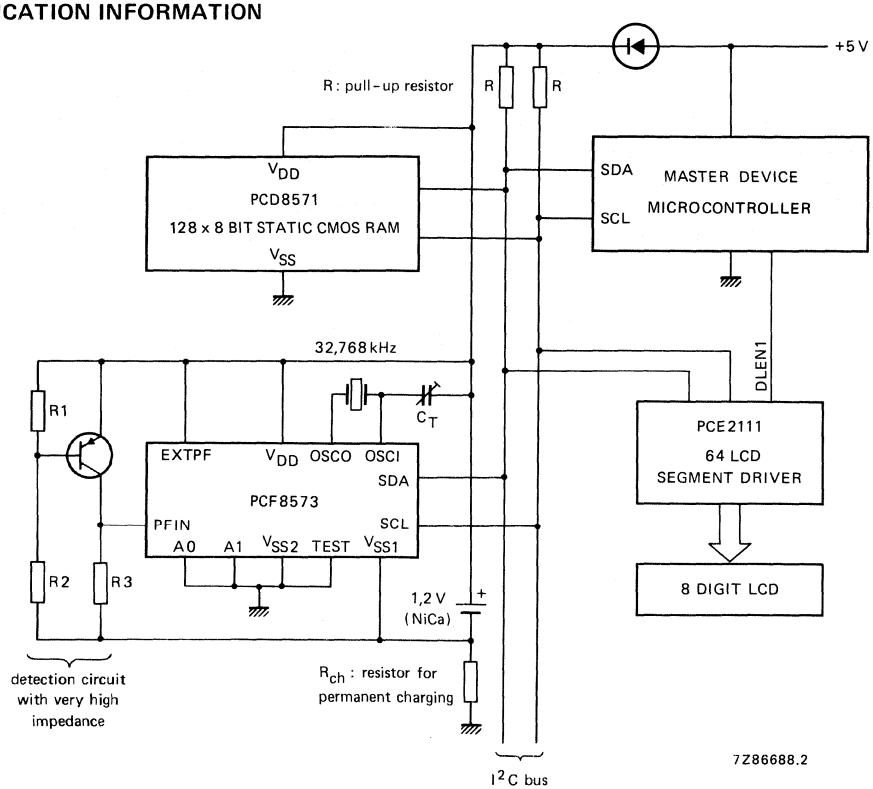


Fig. 15 Application example of the PCF8573 clock/calendar.

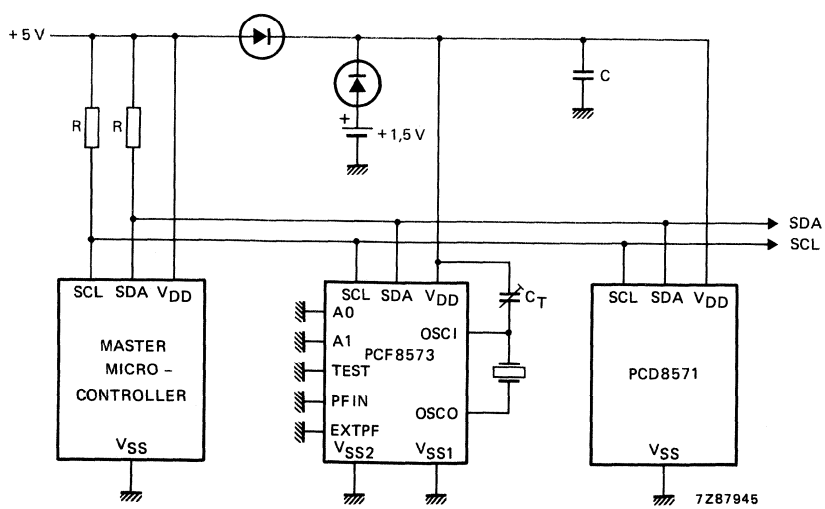


Fig. 16 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

REMOTE 8-BIT I/O FOR I²C BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF8500 microcomputer families via the two-line serial bidirectional bus (I^2C).
It can also interface microcomputers without a serial interface to the I^2C bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I^2C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I^2C bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I^2C bus. This means that the PCF8574 can remain a simple slave device.

Features

- Operating supply voltage 2,5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I^2C bus
- Peripheral for the MAB8400 and PCF8500 microcomputer families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 possible with mask option)

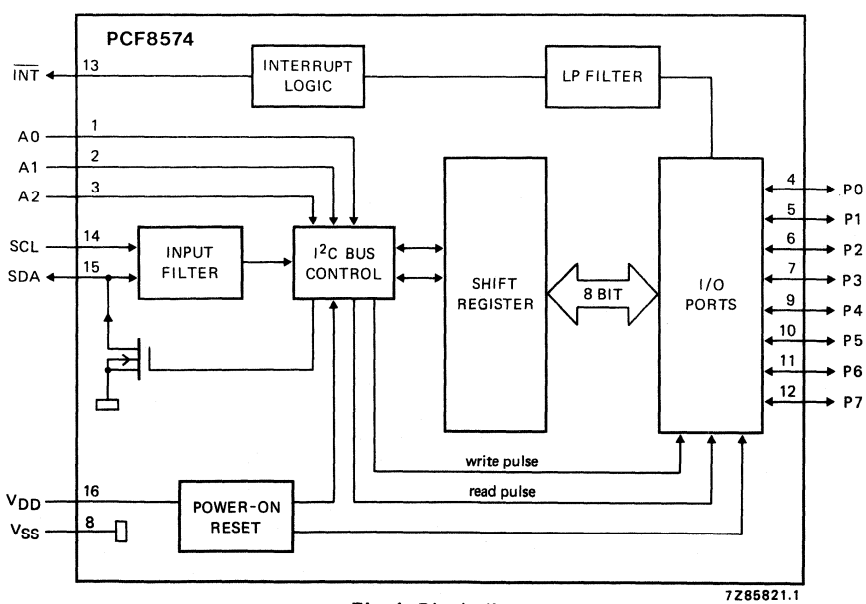


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8574P: 16-lead DIL; plastic (SOT-38).
PCF8574T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

PINNING

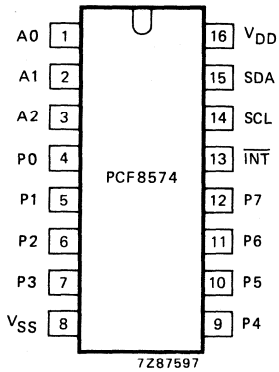


Fig. 2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7 9 to 12	P0 to P3 P4 to P7	8-bit quasi-bidirectional I/O port
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

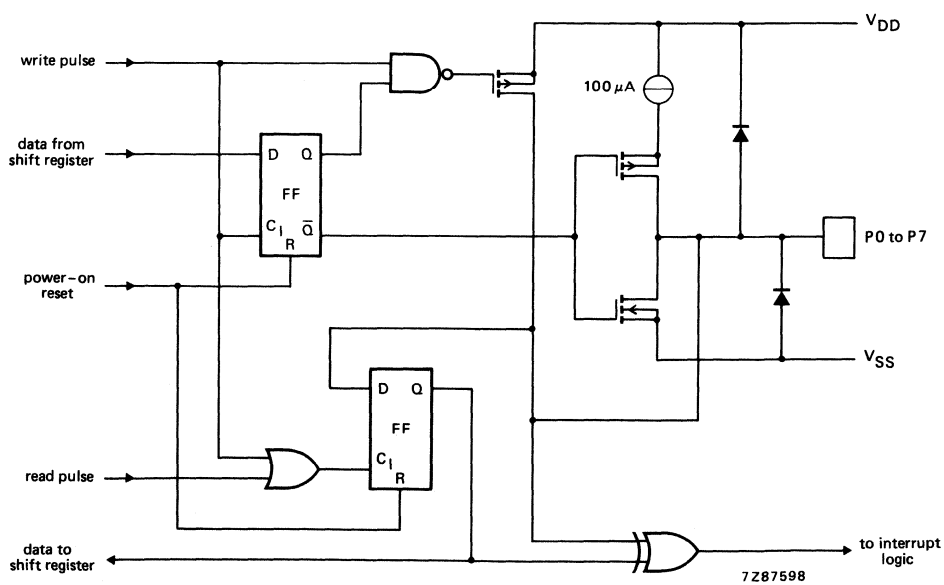


Fig. 3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

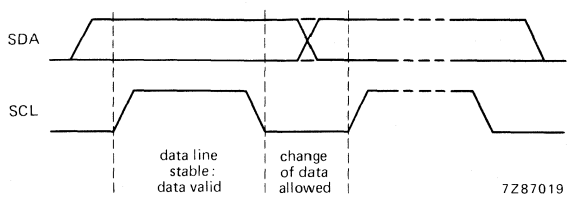


Fig. 4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

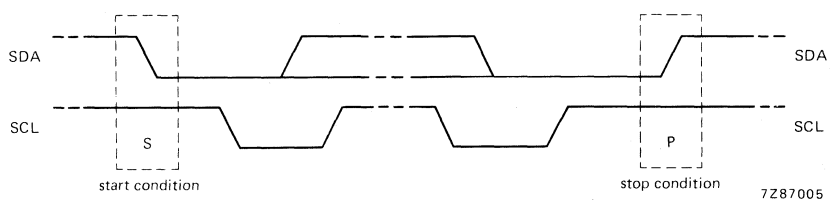


Fig. 5 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

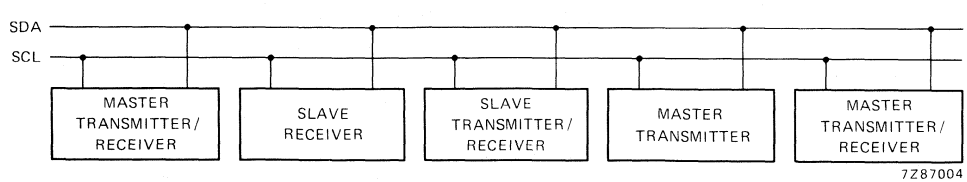


Fig. 6 System configuration.

CHARACTERISTICS OF THE I²C BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

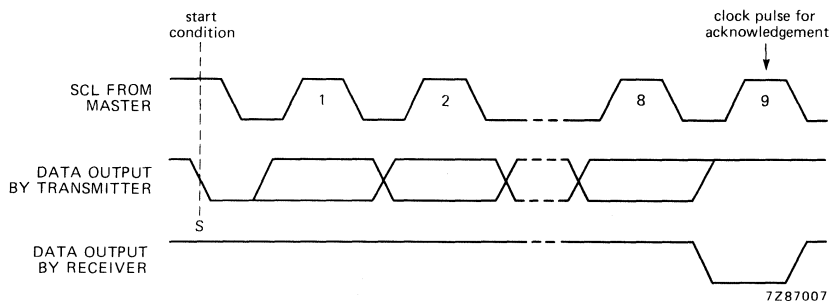


Fig. 7 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8574 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 8.

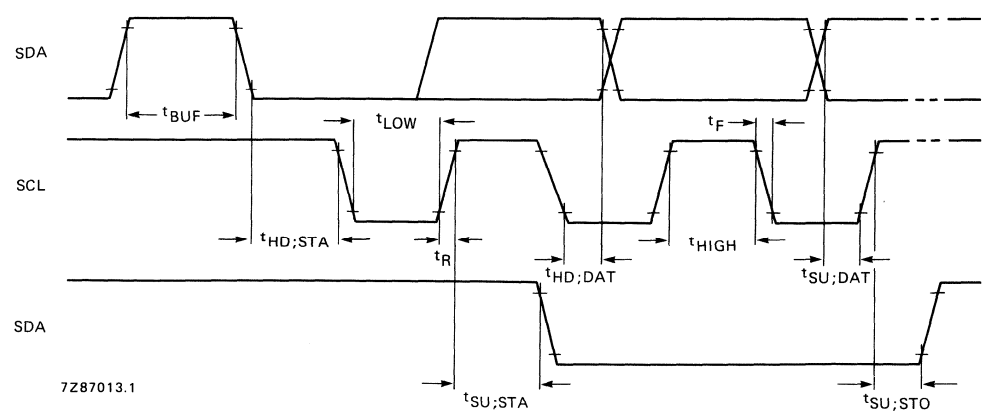


Fig. 8 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

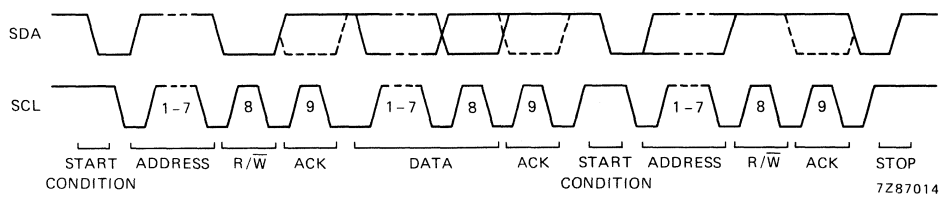


Fig. 9 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

CHARACTERISTICS OF THE I²C BUS (continued)

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 10.

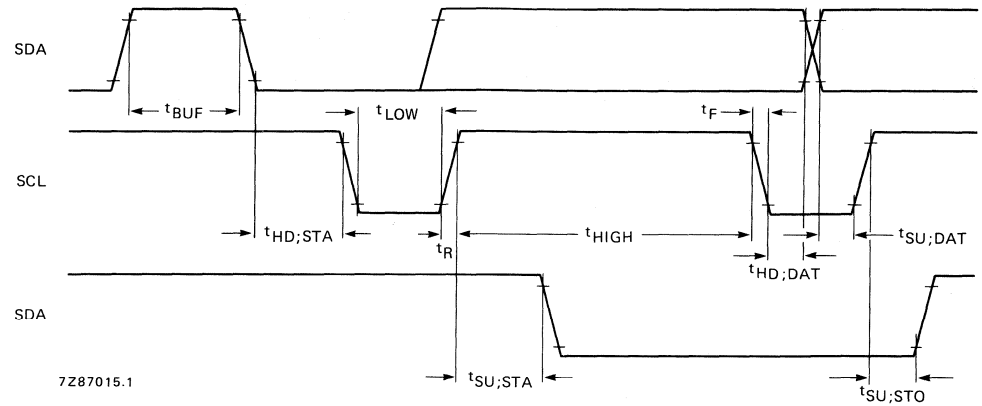


Fig. 10 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see high-speed mode.

* Only valid for repeated start code.

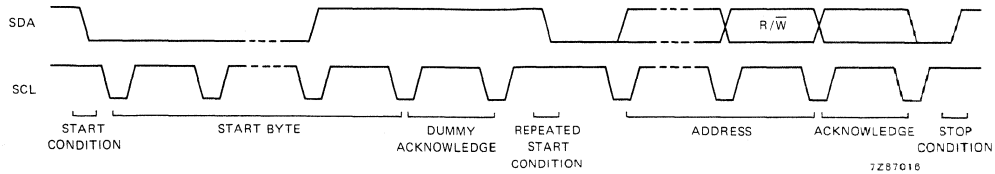


Fig. 11 Complete data transfer in the low-speed mode.

Where:	
Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

FUNCTIONAL DESCRIPTION

Addressing (see Figs 12 and 13)

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

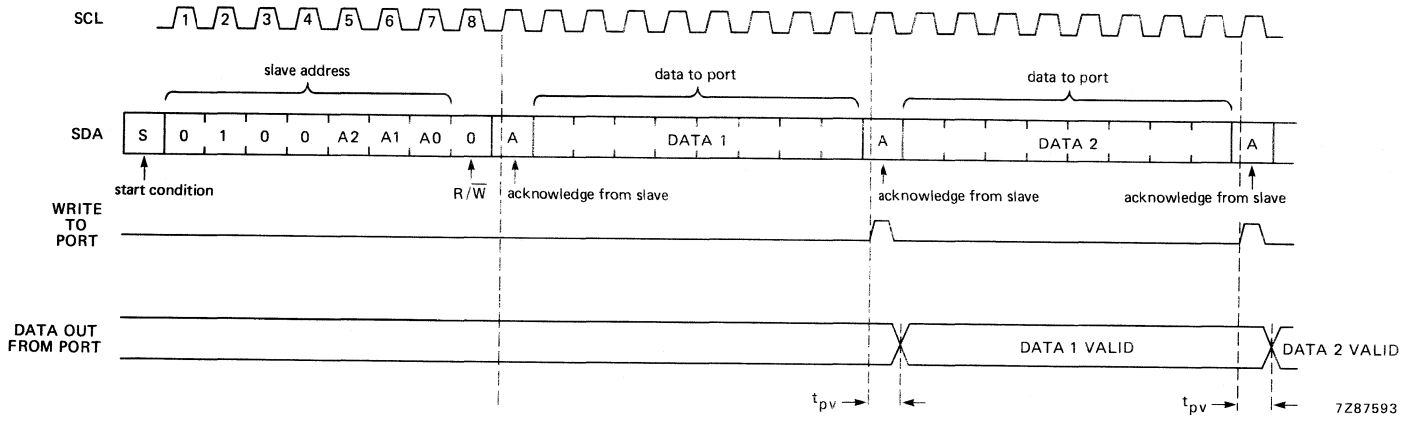


Fig. 12 WRITE mode (output port).

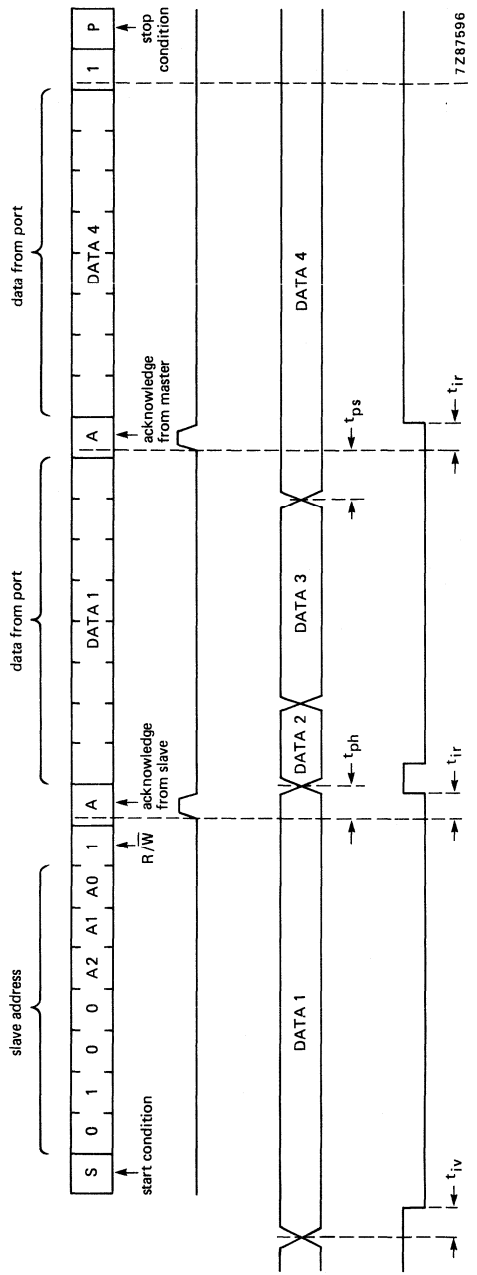


Fig. 13 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 14 and 15)

The PCF8574 provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

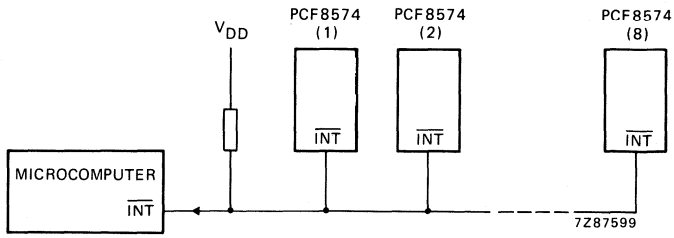


Fig. 14 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH to LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

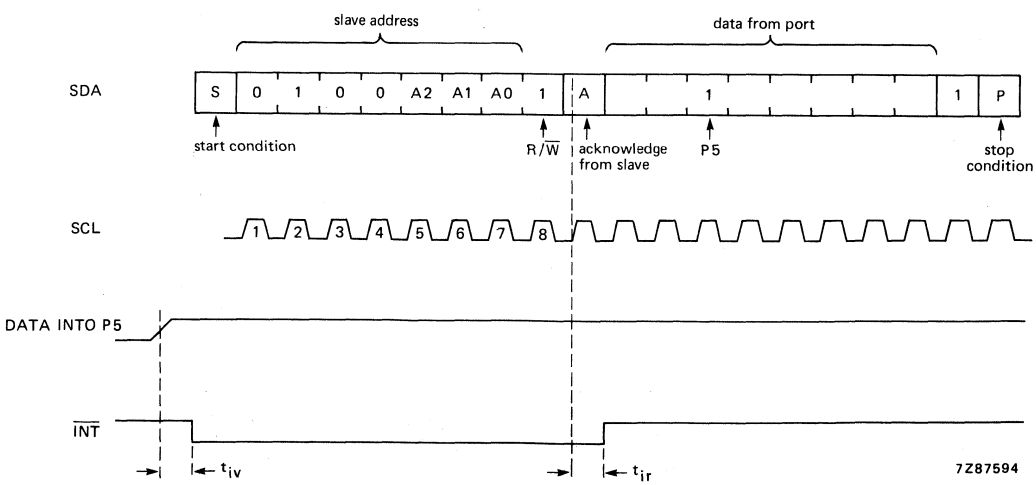


Fig. 15 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig. 16)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. The bit designated as an input must first be loaded with a logic 1. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output changes from LOW to HIGH, and are switched off by the negative edge of SCL. SCL should not remain HIGH when a short-circuit to V_{SS} is allowed (input mode).

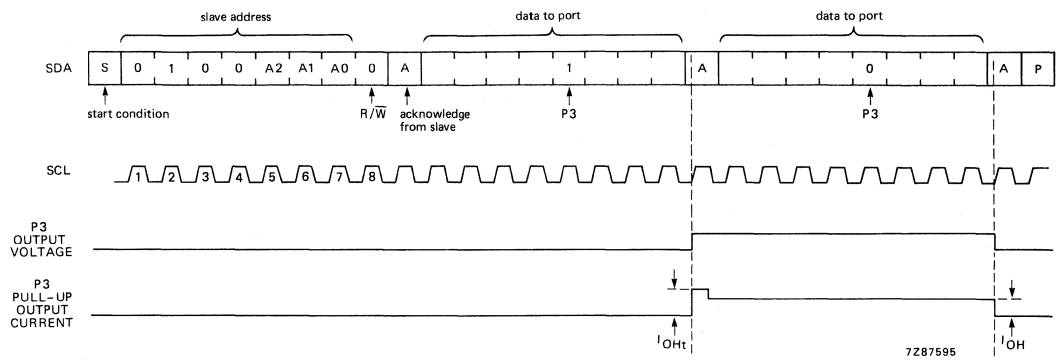


Fig. 16 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to + 7	V
Input voltage range (any pin)	V_I	V_{SS}−0,5 to V_{DD} + 0,5	V
D.C. current into any input	$\pm I_I$ max.	20	mA
D.C. current into any output	$\pm I_O$ max.	25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; I_{SS} max.	100	mA
Total power dissipation	P_{tot} max.	400	mW
Power dissipation per output	P_o max.	100	mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

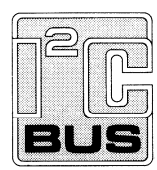
parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current					
at V_{DD} = 6 V; no load, inputs at V_{DD}, V_{SS}					
operating; (SCL = 100 kHz)	I_{DD}	–	40	100	μA
standby	I_{DDO}	–	1,5	10	μA
Power-on reset voltage level (note 1)	V_{REF}	–	1,3	2,4	V
Input SCL; input/output SDA (pins 14; 15)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD} + 0,5 V	V
Output current LOW					
at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Input/Output leakage current	$\|I_L\|$	–	–	100	nA
Clock frequency (see Fig. 8)	f_{SCL}	–	–	100	kHz
Tolerable spike width					
at SCL and SDA input	t_s	–	–	100	ns
Input capacitance (SCL, SDA)					
at V_I = V_{SS}	C_I	–	–	7	pF
I/O ports (pins 4 to 7; 9 to 12)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD} + 0,5 V	V
Maximum allowed input current through protection diode					
at $V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW					
at V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	30	–	mA
Output current HIGH					
at V_{OH} = V_{SS} (current source only)	$-I_{OH}$	30	100	300	μA
Transient pull-up current HIGH during acknowledge (see Fig. 16)					
at V_{OH} = V_{SS}	$-I_{OHt}$	–	0,5	–	mA
Input/Output capacitance	$C_{I/O}$	–	–	10	pF
Port timing; $C_L \leqslant 100$ pF (see Figs 12 and 13)					
Output data valid	t_{pv}	–	–	4	μs
Input data set-up	t_{ps}	0	–	–	μs
Input data hold	t_{ph}	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$ (pin 13)					
Output current LOW at V_{OL} = 0,4 V	I_{OL}	1,6	–	–	mA
Output current HIGH at $V_{OH} = V_{DD}$	$\|I_{OH}\|$	–	–	100	nA
$\overline{INT}$ timing; $C_L \leqslant 100$ pF (see Fig. 13)					
Input data valid	t_{iv}	–	–	4	μs
Reset delay	t_{ir}	–	–	4	μs
Select inputs A0, A1, A2 (pins 1 to 3)					
Input voltage LOW	V_{IH}	−0,5 V	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD} + 0,5 V	V
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	100	nA

Note 1

The power-on reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$ and sets all ports to logic 1 (input mode with current source to V_{DD}).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.



UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold(automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO-56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO-56; SOT-190).
PCF8576U: uncased chip in tray

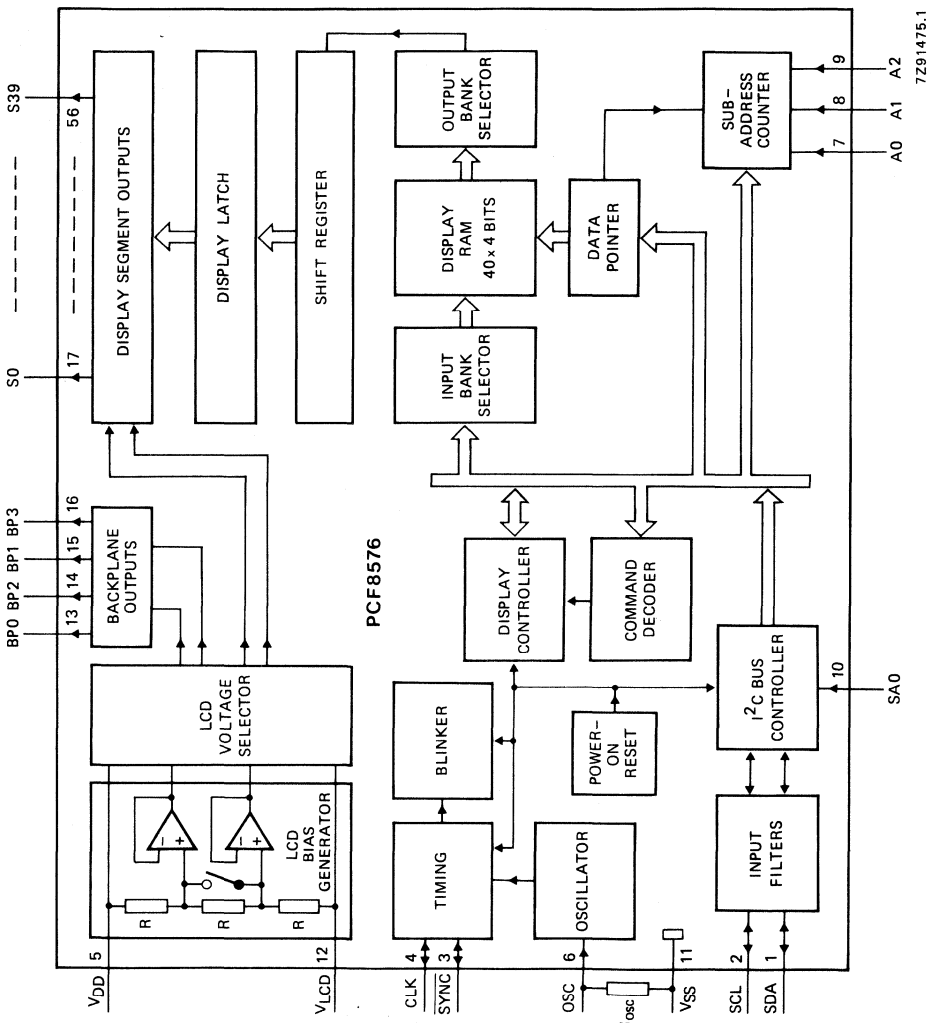


Fig. 1 Block diagram.

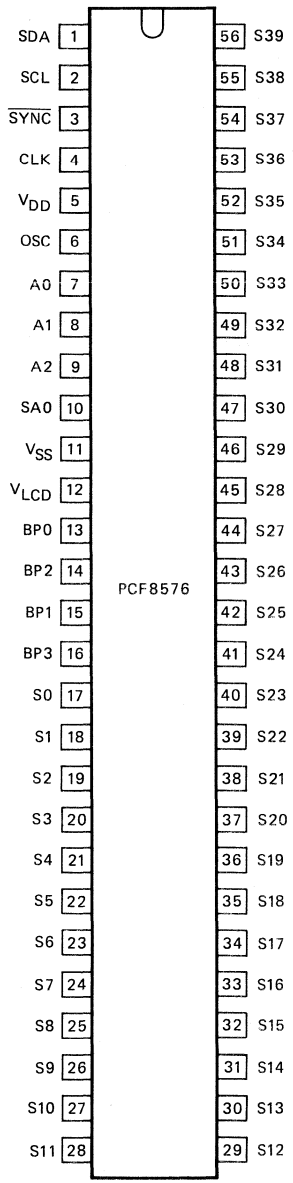


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 56	S0 to S39	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	160	20 digits + 20 indicator symbols	10 characters + 20 indicator symbols	160 dots (4 x 40)
3	120	15 digits + 15 indicator symbols	8 characters + 8 indicator symbols	120 dots (3 x 40)
2	80	10 digits + 10 indicator symbols	5 characters + 10 indicator symbols	80 dots (2 x 40)
1	40	5 digits + 5 indicator symbols	2 characters + 12 indicator symbols	40 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor maintains the 2-line I²C bus communication channel with the PCF8576. A resistor connected between OSC (pin 6) and V_{SS} (pin 11) controls the device clock frequency. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

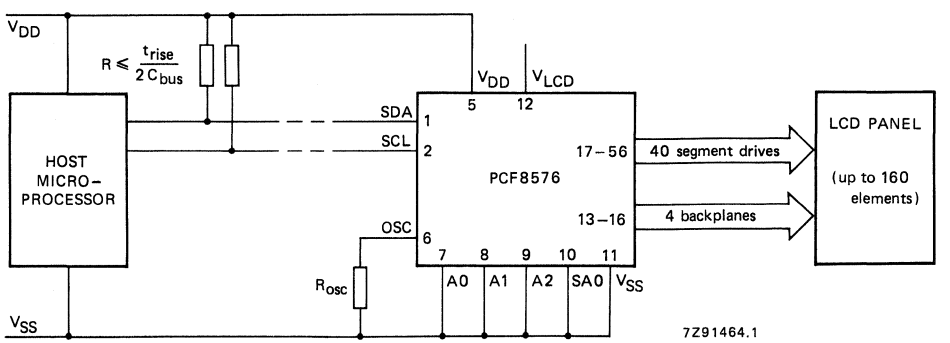


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8576 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{thLCD}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\,V_{thLCD}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\,V_{off(rms)} = 2{,}449\,V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\;V_{off(rms)} = 2{,}309\,V_{off(rms)}$

These compare with $V_{op} = 3\,V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

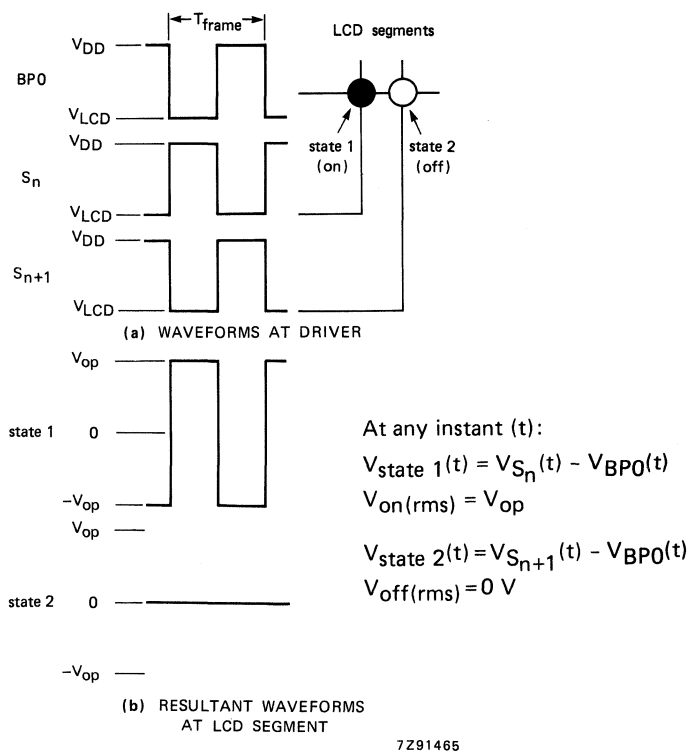


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8576 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

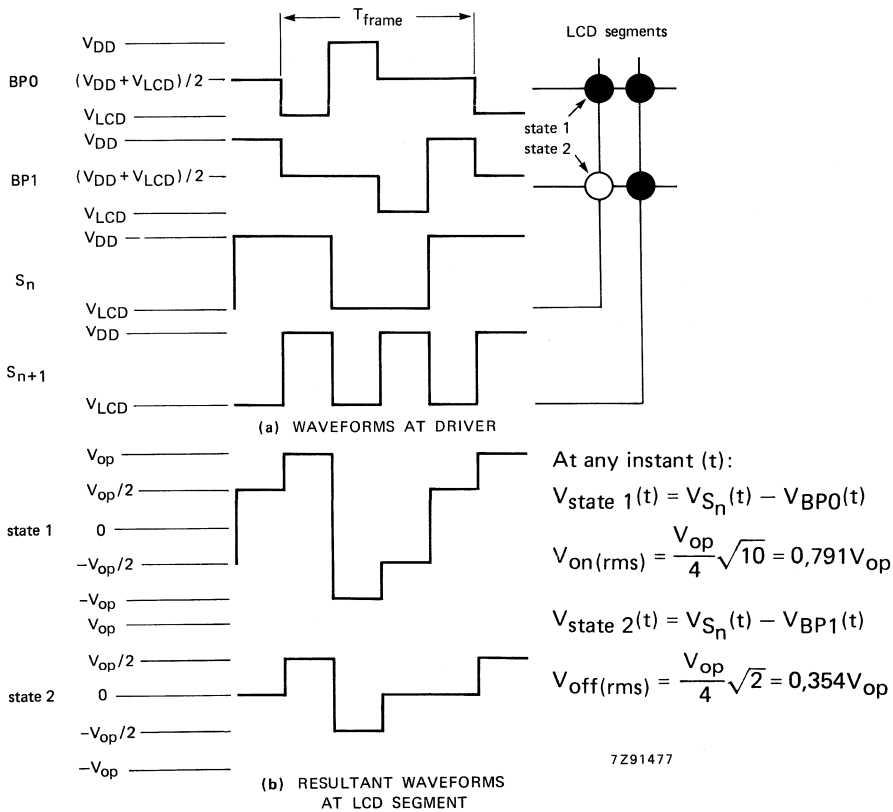


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

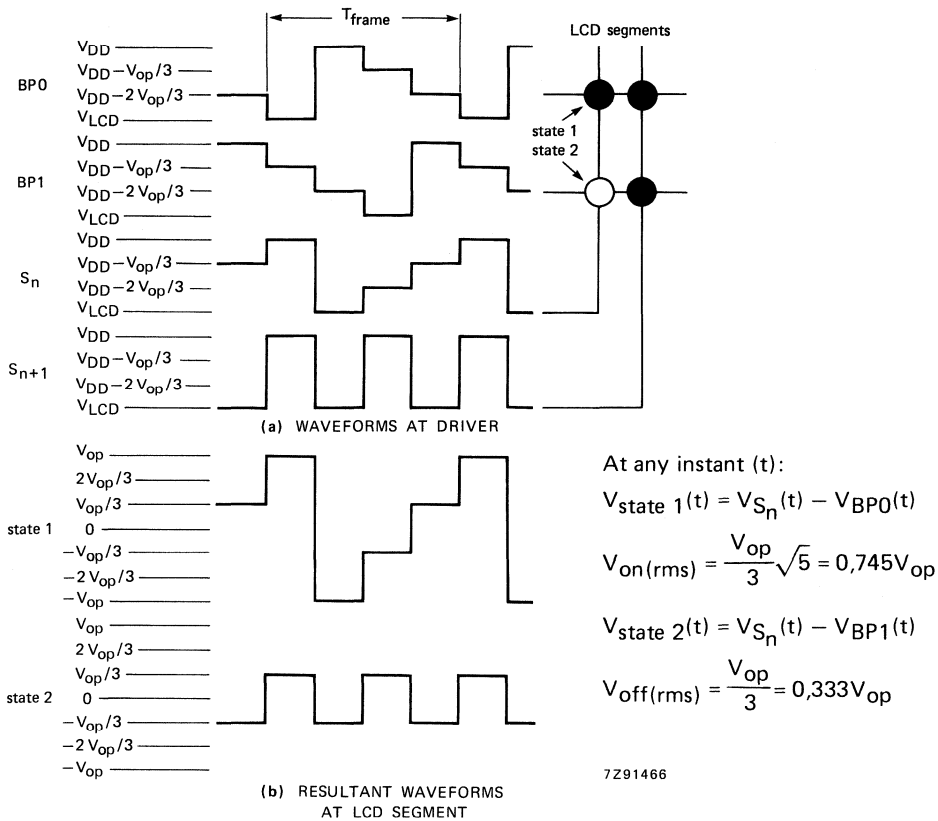


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

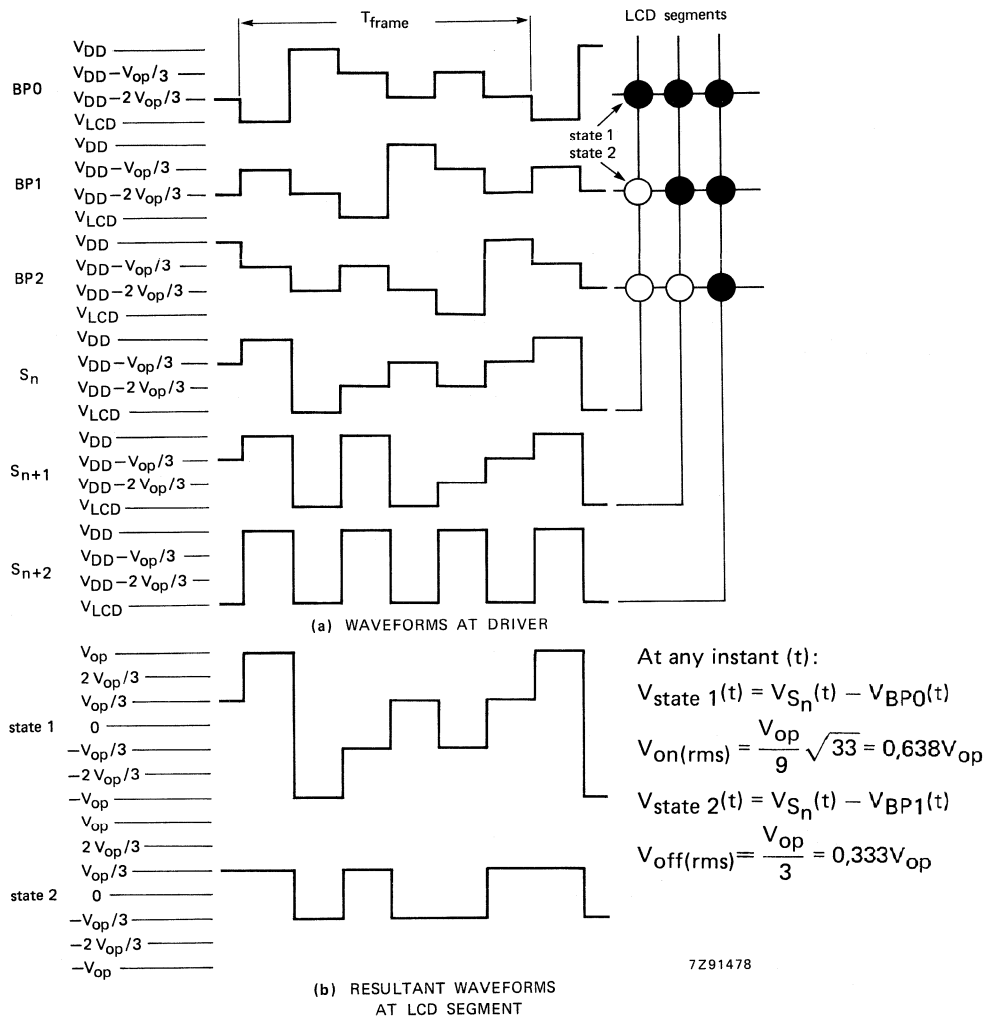


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

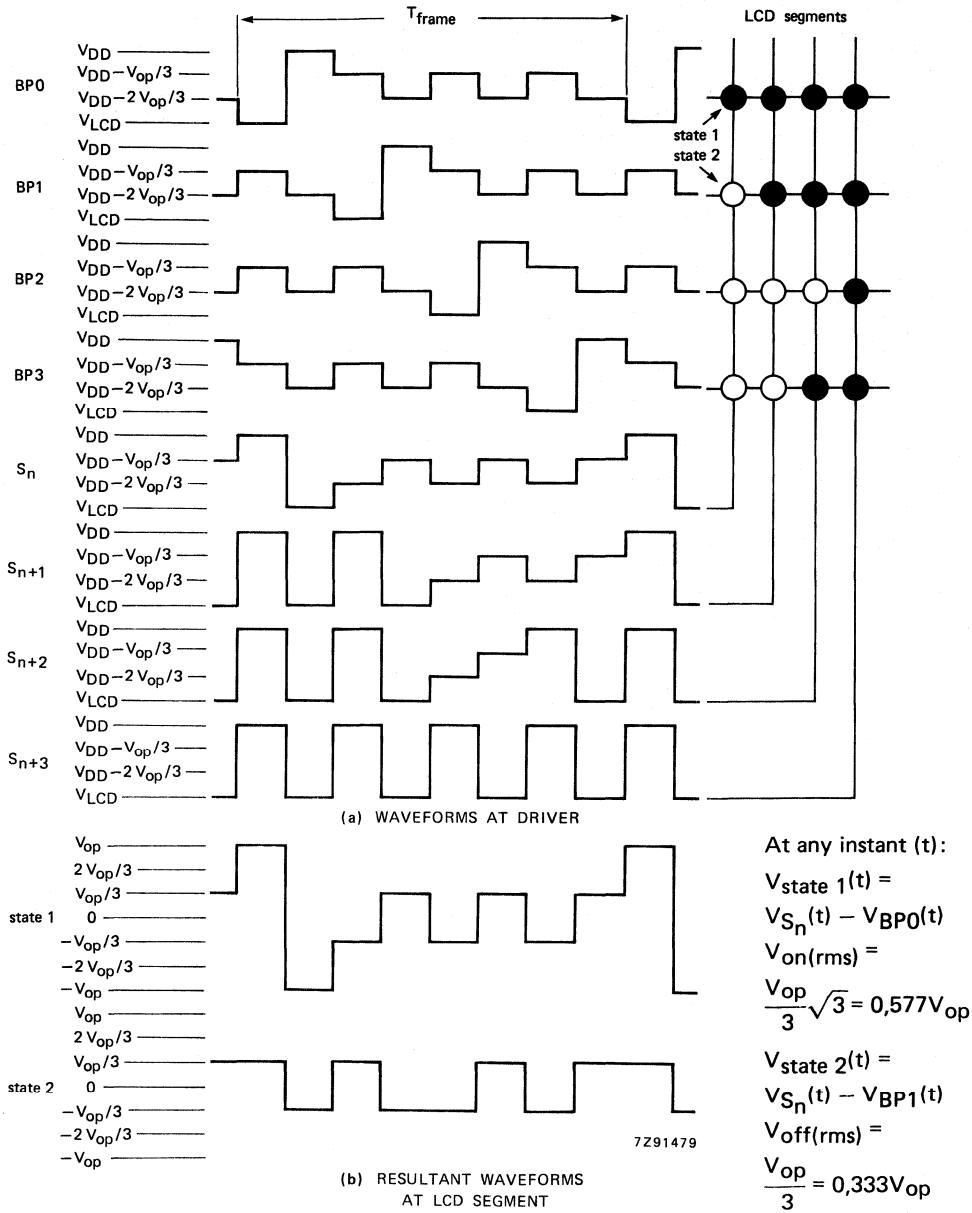


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

Internal clock

The internal logic and the LCD drive signals of the PCF8576 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, frequency control is performed by a single resistor connected between OSC (pin 6) and V_{SS} (pin 11) as shown in Fig. 9. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8576s in the system.

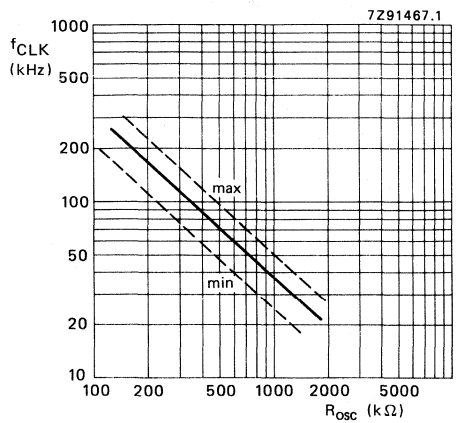


Fig. 9 Oscillator frequency as a function of R_{osc}: $f_{CLK} \approx (3{,}4 \times 10^7 / R_{osc})$ kHz·Ω.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a d.c. state.

Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by the choice of value for R_{osc} when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8576 mode	recommended R_{osc} (kΩ)	f_{frame}	nominal f_{frame} (Hz)
normal mode	180	$f_{CLK}/2880$	64
power-saving mode	1200	$f_{CLK}/480$	64

Timing (continued)

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the normal mode, R_{OSC} = 180 kΩ will result in the nominal frame frequency. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six and for the same frame frequency R_{OSC} will be 1,2 MΩ. The reduced clock frequency and the increased value of R_{OSC} together contribute to a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed back-plane signals and with the data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (Fig. 10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

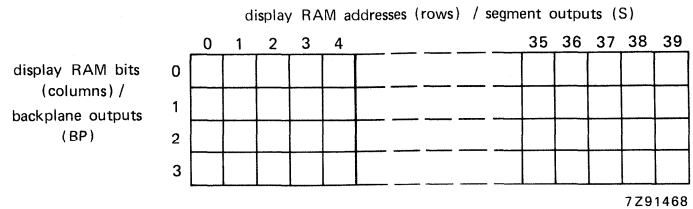


Fig. 10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8576 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 11. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

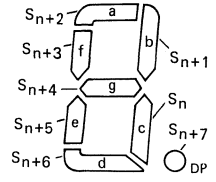
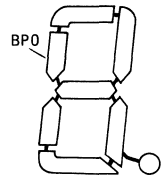
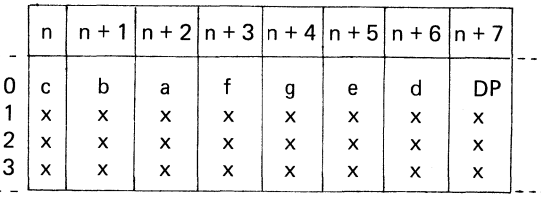
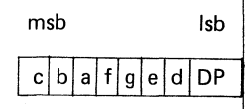
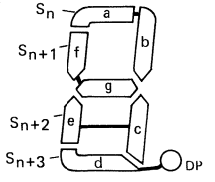
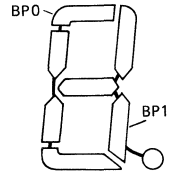
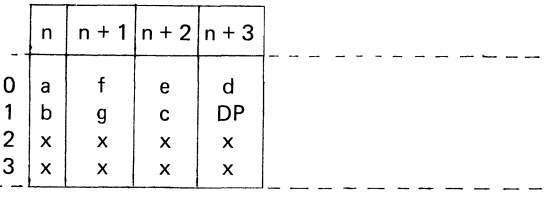
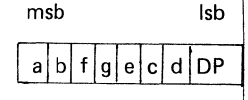
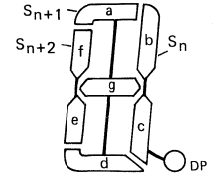
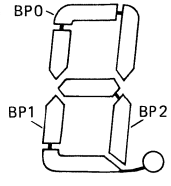
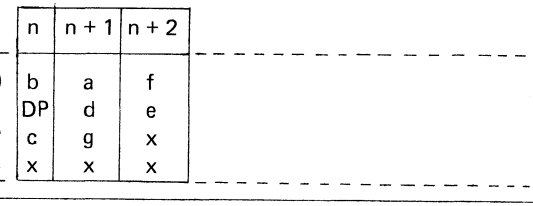
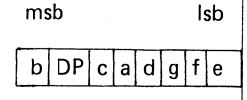
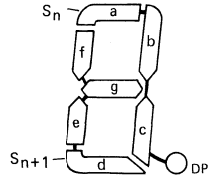
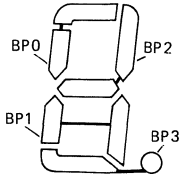
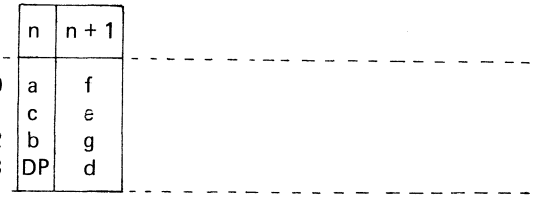
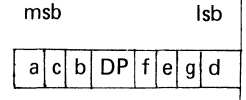
drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

Fig. 11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

7Z91469

Subaddress counter (continued)

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Blinker (continued)

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

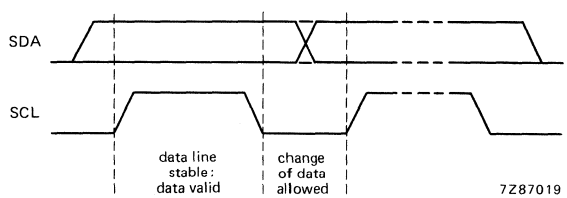


Fig. 12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

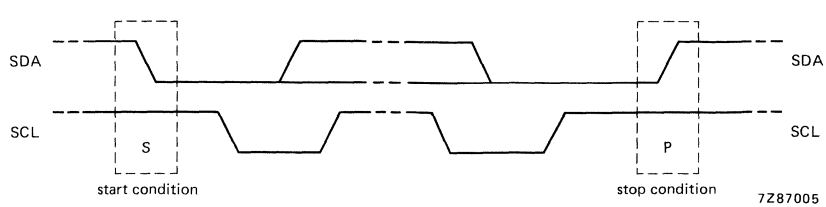


Fig. 13 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

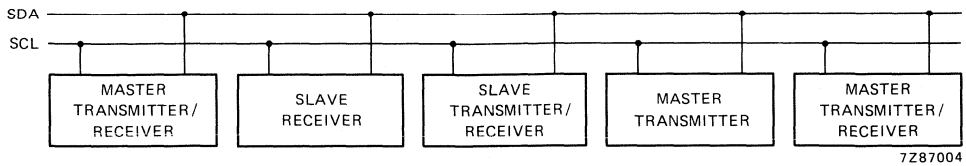


Fig. 14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

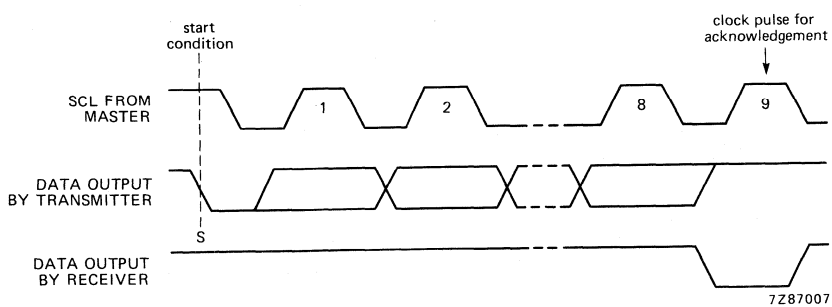


Fig. 15 Acknowledgement on the I²C bus.

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

PCF8576 I²C bus controller

The PCF8576 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111000 and 0111001) are reserved for PCF8576. The least-significant bit of the slave address that a PCF8576 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8576s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 16. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8576. After the last display byte, the I²C bus master issues a stop condition (P).

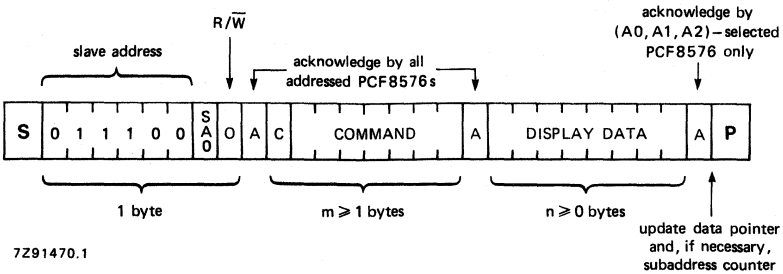


Fig. 16 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

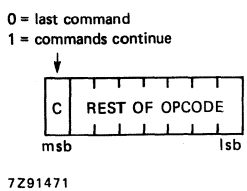


Fig. 17 General format of command byte.

The five commands available to the PCF8576 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8576 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 P5 P4 P3 P2 P1 P0	bits P5 P4 P3 P2 P1 P0 6-bit binary value of 0 to 39	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT
<table><tr><td>C</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>I</td><td>O</td></tr></table></td><td><table><tr><th>static</th><th>1 : 2 MUX</th><th>bit I</th></tr><tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr></table><table><tr><th>static</th><th>1 : 2 MUX</th><th>bit O</th></tr><tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr></table></td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK
<table><tr><td>C</td><td>1</td><td>1</td><td>1</td><td>0</td><td>A</td><td>BF1</td><td>BF0</td></tr></table></td><td><table><tr><th>blink frequency</th><th>bits BF1</th><th>BF0</th></tr><tr><td>off</td><td>0</td><td>0</td></tr><tr><td>2 Hz</td><td>0</td><td>1</td></tr><tr><td>1 Hz</td><td>1</td><td>0</td></tr><tr><td>0,5 Hz</td><td>1</td><td>1</td></tr></table><table><tr><th>blink mode</th><th>bit A</th></tr><tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr></table></td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8576s. When cascaded, several PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig. 18).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig. 19.

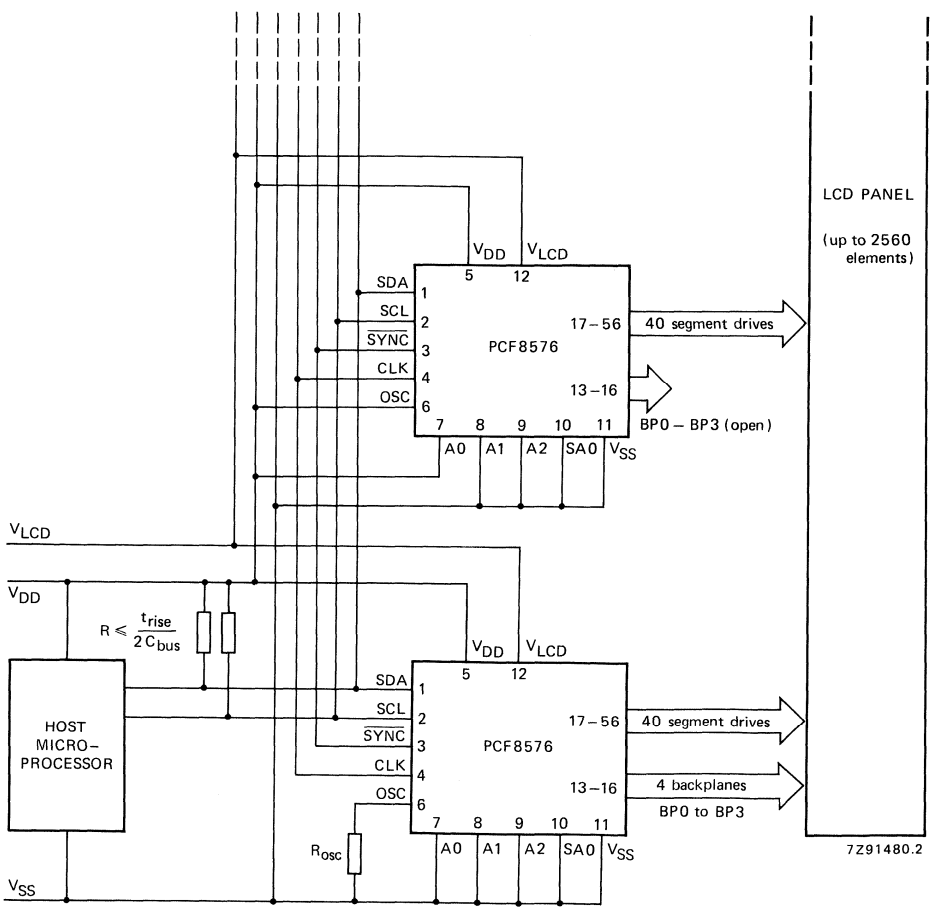


Fig. 18 Cascaded PCF8576 configuration.

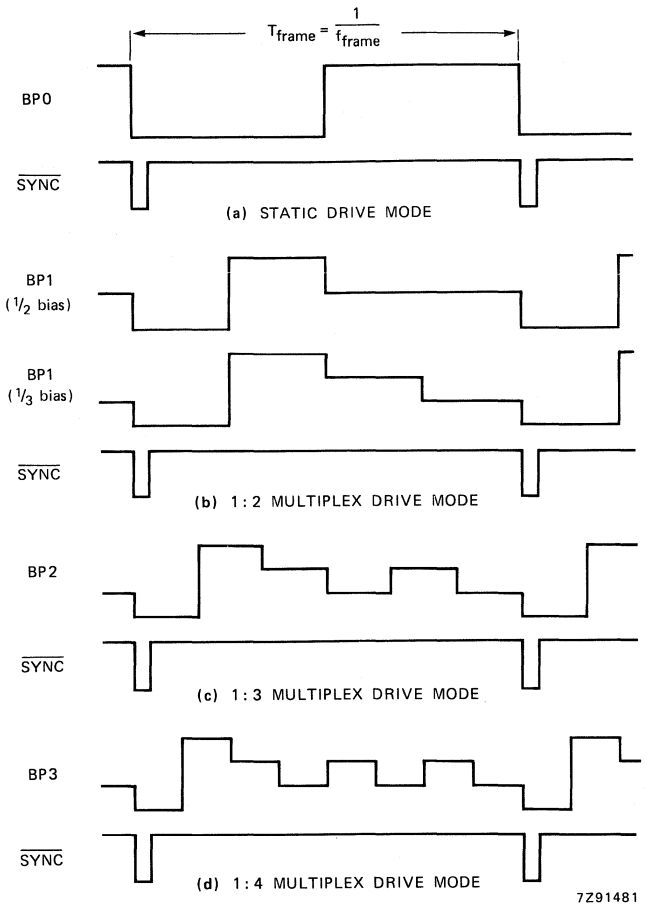


Fig. 19 Synchronization of the cascade for the various PCF8576 drive modes.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see application information.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 11 V
LCD supply voltage range	V_{LCD}		V_{DD}−11 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S39; BP0 to BP3)	V_O		V_{LCD}−0,5 to V_{DD} + 0,5 V
D.C. input current	$\pm I_I$	max.	20 mA
D.C. output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2 to 9 V; V_{LCD} = V_{DD}−2 to V_{DD}−9 V;
T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2	—	9	V
LCD supply voltage (note 1)	V_{LCD}	V_{DD}−9	—	V_{DD}−2	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 2)	I_{DD}	—	—	180	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz (note 2)	I_{LP}	—	—	60	μA
LCD supply current (normal mode) at f_{CLK} = 200 kHz (note 2)	I_{LCD}	—	—	120	μA
Logic					
Input voltage LOW	V_{IL}	V_{SS}	—	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	—	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	—	—	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD}−0,05	—	—	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	—	—	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	—	—	−1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	—	—	mA
Leakage current (SA0; A0 to A2; CLK; SCL; SDA) at V_I = V_{SS} or V_{DD}	$\pm I_{L1}$	—	—	1	μA

parameter	symbol	min.	typ.	max.	unit
Leakage current (OSC) at $V_I = V_{DD}$	$\pm I_{L2}$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	20	50	150	kΩ
Power-on reset level (note 3)	V_{REF}	–	1,0	1,6	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 4)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S39) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}$–5 V (note 5)	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S39) at $V_{LCD} = V_{DD}$–5 V (note 5)	R_S	–	–	7,0	kΩ

A.C. CHARACTERISTICS (note 6)

V_{SS} = 0 V; V_{DD} = 2 to 9 V; $V_{LCD} = V_{DD}$–2 to V_{DD}–9 V;
T_{amb} = –40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V; R_{osc} = 180 kΩ (note 7)	f_{CLK}	125	185	288	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V; R_{osc} = 1,2 MΩ	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at $V_{LCD} = V_{DD}$–5 V	t_{PLCD}	–	–	30	μs

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
I²C bus high-speed mode					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs
I²C bus low-speed mode					
Bus free time	t_{BUF}	105	–	–	μs
Start condition hold time	$t_{HD;STA}$	365	–	–	μs
SCL LOW time	t_{LOW}	105	–	155	μs
SCL HIGH time	t_{HIGH}	365	–	415	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	105	–	155	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	105	–	155	μs

Notes to characteristics

1. $V_{LCD} < V_{DD}-3$ V for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty cycle; I²C bus inactive.
3. Resets all logic when $V_{DD} < V_{REF}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

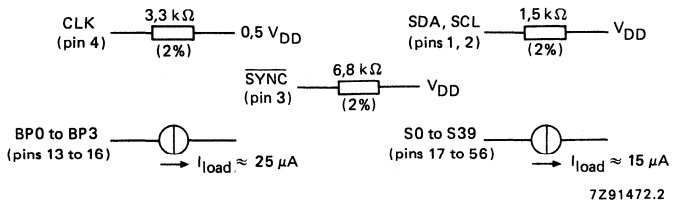


Fig. 20 Test loads.

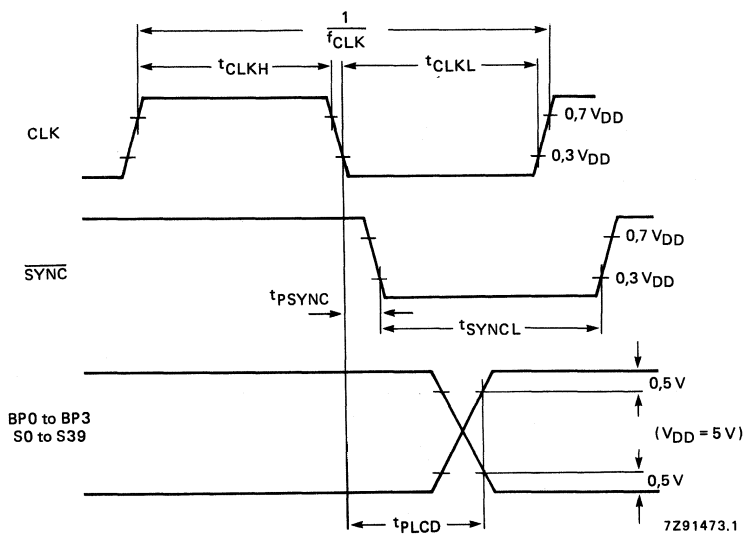


Fig. 21 Driver timing waveforms.

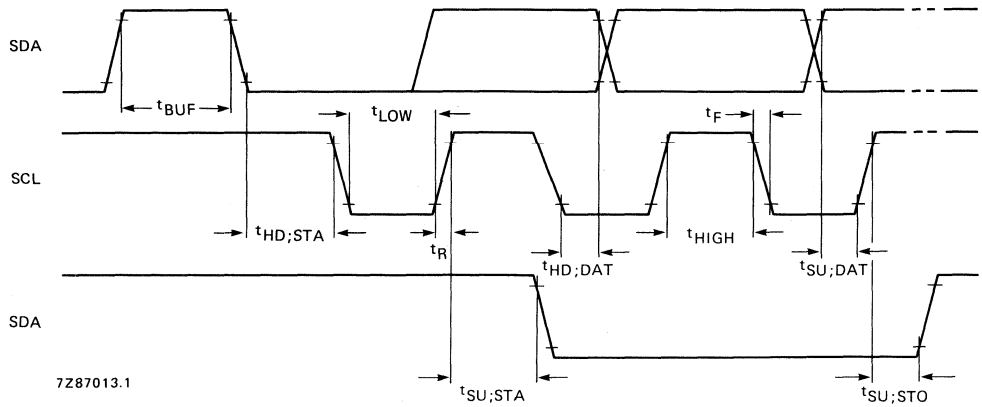


Fig. 22 I²C bus high-speed mode timing waveforms.

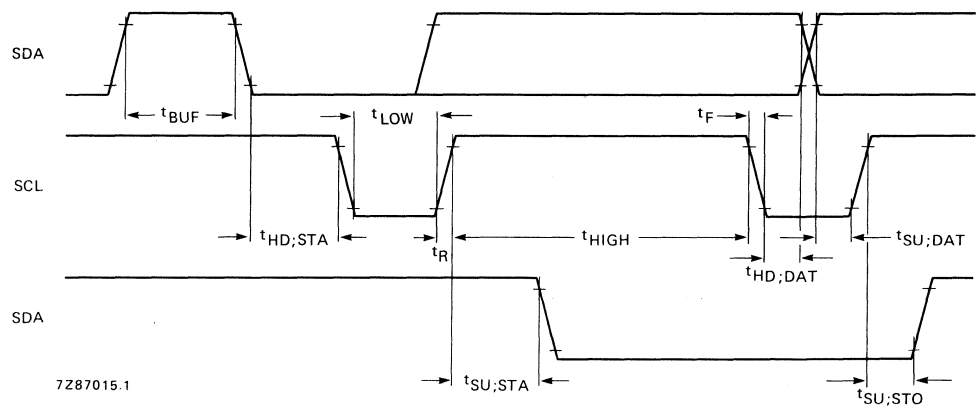
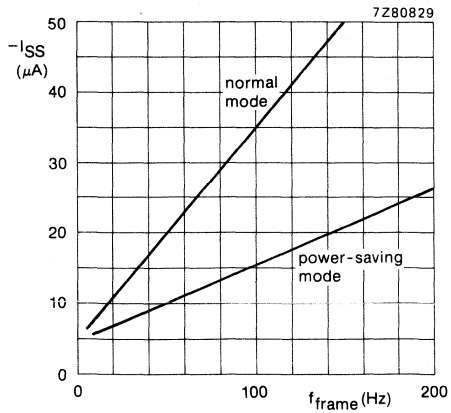
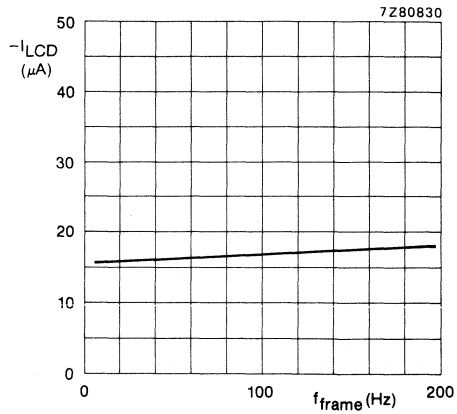


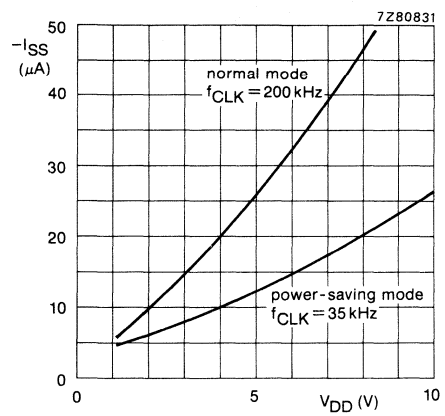
Fig. 23 I²C bus low-speed mode timing waveforms.



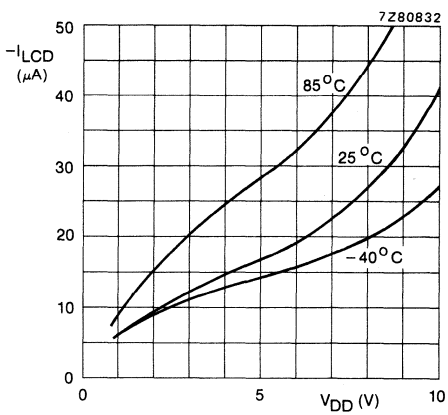
(a) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

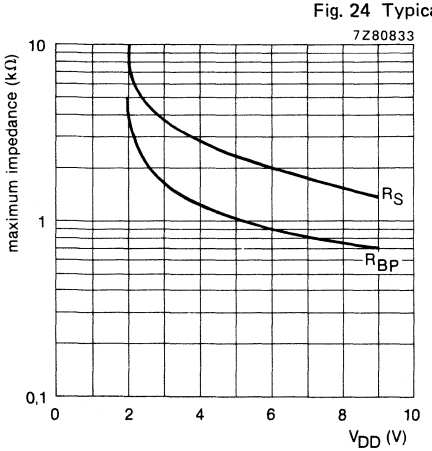


(c) V_{LCD} = 0 V; external clock; T_{amb} = −40 to + 85 °C.

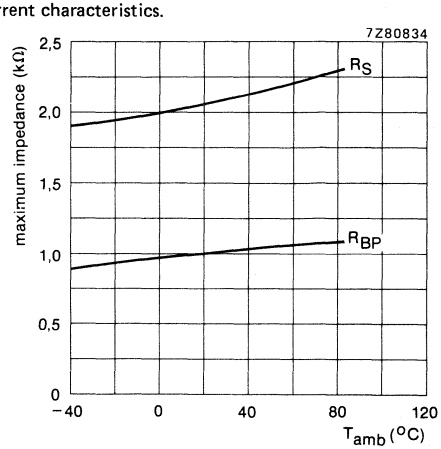


(d) V_{LCD} = 0 V; external clock; f_{CLK} = nominal frequency.

Fig. 24 Typical supply current characteristics.



(a) V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V.

Fig. 25 Typical characteristics of LCD outputs.

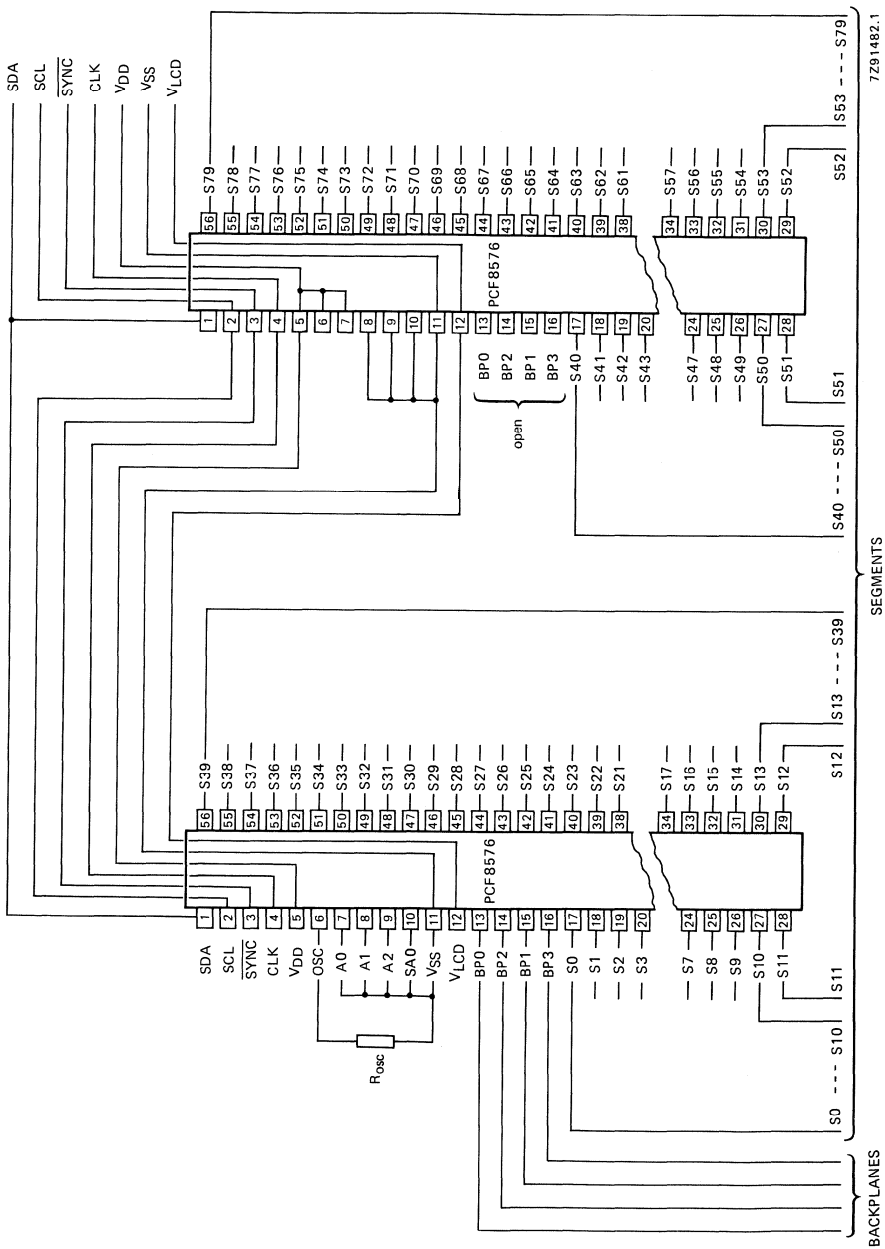


Fig. 26 Single plane wiring of packaged PCF8576s.

Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto the glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (Fig. 27). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between the V_{LCD} pad and the backplane output pads. The only bussed line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

Fig. 28 shows the connection diagram for a cascaded PCF8576 application with single plane wiring. Note the use of the open space between the V_{LCD} pad and the backplane output pads to route V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. The external connections may be made to either end of the cascade, wherever most convenient for the connector.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

APPLICATION INFORMATION (continued)

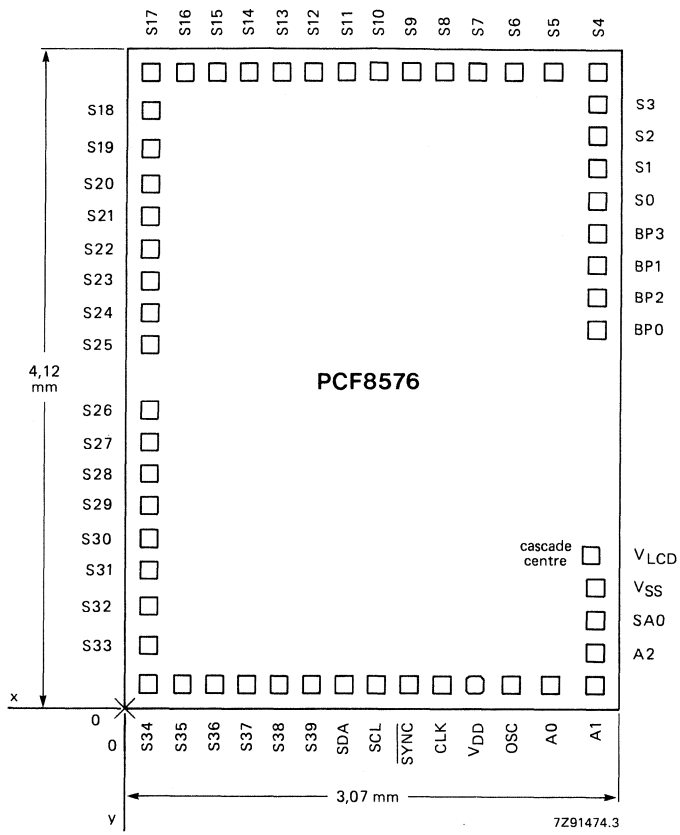


Fig. 27 PCF8576 bonding pad locations.

Bonding pad locations

All x/y coordinates are referenced to left-hand bottom corner (0/0, Fig. 27).

Dimensions in μm

pad	x	y	
S34	160	160	bottom
S35	380	↑	↑
S36	580		
S37	780		
S38	980		
S39	1180		
SDA	1380		
SCL	1580		
SYNC	1780		
CLK	1980		
V_{DD}	2180		
OSC	2400		
A0	2640	↓	↓
A1	2910	160	bottom
S17	160	3960	top
S16	380	↑	↑
S15	580		
S14	780		
S13	980		
S12	1180		
S11	1380		
S10	1580		
S9	1780		
S8	1980		
S7	2180		
S6	2400		
S5	2640		
S4	2910	3960	top

pad	x	y	
S33	160	400	left
S32	↑	640	↑
S31		860	
S30		1060	
S29		1260	
S28		1460	
S27		1660	
S26		1860	
S25		2260	
S24		2460	
S23		2660	
S22		2860	
S21		3060	
S20		3260	
S19		3480	
S18	160	3720	left
A2	2910	360	right
SA0	↑	560	↑
V_{SS}		760	
V_{LCD}		960	
BP0		2360	
BP2		2560	
BP1		2760	
BP3		2960	
S0		3160	
S1		3360	
S2		3560	
S3	2910	3760	right

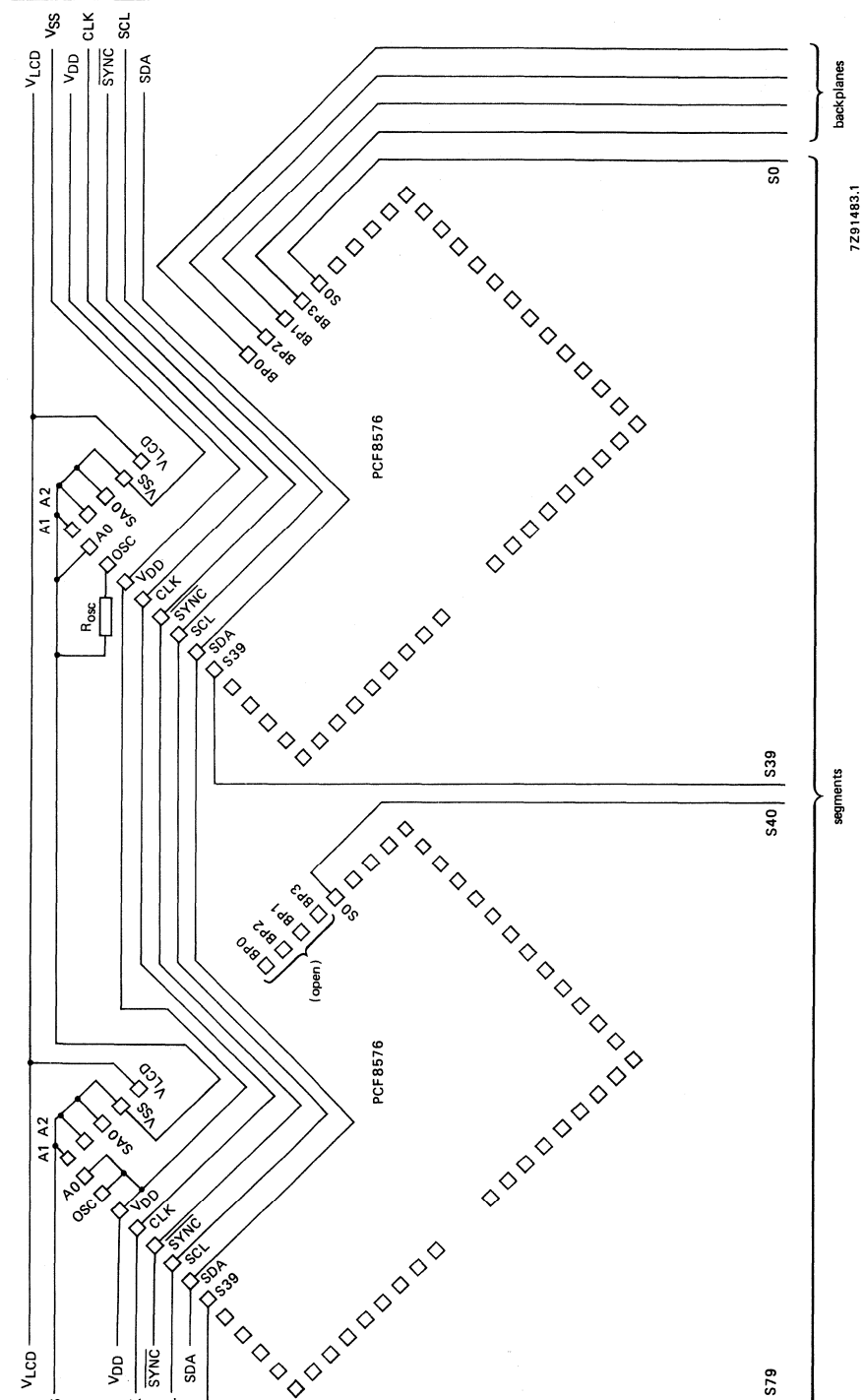
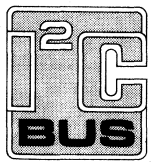


Fig. 28 Chip-on-glass application; cascaded PCF8576s with single-plane wiring (viewed from back of chip).



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

LCD DIRECT/DUPLEX DRIVER WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).

The PCF8577 and PCF8577A differ only in their slave address.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2,5 to 9 V
- Low power consumption
- I²C bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device sub-address boundaries
- Display memory switching in direct drive mode
- May be used for I²C bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A)
- Power-on-reset sets all segments off (to blank)

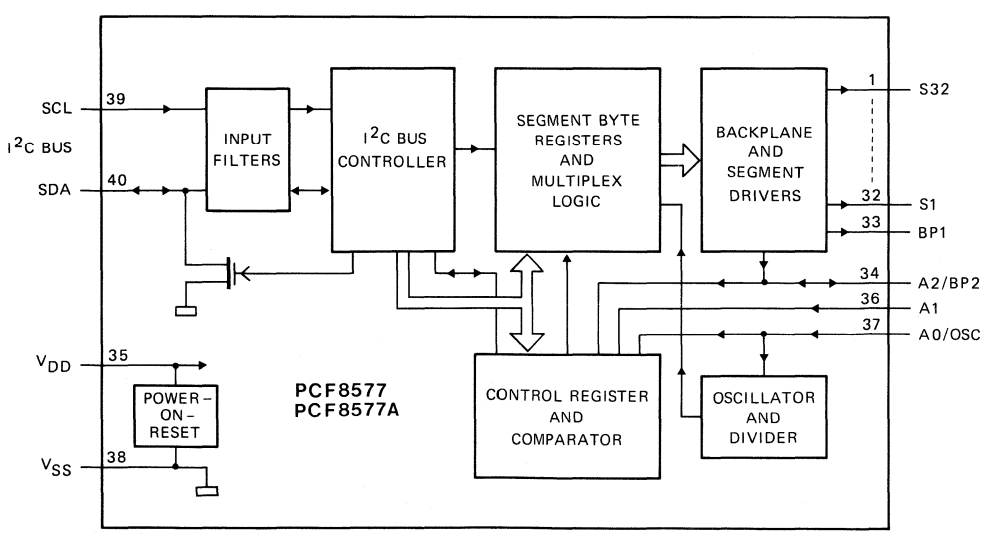


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8577P, PCF8577AP: 40-lead DIL; plastic (SOT-129).
PCF8577T, PCF8577AT: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

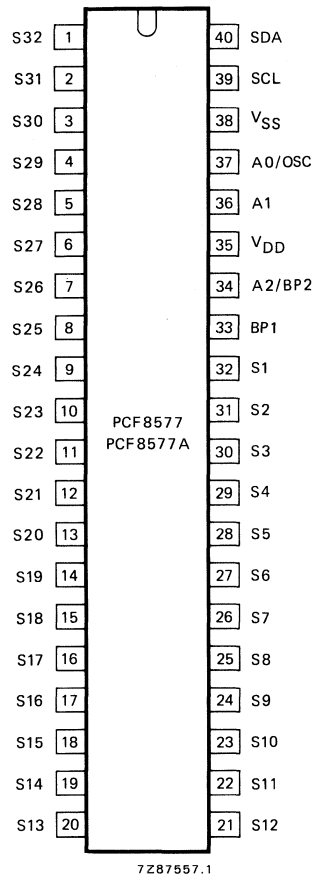


Fig. 2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C bus

40	SDA	I^2C bus data line
39	SCL	I^2C bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S1 – S32	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware sub-address A0, A1, A2

The hardware sub-address lines A0, A1, A2 are used to program the device sub-address for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577 the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the expansion mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the expansion mode each PCF8577 is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accesible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

There are two slave addresses, one for PCF8577, and one for PCF8577A (see Fig. 14). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I²C bus protocol Fig. 15).

The control register is shown in more detail in Fig. 3. The least-significant bits select which device and which segment byte register are loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware sub-address input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

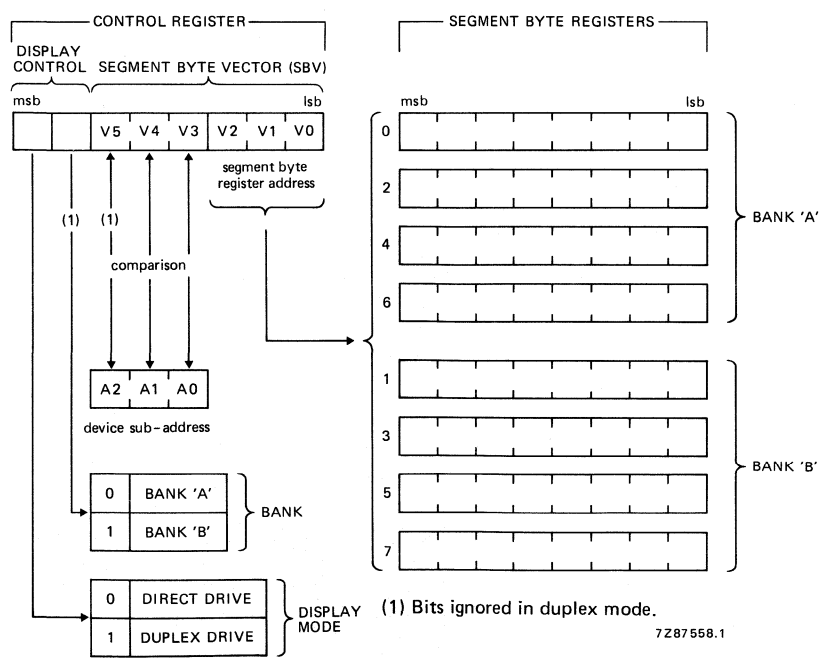


Fig. 3 PCF8577 register organization.

FUNCTIONAL DESCRIPTION (continued)

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

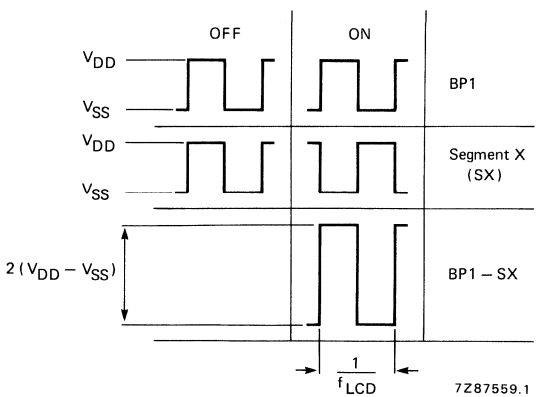
After each segment byte is loaded the SBV is incremented automatically, thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers, auto-incremented loading may proceed across device boundaries provided that the hardware sub-addresses are arranged contiguously.

Direct drive mode

The PCF8577 is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig. 4.



$V_{ON} = V_{DD} - V_{SS}$
$V_{OFF} = 0$

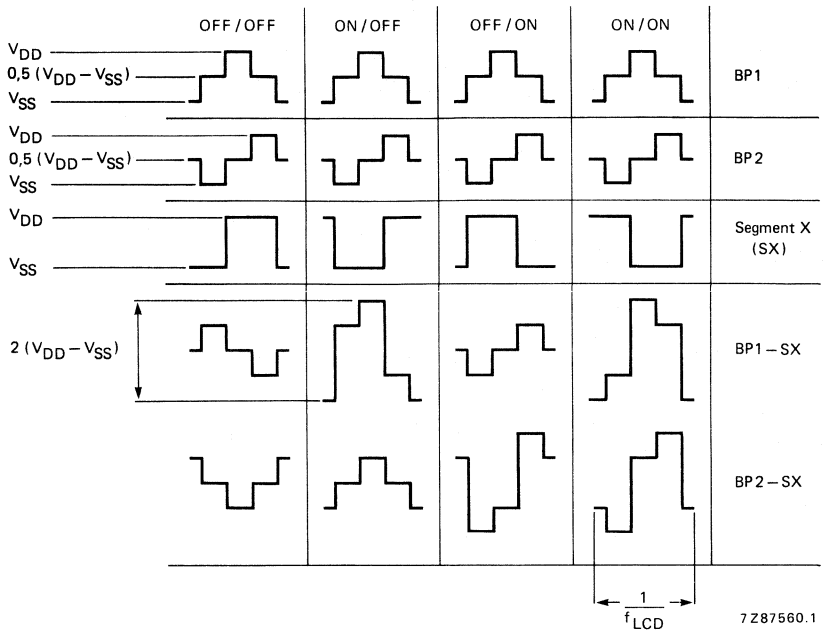
Fig. 4 Direct drive mode display output waveforms.

Duplex mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig. 5.



$$V_{ON} = 0{,}79\ (V_{DD} - V_{SS})$$

$$V_{OFF} = 0{,}35\ (V_{DD} - V_{SS})$$

$$\frac{V_{ON}}{V_{OFF}} = 2{,}26$$

Fig. 5 Duplex mode display output waveforms.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

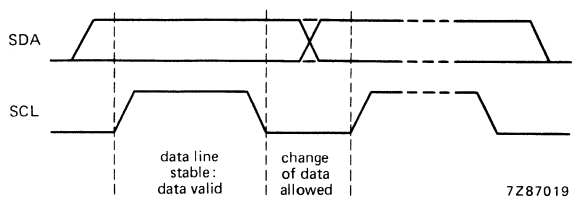


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

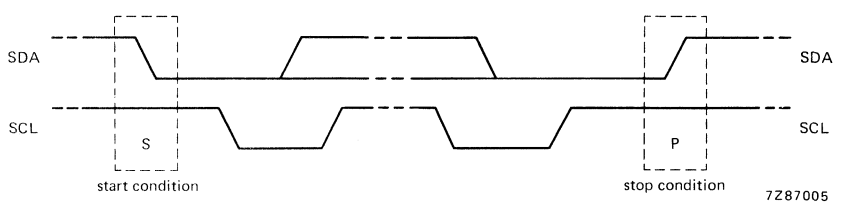


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

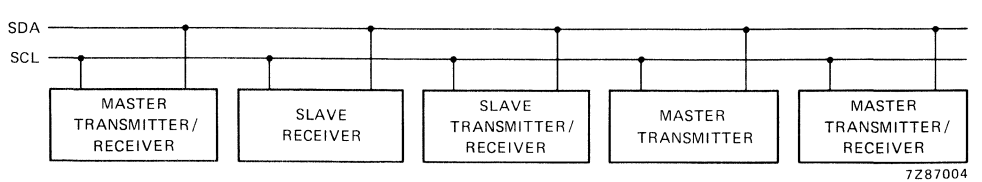


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

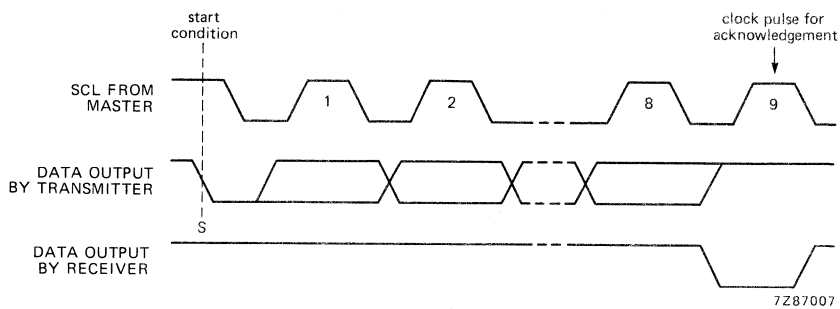


Fig. 9 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8577 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

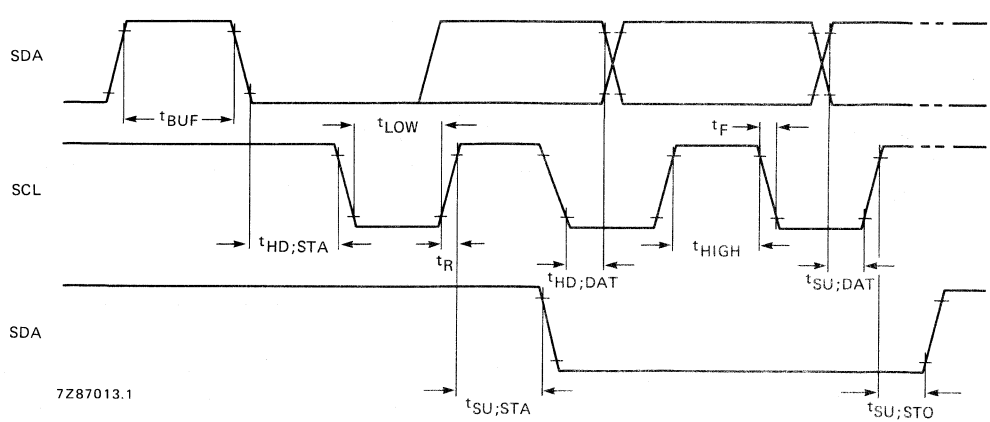


Fig. 10 Timing of the high-speed mode.

CHARACTERISTICS OF THE I²C BUS (continued)

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

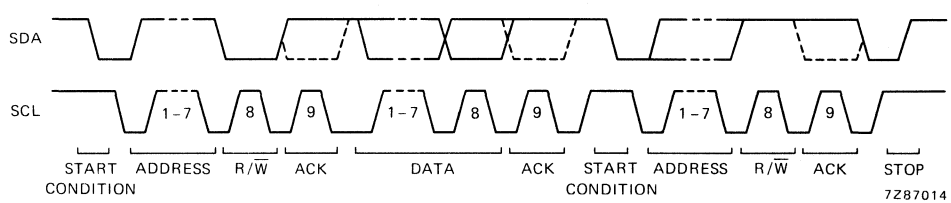


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

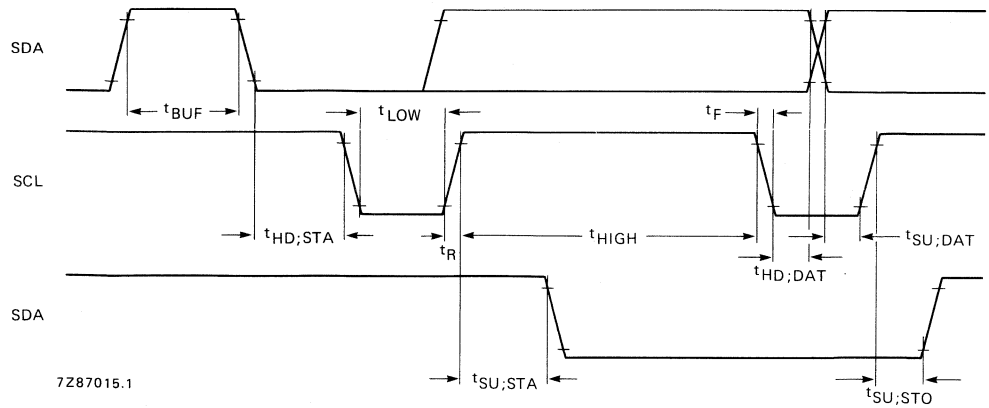


Fig. 12 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see high-speed mode.

* Only valid for repeated start code.

CHARACTERISTICS OF THE I²C BUS (continued)

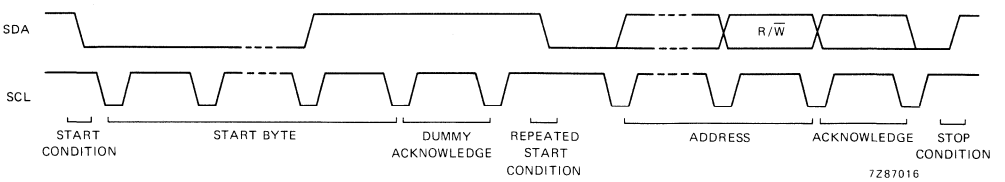


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

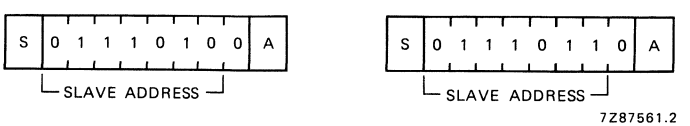
The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The slave address for PCF8577 and PCF8577A are shown in Fig. 14.



(a) PCF8577.

(b) PCF8577A.

Fig. 14 PCF8577 and PCF8577A slave addresses.

I²C bus protocol

The PCF8577 I²C bus protocol is shown in Fig. 15.

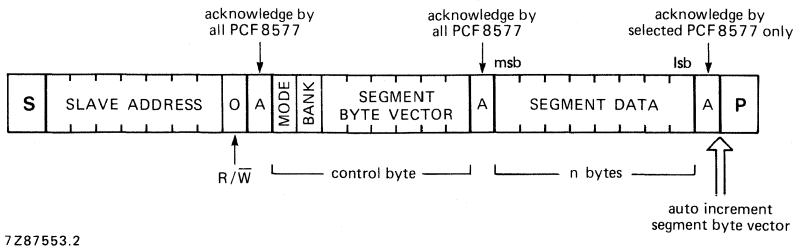


Fig. 15 I²C bus protocol.

The PCF8577 is a slave receiver and has a fixed slave address (Fig. 14). All PCF8577 on the same bus acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

DISPLAY MEMORY MAPPING

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode.

Table 1 Segment byte — segment driver mapping in the direct drive mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

DISPLAY MEMORY MAPPING (continued)

Even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2 Segment byte – segment driver mapping in the duplex mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	**BP1**
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	**BP2**
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	**BP1**
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	**BP2**
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	**BP1**
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	**BP2**
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	**BP1**
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	**BP2**

X = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to 11	V
Voltage on any pin	V_I	V_{SS} − 0,8 to V_{DD} + 0,8	V
D.C. input current	$\pm I_I$	max. 20	mA
D.C. output current	$\pm I_O$	max. 25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$, I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 500*	mW
Power dissipation per output	P	max. 100	mW
Operating ambient temperature range	T_{amb}	−40 to +85	°C
Storage temperature range	T_{stg}	−65 to +150	°C

* Derate 7,7 mW/K when $T_{amb} > 60$ °C.

CHARACTERISTICS

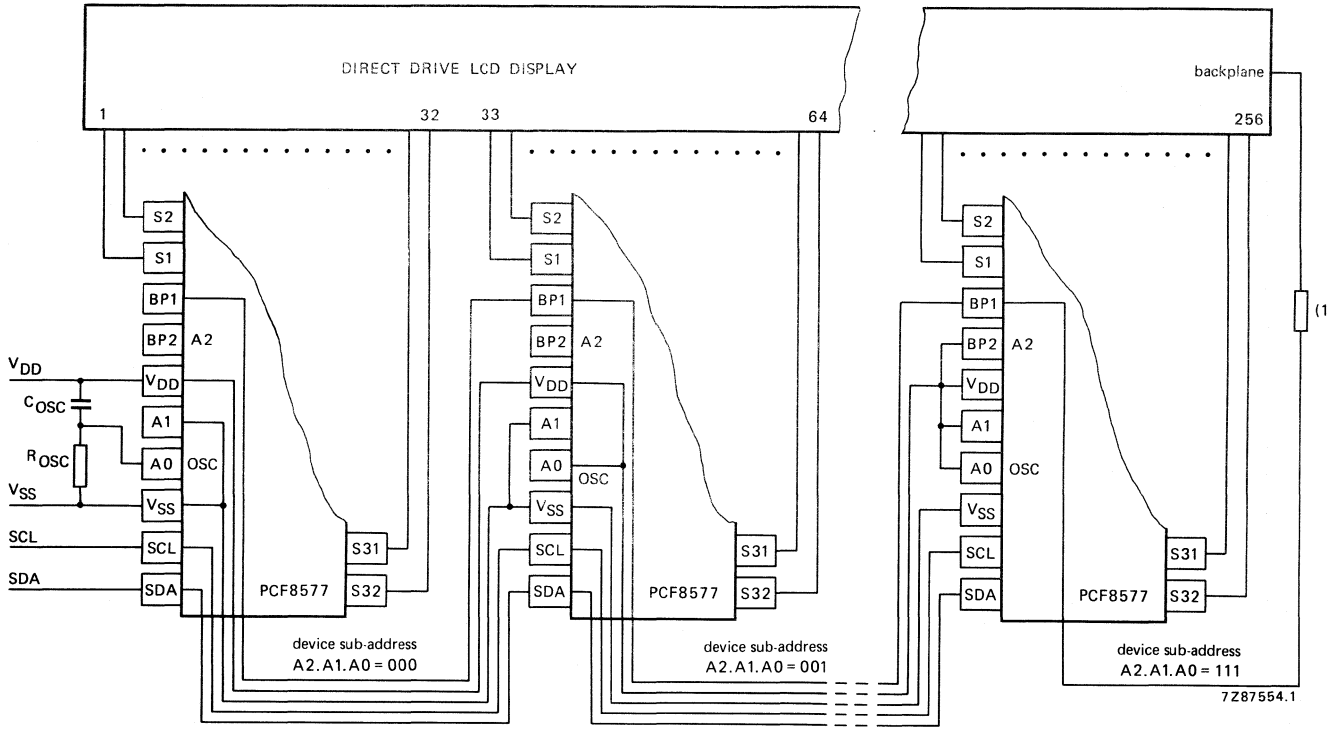
V_{DD} = 2,5 to 9 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.*	max.	unit
Supply voltage	V_{DD}	2,5	–	9,0	V
Supply current					
f_{SCL} = 100 kHz; no load; R_{OSC} = 1 MΩ	I_{DD}	–	80	250	μA
f_{SCL} = 0; no load; R_{OSC} = 1 MΩ; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD}	–	35	70	μA
Power-on-reset level**	V_{REF}	–	1,1	2,0	V
Input SCL; input/output SDA					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	9,0	V
output current LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA
output leakage current HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
tolerable spike width on bus	t_{sw}	–	–	100	ns
input capacitance at V_I = V_{SS}	C_I	–	–	7	pF
A1 input leakage current at V_I = V_{SS} or V_{DD}	I_I	–	–	250	nA
A2/BP2 input current at V_I = V_{DD}	I_I	–	2,0	–	μA
A0/OSC input current at V_I = V_{SS} or V_{DD}	$\pm I_I$	–	5,0	–	μA
DC component of LCD driver	$\pm V_{BP}$	–	20	–	mV
Segment loads	C_{SX}	–	–	5	nF
	R_{SX}	1	–	–	MΩ
Segment output current at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL}	0,3	–	–	mA
Segment output current at V_{OH} = V_{DD} − 0,4 V; V_{DD} = 5 V	$-I_{OH}$	0,3	–	–	mA
Backplane load (direct drive)	C_{BP}	–	–	50	nF
	R_{BP}	100	–	–	kΩ
Backplane loads (duplex drive)	C_{BP}	–	–	35	nF
	R_{BP}	100	–	–	kΩ
Rise and fall times (V_{BP} − V_{SX}) at maximum load	t_r, t_f	–	–	200	μs
Display frequency at C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz

* V_{DD} = 5 V; T_{amb} = 25 °C.

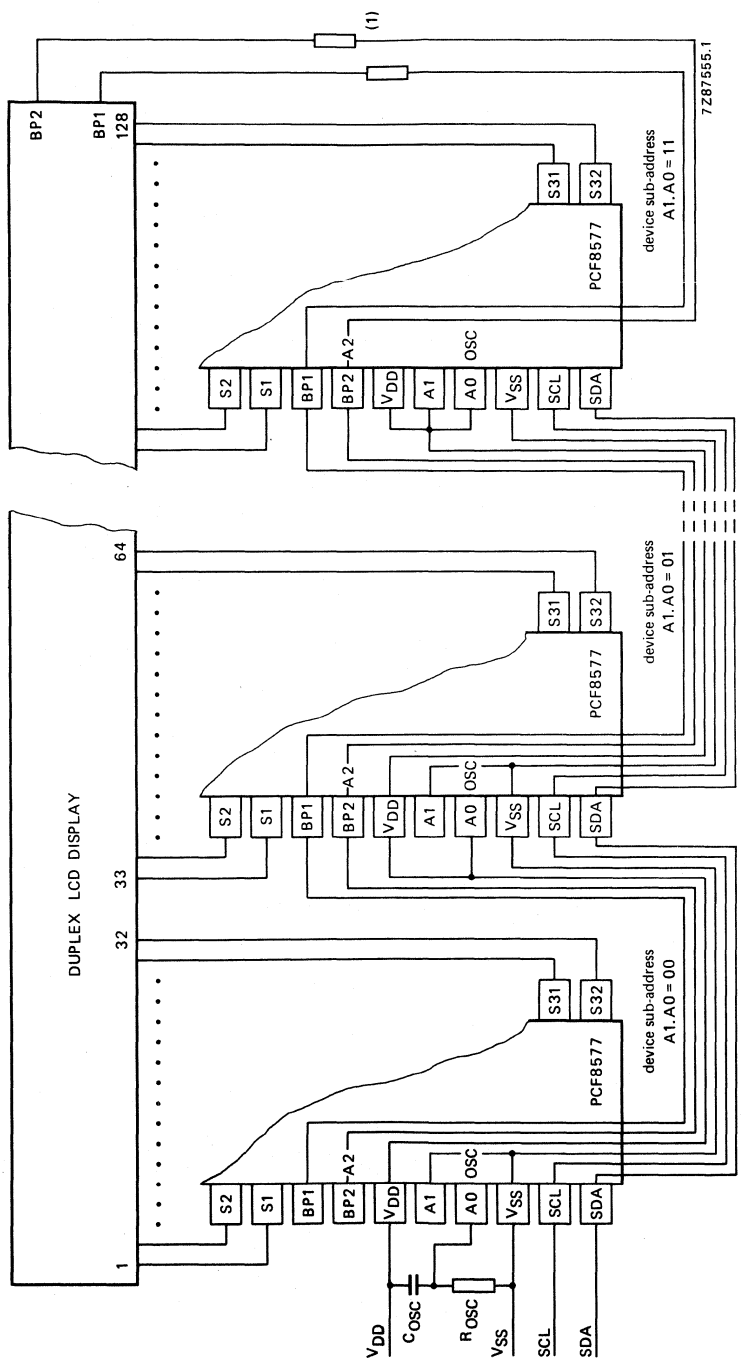
** The power-on-reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$.

APPLICATION INFORMATION



(1) The series resistance of the display backplane must be greater than 1 Ω.

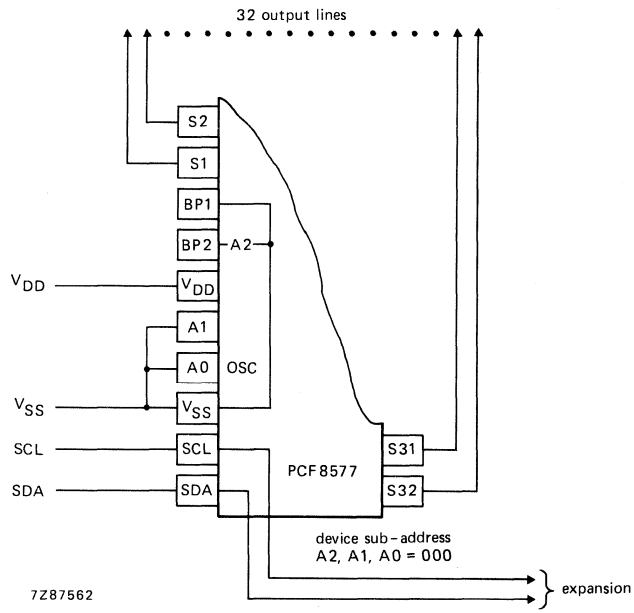
Fig. 16 Direct drive display; expansion to 256 segments using eight PCF8577.



(1) The series resistances of the display backplanes must be greater than 1 kΩ.

Fig. 17 Duplex display; expansion to 2 x 128 segments using four PCF8577.

APPLICATION INFORMATION (continued)



Notes

1. MODE bit must always be set to 0 (direct drive)
2. BANK switching is permitted
3. BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation)

Fig. 18 Use of PCF8577 as 32-bit output expander in I²C bus application.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

7-BIT ANALOGUE-TO-DIGITAL CONVERTER (ADC 7)

GENERAL DESCRIPTION

The PNA7509 is a monolithic NMOS 7-bit analogue-to-digital converter (ADC) designed for video applications. The device converts the analogue input signal into 7-bit binary coded digital words at a sampling rate of 22 MHz.

The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge triggered and can be switched into 3-state mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

Features

- 7-bit resolution
- Digitizing rates up to 22 MHz
- No external sample and hold required
- High input impedance
- Binary or two's complement 3-state TTL outputs
- Overflow and underflow 3-state TTL outputs
- Low reference current (250 μA typ.)
- Positive supply voltages (+ 5 V/+ 10 V)
- Low power consumption (400 mW typ.)
- Standard 24-pin package

Applications

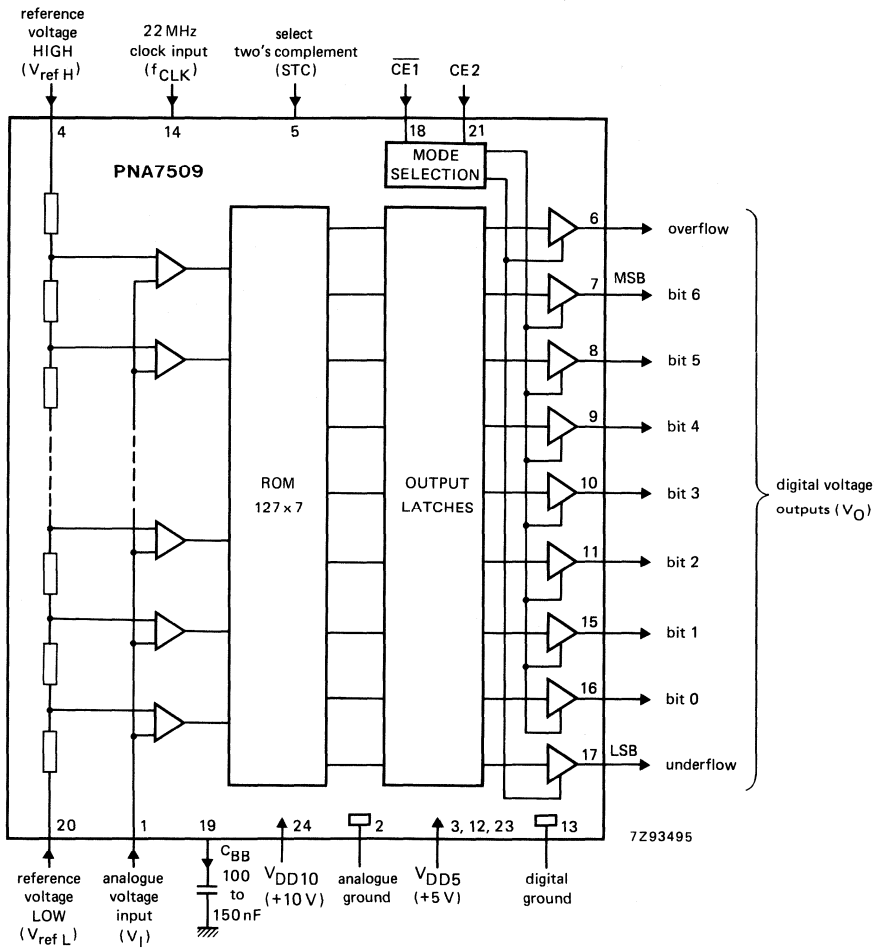
- High-speed A/D conversion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research

QUICK REFERENCE DATA

Supply voltage range (pins 3, 12, 23)	V_{DD5}	4,5 to 5,5		V
Supply voltage range (pin 24)	V_{DD10}	9,5 to 10,5		V
Supply current (pins 3, 12, 23)	I_{DD5}	typ.	60	mA
Supply current (pin 24)	I_{DD10}	typ.	10	mA
Reference voltage LOW (pin 20)	V_{refL}	min.	2,4	V
Reference voltage HIGH (pin 4)	V_{refH}	max.	5,2	V
Differential non-linearity		$\pm$ ½ $\triangleq$ 0,4%		LSB
Bandwidth (−3 dB)	B	min.	10	MHz
Clock frequency	f_{CLK}	max.	22	MHz
Total power dissipation	P_{tot}	typ.	400	mW

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101).



Note

All three pins 3, 12 and 23 must be connected to positive supply voltage + 5 V.

Fig. 1 Block diagram.

DEVELOPMENT DATA

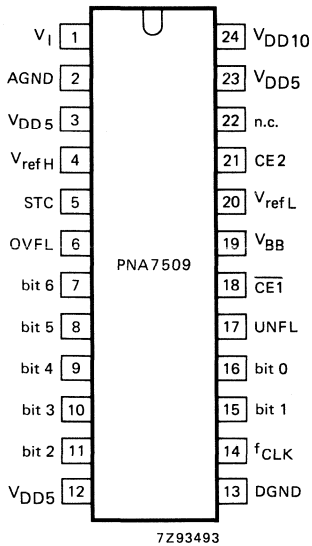


Fig. 2 Pinning diagram.

PINNING

1	V_I	analogue voltage input
2	AGND	analogue ground
3	V_{DD5}	positive supply voltage (+ 5 V)
4	V_{refH}	reference voltage HIGH
5	STC	select two's complement
6	OVFL	overflow
7	bit 6	most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD5}	positive supply voltage (+ 5 V)
13	DGND	digital ground
14	f_{CLK}	22 MHz clock input
15	bit 1	
16	bit 0	least-significant bit (LSB)
17	UNFL	underflow
18	$\overline{CE1}$	chip enable input 1
19	V_{BB}	back bias output
20	V_{refL}	reference voltage LOW
21	CE 2	chip enable input 2
22	n.c.	not connected
23	V_{DD5}	positive supply voltage (+ 5 V)
24	V_{DD10}	positive supply voltage (+ 10 V)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pins 3, 12, 23)	V_{DD5}	−0,5 to + 7	V
Supply voltage range (pin 24)	V_{DD10}	−0,5 to + 12	V
Input voltage range	V_I	−0,5 to + 7	V
Output current	I_O	5	mA
Total power dissipation	P_{tot}	tbf	mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

$V_{DD5} = V_{3, 12, 23-13} = 4{,}5$ to 5,5 V; $V_{DD10} = V_{24-2} = 9{,}5$ to 10,5 V; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pins 3, 12, 23)	V_{DD5}	4,5	–	5,5	V
Supply voltage (pin 24)	V_{DD10}	9,5	–	10,5	V
Supply current (pins 3, 12, 23)	I_{DD5}	–	60	–	mA
Supply current (pin 24)	I_{DD10}	–	10	–	mA
Reference voltages					
Reference voltage LOW (pin 20)	V_{refL}	2,4	2,5	2,6	V
Reference voltage HIGH (pin 4)	V_{refH}	5,0	5,1	5,2	V
Reference current	I_{ref}	175	250	375	μA
Inputs					
Clock input (pin 14)					
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
→ Input voltage HIGH	V_{IH}	3,0	–	V_{DD5}	V
Digital input levels (pins 5, 18, 21)*					
Input voltage LOW	V_{IL}	0	–	0,8	V
→ Input voltage HIGH	V_{IH}	2,0	–	V_{DD5}	V
Input current					
at $V_{5, 21-13} = 0$ V	$-I_{5, 21}$	–	–	100	μA
at $V_{18-13} = 5$ V	I_{18}	–	–	100	μA
Input leakage current (except pins 5, 18 and 21)	I_{LI}	–	–	10	μA
Analogue input levels (pin 1) at $V_{refL} = 2{,}5$ V; $V_{refH} = 5{,}1$ V					
Input voltage amplitude (peak-to-peak value)	$V_{I(p-p)}$	–	2,6	–	V
Input voltage (underflow)	V_I	–	2,5	–	V
Input voltage (overflow)	V_I	–	5,1	–	V
Offset input voltage (underflow)	$V_I - V_{refL}$	–	10	–	mV
Offset input voltage (overflow)	$V_I - V_{refH}$	–	−10	–	mV
Input capacitance	C_{1-2}	–	–	60	pF

* When pin 5 is LOW binary coding is selected.
When pin 5 is HIGH two's complement is selected.
If pin 5, 18 and 21 are open-circuit, pin 5, 21 are HIGH and pin 18 is LOW.
For output coding see Table 1 and mode selection see Table 2.

parameter	symbol	min.	typ.	max.	unit
Outputs					
Digital voltage outputs (pins 6 to 11 and 15 to 17)					
Output voltage LOW at I_O = 2 mA	V_{OL}	0	–	–0,4	V
Output voltage HIGH at $-I_O$ = 0,5 mA	V_{OL}	2,4	–	V_{DD5}	V

Table 1 Output coding (V_{refL} = 2,5 V; V_{refH} = 5,1 V)

step	V_{1-2} (typ.)	UNFL	OVFL	binary bit 6 – bit 0	two's complement bit 6 – bit 0
underflow	< 2,51	1	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
0	2,51	0	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
1	2,53	0	0	0 0 0 0 0 0 1	1 0 0 0 0 0 1
.	.	.	.	. . . .	. . . .
.	.	.	.	. . . .	. . . .
.	.	.	.	. . . .	. . . .
126	5,03	0	0	1 1 1 1 1 1 0	0 1 1 1 1 1 0
127	5,05	0	0	1 1 1 1 1 1 1	0 1 1 1 1 1 1
overflow	⩾ 5,07	0	1	1 1 1 1 1 1 1	0 1 1 1 1 1 1

steps 2-125

DEVELOPMENT DATA

Table 2 Mode selection

CE 1	CE 2	bit 0 to bit 6	UNFL, OVFL
X	0	HIGH impedance	HIGH impedance
0	1	active	active
1	1	HIGH impedance	active

CHARACTERISTICS (continued)

$V_{DD5} = V_{3, 12, 23\text{-}13} = 4{,}5$ V to 5,5 V; $V_{DD10} = V_{24\text{-}2} = 9{,}5$ V to 10,5 V; $V_{refL} = 2{,}5$ V; $V_{refH} = 5{,}1$ V; $f_{CLK} = 22$ MHz; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Timing (see also Fig. 3)					
Clock input (pin 14)					
Clock frequency	f_{CLK}	1	–	22	MHz
Clock cycle time LOW	t_{LOW}	20	–	–	ns
Clock cycle time HIGH	t_{HIGH}	20	–	–	ns
Input rise and fall times (note 1)					
rise time	t_r	–	–	3	ns
fall time	t_f	–	–	3	ns
Analogue input (note 1)					
Bandwidth (–3 dB)					
at $V_{1\text{-}2(p\text{-}p)} = 2{,}2$ V	B	10	–	–	MHz
Differential gain					
at $f_i = \leqslant 4{,}5$ MHz (note 2)	dG	–	–	5	%
Differential phase					
at $f_i = \leqslant 4{,}5$ MHz (note 2)	d_p	–	–	5	deg
Phase error					
at $f_i = \leqslant 4{,}5$ MHz (note 3)	P_e	–	–	± 10	deg
Signal-to-noise ratio					
at $V_{1\text{-}2(p\text{-}p)} = 2{,}2$ V; $f_i = \leqslant 4{,}5$ MHz; B = ± 1 MHz	S/N	36	–	–	dB
Harmonics					
at $V_{1\text{-}2(p\text{-}p)} = 2{,}2$ V; $f_i = 3{,}6$ MHz					
fundamental	f_0	–	0	0	dB
2nd harmonic	f_{2nd}	–	–	tbf	dB
3rd harmonic	f_{3rd}	–	–	tbf	dB
4th harmonic	f_{4th}	–	–	tbf	dB
5th harmonic	f_{5th}	–	–	tbf	dB
6th harmonic	f_{6th}	–	–	tbf	dB
7th harmonic	f_{7th}	–	–	tbf	dB

parameter	symbol	min.	typ.	max.	unit
Harmonics at $V_{1\text{-}2(p\text{-}p)}$ = 2,2 V; f_i = 4,5 MHz					
fundamental	f_0	–	0	0	dB
2nd harmonic	f_{2nd}	–	–	tbf	dB
3rd harmonic	f_{3rd}	–	–	tbf	dB
4th harmonic	f_{4th}	–	–	tbf	dB
5th harmonic	f_{5th}	–	–	tbf	dB
6th harmonic	f_{6th}	–	–	tbf	dB
7th harmonic	f_{7th}	–	–	tbf	dB
Digital outputs (notes 2 and 4)					
Output hold time	t_{HOLD}	6	15	–	ns
Output delay time	t_d	–	20	28	ns
Internal delay	t_{CY}	–	3	–	clocks
Propagation delay time at f_{CLK} = 20,25 MHz	t_{pd}	154	–	176	ns
3-state delay time (see Fig. 4)	t_{dt}	tbf	10	20	ns
Capacitive output load (note 2)	C_{OL}	0	–	15	pF
Transfer function					
Non-linearity					
integral	INL	–	–	± 1	LSB
differential	DNL	–	–	± ½ ≙ 0,4%	LSB

DEVELOPMENT DATA

Notes to timing characteristics

1. Clock input rise and fall times are at the maximum clock frequency (10% and 90% levels).
2. Low frequency sinewave (peak-to-peak value of the analogue input voltage at $V_{I(p\text{-}p)}$ = 1,8 V) amplitude modulated with a sinewave voltage ($V_{I(p\text{-}p)}$ = 0,7 V) at $f_i \leqslant$ 4,5 MHz.
3. Sinewave voltage with increasing amplitude at $f_i \leqslant$ 4,5 MHz (minimum amplitude $V_{I(p\text{-}p)}$ = 0,25 V; maximum amplitude $V_{I(p\text{-}p)}$ = 2,5 V).
4. The timing values of the digital outputs at pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1,5 V.

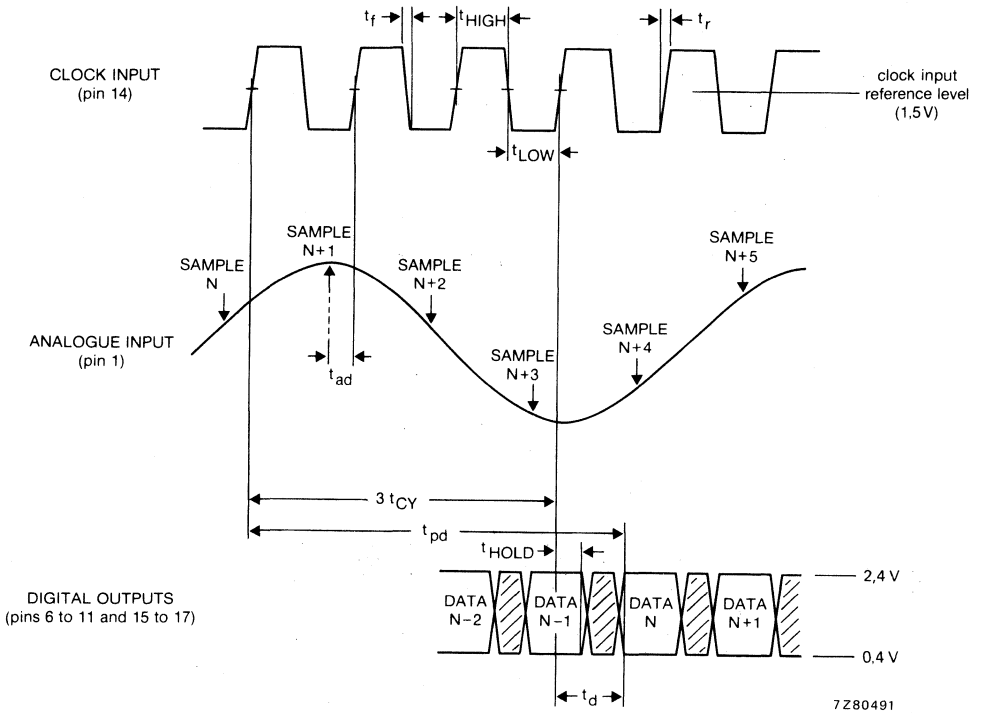


Fig. 3 Timing diagram.

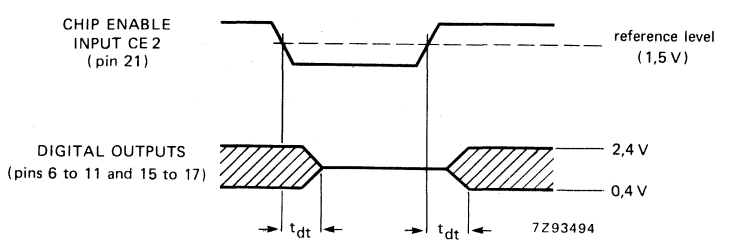


Fig. 4 Timing diagram for 3-state delay.

8-BIT MULTIPLYING DAC

GENERAL DESCRIPTION

The PNA7518 is a NMOS 8-bit multiplying digital-to-analogue converter (DAC) designed for video applications. The device converts a digital input signal into a voltage-equivalent analogue output at a sampling rate of 30 MHz.

The input signal is latched, then fed to a decoder which switches a transfer gate array (1 out of 256) to select the appropriate analogue signal from a resistor chain. Two external reference voltages supply the resistor chain.

The input latches are positive-edge triggered. The output impedance is approximately 0,5 kΩ depending on the applied digital code. An additional operational amplifier is required for the 75 Ω output impedance. Two's complement is selected when STC (pin 11) is HIGH or is not connected.

Features

- TTL input levels
- Positive-edge triggered
- Analogue voltage output at 30 MHz sampling rate
- Binary or two's complement input
- Output voltage accuracy to within ± ½ of the input LSB

QUICK REFERENCE DATA

Supply voltage range (pin 16)	V_{DD}	4,5 to 5,5	V
Supply current (pin 16)	I_{DD} typ.	50	mA
Reference voltage LOW (pin 2)	V_{refL} min.	0	V
Reference voltage HIGH (pin 9)	V_{refH} max.	2	V
Linearity at R_L = 200 kΩ; V_O = 2 V (peak-to-peak value)		± ½	LSB
Bandwidth (−3 dB) at C_L = 6 pF	B min.	12	MHz
Clock frequency	f_{CLK} max.	30	MHz
Total power dissipation	P_{tot} typ.	300	mW

Applications

- Video data conversion
- CRT displays
- Waveform/test signal generation
- Colour/black-and-white graphics

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38WE-1).

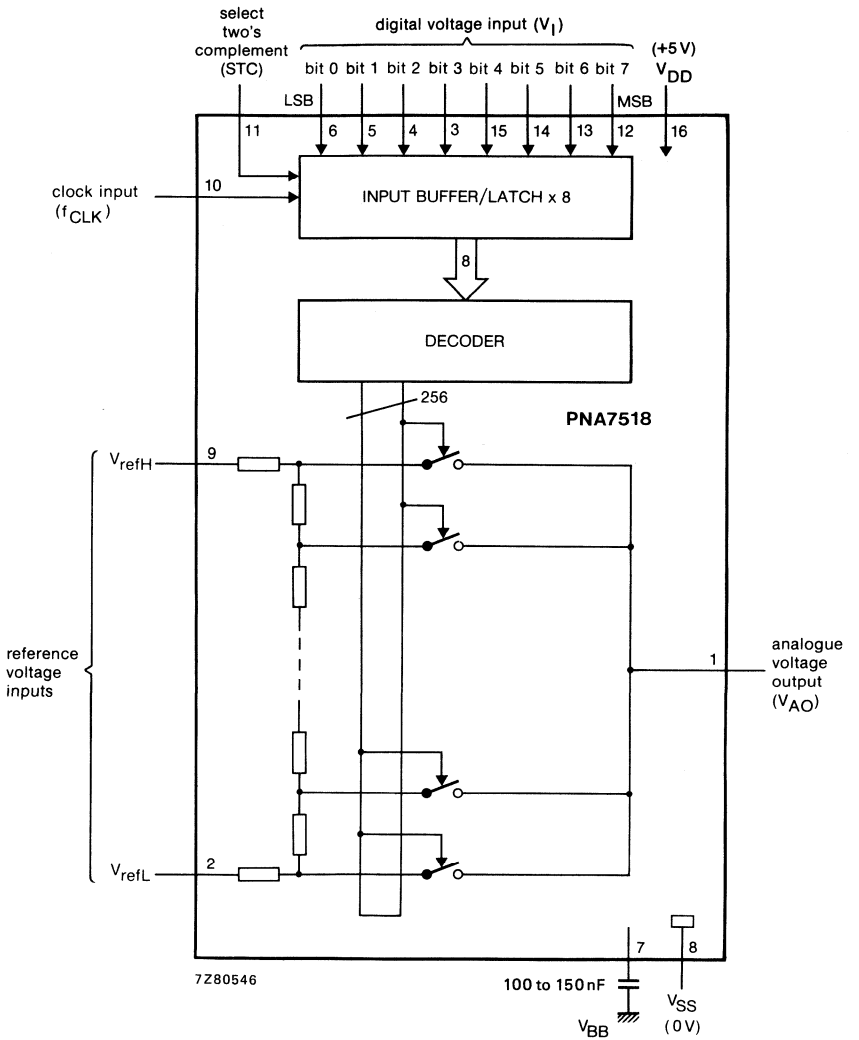


Fig. 1 Block diagram.

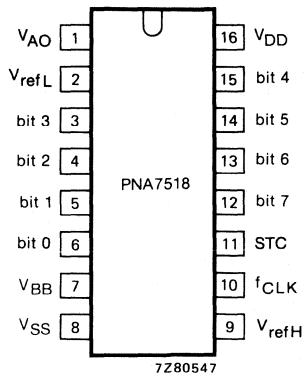


Fig. 2 Pinning diagram.

PINNING

1	V_{AO}	analogue output voltage
2	V_{refL}	reference voltage LOW
3	bit 3	digital voltage inputs (V_I)
4	bit 2	
5	bit 1	
6	bit 0	least-significant bit (LSB)
7	V_{BB}	back bias
8	V_{SS}	ground
9	V_{refH}	reference voltage HIGH
10	f_{CLK}	clock input
11	STC	select two's complement
12	bit 7	most-significant bit (MSB)
13	bit 6	digital voltage inputs (V_I)
14	bit 5	
15	bit 4	
16	V_{DD}	positive supply voltage

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 16)	V_{DD}	−0,5 to + 7 V
Input voltage range (pins 3, 4, 5, 6, 11, 12, 13, 14 and 15)	V_I	−0,5 to + 7 V
Output voltage range (pin 1)	V_{AO}	−0,5 to + 7 V
Total power dissipation	P_{tot}	max. 400 mW
Storage temperature range	T_{stg}	−65 to + 150 °C
Operating ambient temperature range	T_{amb}	0 to + 70 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

V_{DD} = 4,5 to 5,5; V_{SS} = 0 V; C_{BB} = 100 nF; T_{amb} = 0 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{DD}	4,5	5	5,5	V
Supply current	I_{DD}	–	50	80	mA
Reference voltages					
Reference voltage LOW (pin 2)	V_{refL}	−0,1	–	+ 2,1	V
Reference voltage HIGH (pin 9)	V_{refH}	−0,1	–	+ 2,1	V
Reference ladder	R_{ref}	150	230	300	Ω
Inputs					
Digital input levels (TTL) (note 1)					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	5,25	V
input leakage current	I_{LI}	–	–	10	μA
Clock input (pin 10)					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	5,25	V
input leakage current	I_{LI}	–	–	10	μA
frequency	f_{CLK}	1	–	30	MHz
pulse width HIGH	t_{PWH}	10	–	–	ns
pulse width LOW	t_{PWL}	10	–	–	ns
input rise time at f_{CLK} = 30 MHz	t_r	–	–	3	ns
input fall time at f_{CLK} = 30 MHz	t_f	–	–	3	ns
Output					
Analogue voltage output (pin 1) at R_L = 200 kΩ)	V_{AO}	0	–	2	V
Bandwidth (−3 dB) at C_L = 6 pF	B	12	18	–	MHz
Switching characteristics (Fig. 3)					
Data set-up time	$t_{SU;DAT}$	3	–	–	ns
Data hold time	$t_{HD;DAT}$	4	–	–	ns
Propagation delay time, input to output	t_{PD}	t_{CLK} + 15	t_{CLK} + 22	t_{CLK} + 30	ns
Settling time: 10 to 90% full-scale change; C_L = 6 pF; R_L = 200 kΩ	t_{S1}	–	13	20	ns
Settling time to ± 1 LSB; C_L = 6 pF; R_L = 200 kΩ	t_{S2}	–	40	–	ns

parameter	symbol	min.	typ.	max.	unit
Output transients (glitches) (note 2 and Fig. 3)					
1 LSB change:					
Maximum occurring at step 7F-80 (HEX)		–	3	–	LSB
area amplitude	V_g	–	23	–	LSB.ns
Generally:					
Maximum occurring at step 00-AA (HEX)		–	5	–	LSB
are amplitude	V_g	–	41	–	LSB.ns
Influence of clock frequency (note 2)					
Cross-talk at 2 x f_{CLK}					
amplitude		–	2	–	LSB
area		–	8	–	LSB.ns

Notes to the characteristics

1. Inputs bit 0 to bit 7 are positive-edge triggered.
2. Measured at V_{refH}-V_{refL} = 2,0 V; 1 x LSB = 7,8 mV. The energy equivalent of output transients is given as the area contained by the graph of output amplitude (LSB) against time (ns). The glitch area is independent of the value of V_{ref}. Glitch amplitudes and clock cross-talk can be reduced by using a shielded printed circuit board.

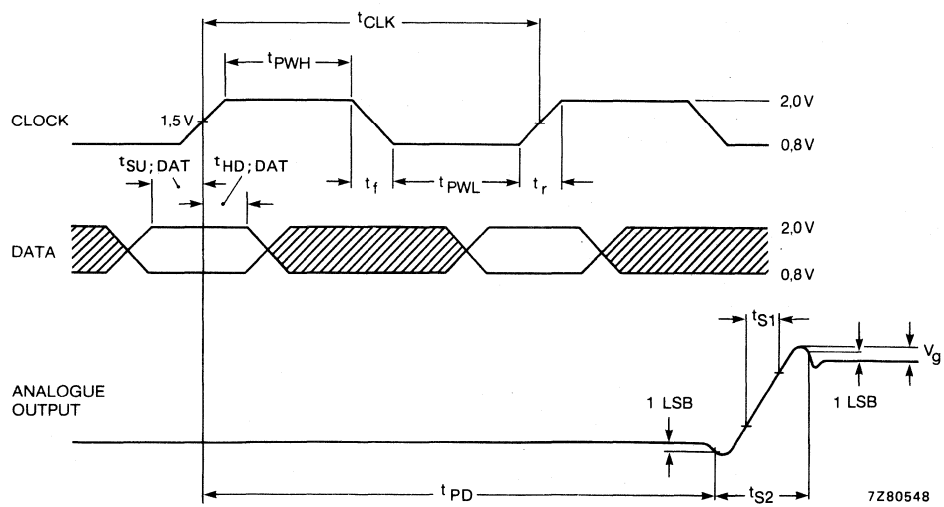


Fig. 3 Switching characteristics.

UNIVERSAL SYNC GENERATOR

GENERAL DESCRIPTION

The SAA1043 generates the synchronizing waveforms required in all types of video source equipment (video cameras, film-scanners, video games, computer displays and similar applications). The device is programmable to suit standards SECAM 1, SECAM 2, PAL/CCIR, NTSC 1, NTSC 2, and PAL-M; the video game 624 and 524-line standards; and can be synchronized to an external sync signal. Inputs and outputs are CMOS compatible.

Features

- Programmable to eight standards
- Horizontal frequency manipulation for application in non-standard systems
- Oscillator functions with LC or crystal elements
- Additional outputs to simplify camera signal processing
- Can be synchronized to an external sync signal
- Vertical reset for fast vertical lock
- Subcarrier lock in combination with subcarrier coupler SAA1044
- Very low power consumption

QUICK REFERENCE DATA

Supply voltage range (pin 28)	V_{DD}	5,7 to 7,5	V
Supply current (quiescent)	I_{DD}	max. 10	μA
Oscillator frequency	f_{OSCI}	max. 5,1	MHz

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

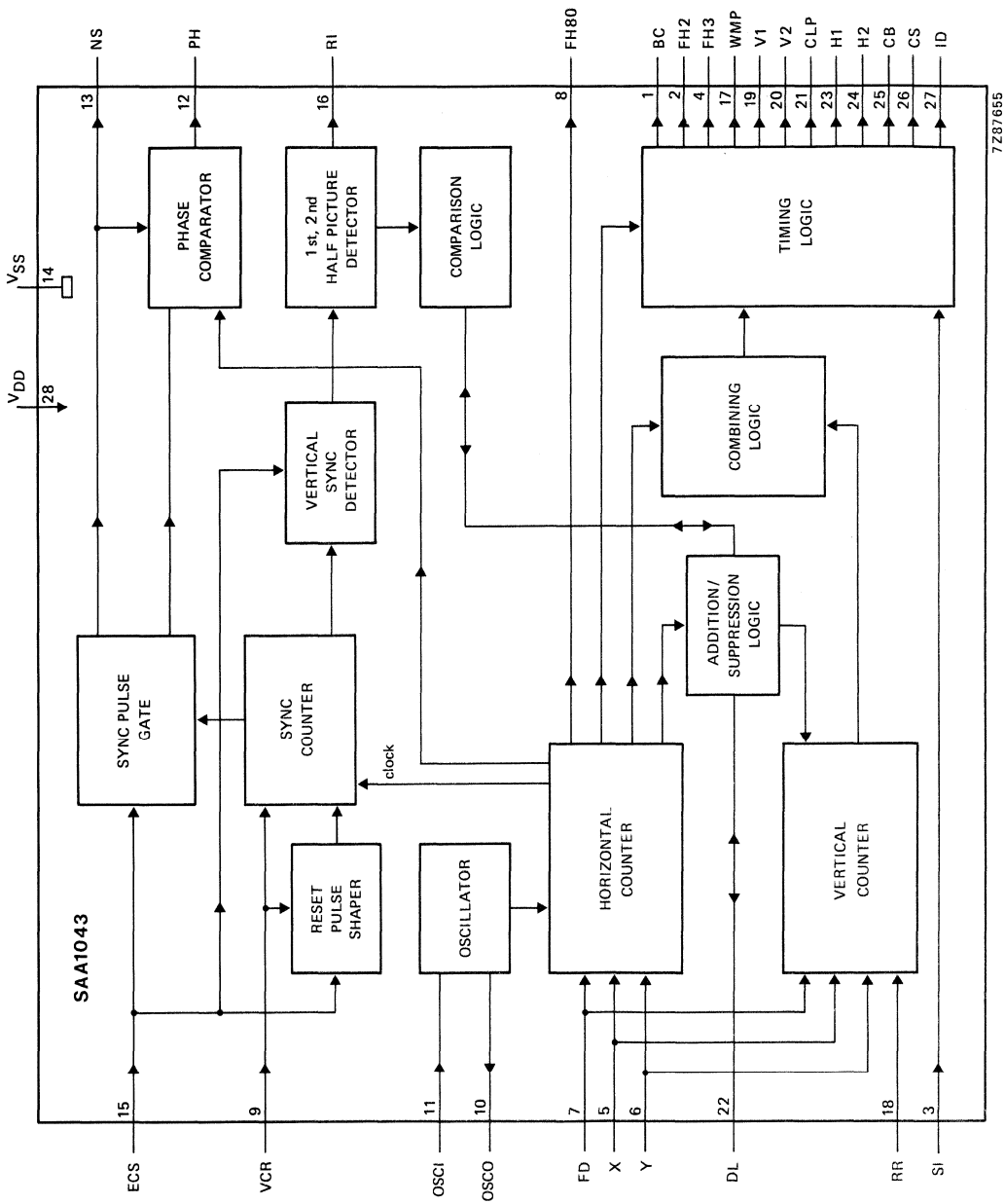


Fig. 1 Block diagram.

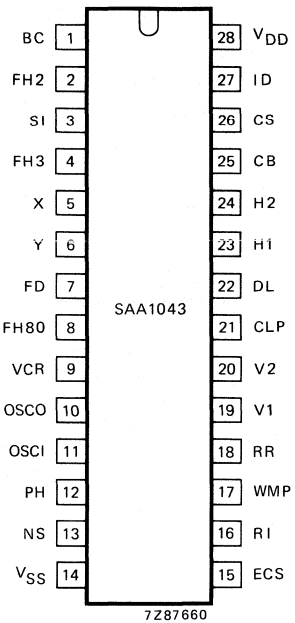


Fig. 2 Pinning diagram.

PINNING

1	BC	burst flag/chroma blanking (SECAM) output
2	FH2	PAL identification output
3	SI	set identification input (SECAM, PAL, PAL-M)
4	FH3	400 Hz (PAL); 360 HZ (NTSC, PAL-M) and $f_H/3$ (SECAM)
5	X	standard programming input
6	Y	standard programming input
7	FD	standard programming input
8	FH80	80 x f_H output (1,25 MHz)
9	VCR	VCR standard input
10	OSCO	oscillator output
11	OSCI	oscillator input
12	PH	phase detector output
13	NS	no-sync detector output
14	V_{SS}	negative supply voltage (ground)
15	ECS	external composite sync input
16	RI	vertical identification output
17	WMP	white measurement pulse output
18	RR	vertical reset input
19	V1	vertical drive output
20	V2	vertical drive output
21	CLP	clamp pulse output
22	DL	2 x f_H input/output
23	H1	horizontal drive output
24	H2	horizontal drive output
25	CB	composite blanking output
26	CS	composite sync output
27	ID	SECAM identification output
28	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Sync pulse generation

Programming of operating standard

The standard required for operation is programmed using the inputs X, Y and FD as shown in Table 1. The FD input selects 525 or 625-line working of the vertical counter (524 or 624-lines for video game standards) and also influences the choice of oscillator frequency as shown in Table 2.

Table 1 Programming of operating standard

standard	FD	X	Y
SECAM 1	0	0	0
SECAM 2	0	0	1
624	0	1	0
PAL/CCIR	0	1	1
NTSC 1	1	0	0
NTSC 2	1	0	1
524	1	1	0
PAL-M	1	1	1

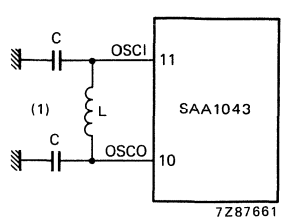
positive logic: 1 = HIGH; 0 = LOW

Oscillator

The built-in oscillator of the SAA1043 functions with an external LC-circuit (Fig. 3) or with a crystal of the parallel resonance type (Fig. 4). For operation in the VCR mode the LC oscillator circuit is recommended. The frequencies required for the operating standards are shown in Table 2.

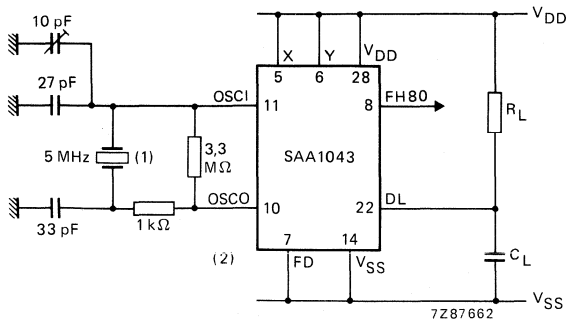
Table 2 Oscillator input frequencies

operating standard	osc. frequency (f_{OSCI}) MHz	vertical divider (FD)	vertical frequency (f_V) Hz	horizontal frequency (f_H) Hz
PAL, SECAM, 624	5,0	0	50	15625
NTSC, PAL-M, 524	5,034964	1	59,94	15734,26
PAL, SECAM, 624	2,5	H2 (pin 24)	50	15625
NTSC, PAL-M, 524	2,501748	H1 (pin 23)	59,94	15734,26



(1) Component values can be calculated from the formula $f_{OSCI} = 1/2\pi\sqrt{LC_V}$ where $C_V = C/2 + C_p$ and C_p = parasitic capacitance of typically 5 pF.

Fig. 3 LC oscillator circuit.



(1) Catalogue number of crystal: 8222 298 40760.

(2) All inputs not shown are at V_{SS}.

Fig. 4 Crystal oscillator circuit showing test set-up for oscillator frequency measurement.

Synchronization to an external sync signal

Use is made of the phase comparator output PH to lock the internally generated sync pulses to an external sync signal. Reset pulses derived at each falling edge of the external sync signal (ECS) reset the the sync counter which is clocked at the internal horizontal frequency by the horizontal counter. At each horizontal scan period the sync counter opens the sync pulse gate and allows the ECS to be applied to the phase comparator where it is compared with the phase of the internally generated horizontal sync pulse. When the two signals are in phase the output PH is in a high impedance state. When a phase difference exists PH is pulled towards V_{DD} or V_{SS} depending on the direction of the error (Fig. 5). The phase-analogue voltage on PH is used to correct the frequency at OSCI via a voltage-controlled oscillator and null the phase error between internal and external signals. Pulses occurring on the ECS outside of the sync pulse gating time (serration and equalization pulses) do not effect the phase comparator.

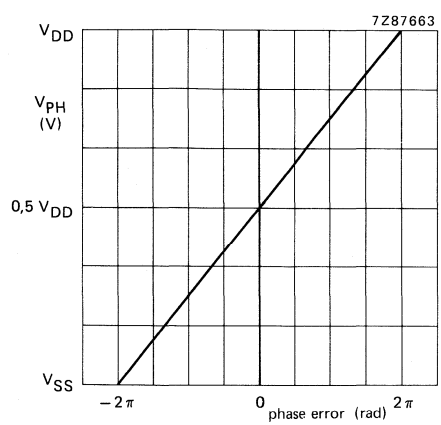


Fig. 5 Phase comparator characteristic.

FUNCTIONAL DESCRIPTION (continued)

Synchronization to an external sync signal (continued)

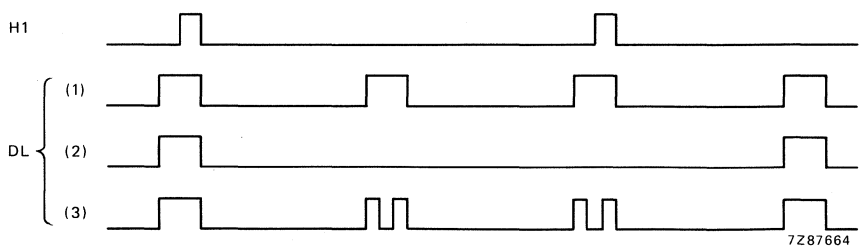
The circuit will lock to standard and non-standard sync signals. With standard signals the resetting of the sync counter is permitted after 3/4 of the horizontal scan period and if one reset pulse is missed the next pulse will reset the counter. With non-standard signals a narrow reset window is imposed to avoid disturbances which would otherwise be visible on the screen during vertical blanking time. The width of this window is $64 - 15{,}2 <$ reset time $< 64 + 15{,}2$ μs. If a reset pulse does not occur within this window the same window timing is specified for the next horizontal scan.

A no-sync signal is generated by the sync pulse gate if the sync counter is not reset from the ECS. The no-sync signal (NS) occurs 6,4 μs after the time of the missing reset pulse.

Detection of the vertical sync in the ECS is performed using a double sampling method which minimizes detection failures. Vertical lock is performed by comparing the internal vertical sync with a pulse derived from the ECS and using the result to modify the period of the vertical counter. This is achieved by manipulating the DL ($2 \times f_H$) input to the vertical counter via the addition/subtraction logic. The DL pulses are added or suppressed to bring the circuit into lock in the shortest possible time; the direction taken is determined by a logic decision based on the half picture in which the ECS derived pulse occurred.

Use in non-standard systems

For systems requiring a non-standard horizontal frequency the number of horizontal scans per picture can be manipulated using the open drain input/output DL. The addition or suppression of pulses during the high ohmic period of DL modifies the vertical counter value. The suppression of two DL pulses per half picture will give one extra horizontal scan and the addition of two DL pulses will remove one horizontal scan from the half picture (see Fig. 6).



(1) Normal waveform at DL; $f_{DL} = 2 \times f_H$.

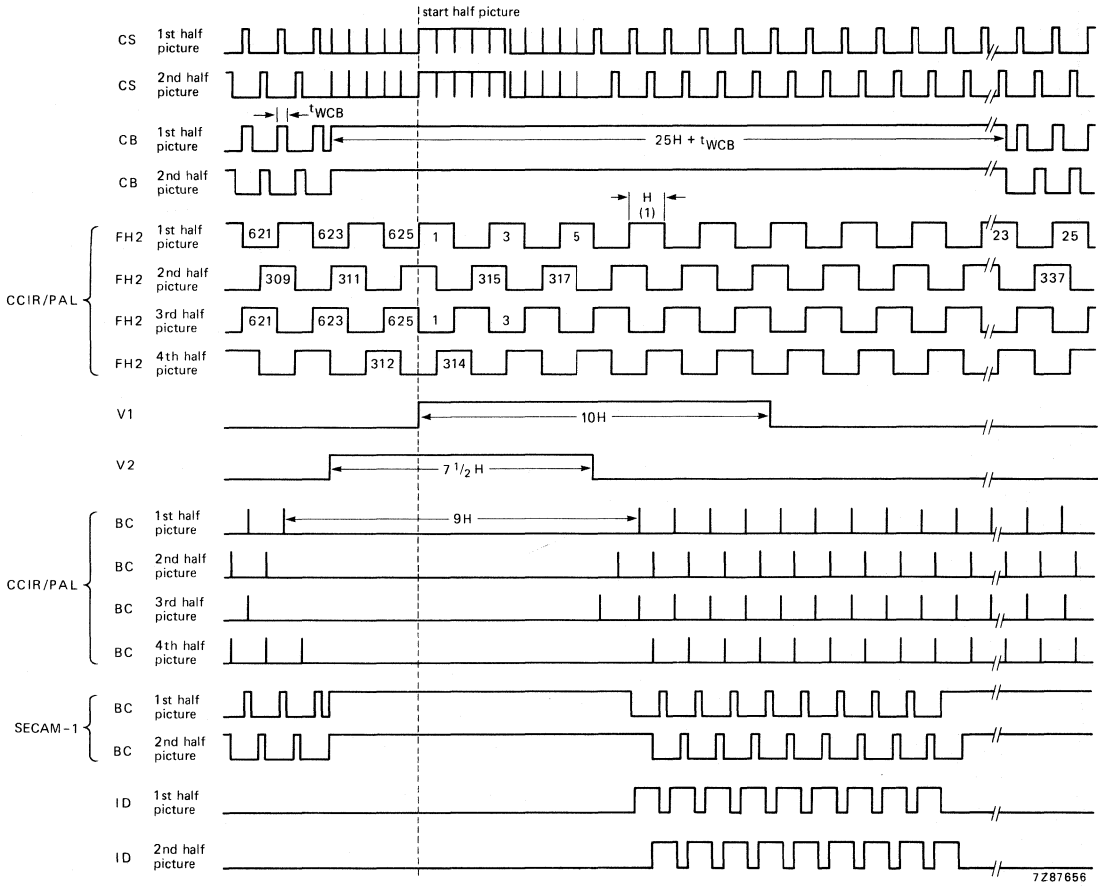
(2) Waveform at DL with two pulses suppressed increases the number of horizontal scans per half picture by 1.

(3) Waveform at DL with two additional pulses decreases the number of horizontal scans per half picture by 1.

Fig. 6 Manipulation of the horizontal frequency for non-standard systems.

Output waveforms

The output waveforms for the different modes of operation are shown in Figs 7 and 8.

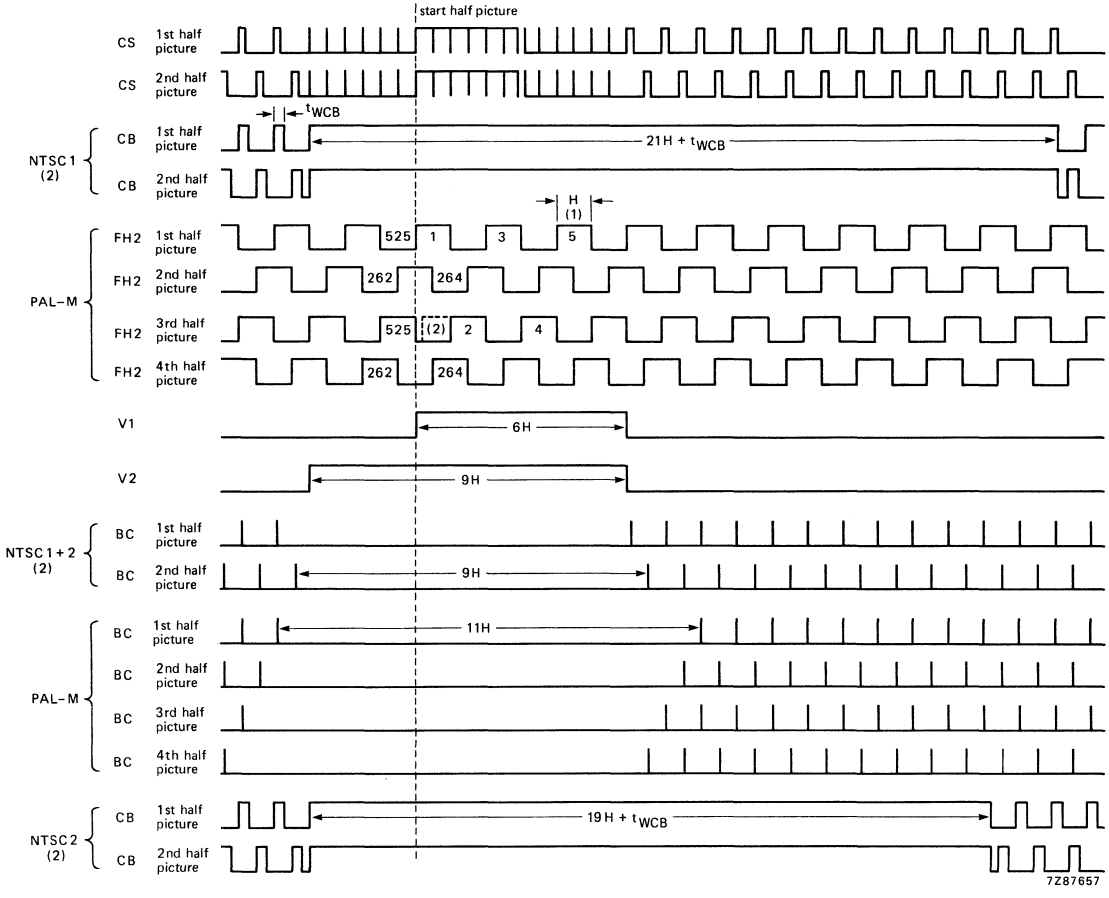


(1) H = 1 horizontal scan.

Fig. 7 Typical output waveforms for PAL/CCIR and SECAM. In the 624-line mode the output waveforms are identical to the 1st half picture of PAL/CCIR and are not interlaced (0,5H subtracted from the waveform timing).

FUNCTIONAL DESCRIPTION (continued)

Output waveforms (continued)



(1) H = 1 horizontal scan.

(2) NTSC mode reset; the 4th half picture is identical to the 2nd half picture for NTSC.

Fig. 8 Typical output waveforms for NTSC and PAL-M. In the 524-line mode the output waveforms are identical to the 1st half picture of NTSC and are not interlaced (0,5H subtracted from the waveform timing).

WAVEFORM TIMING (Table 3, Figs 9 and 10)

The waveform timing depends on the frequency of the oscillator input (f_{OSCI}). This is shown in Table 3 as the number (n) of oscillations at OSCI. The timings given are derived from n x t_{OSCI} ± 100 ns. One horizontal scan (H) = 320 x t_{OSCI} = $1/f_H$. Note that the number of horizontal scans per half picture can be modified for non-standard systems using input/output DL as shown in Fig. 6.

Table 3 Waveform timing

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
CS							
Horizontal sync pulse width	t_{WSC1}	4,8	4,77	4,77	4,8	µs	24
Equalizing pulse width	t_{WSC2}	2,4	2,38	2,38	2,4	µs	8
Serration pulse width	t_{WSC3}	4,8	4,77	4,77	4,8	µs	24
Duration of pre-equalizing pulses	–	2,5	3	3	2,5	H	
Duration of post-equalizing pulses	–	2,5	3	3	2,5	H	
Duration of serration pulses	–	2,5	3	3,5	2,5	H	
CB							
Horizontal blanking pulse width							
PAL/SECAM/PAL-M	t_{WCB}	12	–	11,12	12	µs	60
NTSC 1	t_{WCB}	–	11,12	–	–	µs	56
NTSC 2	t_{WCB}	–	10,53*	–	–	µs	53
Front porch	t_{PCBCS}	1,6	1,59	1,59	1,6	µs	8
Duration of vertical blanking							
PAL/SECAM/PAL-M		25H+t_{WCB}	–	21H+t_{WCB}	25H+t_{WCB}		
NTSC 1		–	21H+t_{WCB}	–	–		
NTSC 2		–	19H+t_{WCB}	–	–		
BC (PAL)							
Burst key pulse width	t_{WBC}	2,4	2,38	2,38	–	µs	12
Sync to burst delay	t_{PCSBC}	5,6	5,56	5,76	–	µs	28
Burst suppression	–	9	9	11	–	H	
Position of burst suppression: 1st half picture	–	H623 to H6	H523 to H6	H523 to H8	–	–	
2nd half picture	–	H310 to H318	H261 to H269	H260 to H270	–	–	
3rd half picture	–	H622 to H5	H523 to H6	H522 to H7	–	–	
4th half picture	–	H311 to H319	H261 to H269	H259 to H269	–	–	

WAVEFORM TIMING (continued)

Table 3 (continued)

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
BC (SECAM)							
Chroma pulse width	t_{WBC}	–	–	–	7,2	µs	36
Chroma to sync delay	t_{PBCCS}	–	–	–	1,6	µs	8
Duration of vertical blanking: SECAM 1	1st half picture: 25H + t_{WBC} except H320 to H328 2nd half picture: 24,5H + t_{WBC} except H7 to H15						
SECAM 2	1st half picture: 25H + t_{WBC} 2nd half picture: 24,5H + t_{WBC}						
CLP							
Clamp pulse width	t_{WCLP}	2,4	2,38	2,38	2,4	µs	12
Sync to clamp delay	t_{PCSCLP}	2,4	2,38	2,38	2,4	µs	12
DL							
Frequency	f_{DL}	2 x f_H	2 x f_H	2 x f_H	2 x f_H	–	
Pulse width	t_{WDL}	9,6	9,53	9,53	9,6	µs	48
DL to sync delay	t_{PCLCS}	5,6	5,56	5,56	5,6	µs	28
FH80							
Frequency	f_{FH80}	80 x f_H	80 x f_H	80 x f_H	80 x f_H	–	
Sync to FH80 delay	–	0,2	0,2	0,2	0,2	µs	1
H1, H2							
H1 pulse width	t_{WH1}	7,2	7,15	7,15	7,2	µs	36
H2 pulse width	t_{WH2}	7,2	7,15	7,15	7,2	µs	36
H1 to sync delay	t_{PH1CS}	0,8	0,79	0,79	0,8	µs	4
Sync to H2 delay	t_{PCSH2}	0,8	0,79	0,79	0,8	µs	4
Repetition period	–	64	63,56	63,56	64	µs	
V1, V2							
V1 duration	–	10	6	6	10	H	
V2 duration	–	7,5	9	9	7,5	H	
V1 to sync delay	t_{PV1CS}	1,6	1,59	1,59	1,6	µs	8
Sync to V2 delay	t_{PV2CS}	1,6	1,59	1,59	1,6	µs	8
FH2							
Frequency	f_{FH2}	$f_H/2$	$f_H/2$	$f_H/2$	$f_H/2$	–	
Sync to FH2 delay	–	0	0	0	0	µs	
FH3							
Frequency	f_{FH3}	400	360	360	$f_H/3$	–	
Sync to FH3 delay	–	–	–	–	0	µs	

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
WMP							
WMP pulse width	–	2,4	2,38	2,38	2,4	μs	12
Sync to WMP delay	–	34,4	34,16	34,16	34,4	μs	172
Duration of WMP	–	10	9	9	10	H	
Position of WMP							
1st half picture:	–	H163 to H173	H134 to H143	H134 to H143	H163 to H173	– –	
2nd half picture:	–	H475 to H485	H396 to H405	H396 to H405	H475 to H485	– –	
RI							
Frequency	–	$f_V/2$	$f_V/2$	$f_V/2$	$10f_H$	–	
Position of edges	–	H6 and H318	H7 and H269	H7 and H269	–	–	
ID							
ID pulse width	t_{WID}	12,0	11,12	11,12	12,0	μs	60
ID to sync delay	t_{PIDCS}	1,6	1,59	1,59	1,6	μs	8
Position of ID							
1st half picture:	–	H7 to H15	H8 to H22	H8 to H22	H7 to H15	–	
2nd half picture:	–	H320 to H328	H271 to H285	H271 to H285	H320 to H328	– –	

* Horizontal blanking pulse width for NTSC 2 can be 11, 12 μs maximum.

WAVEFORM TIMING (continued)

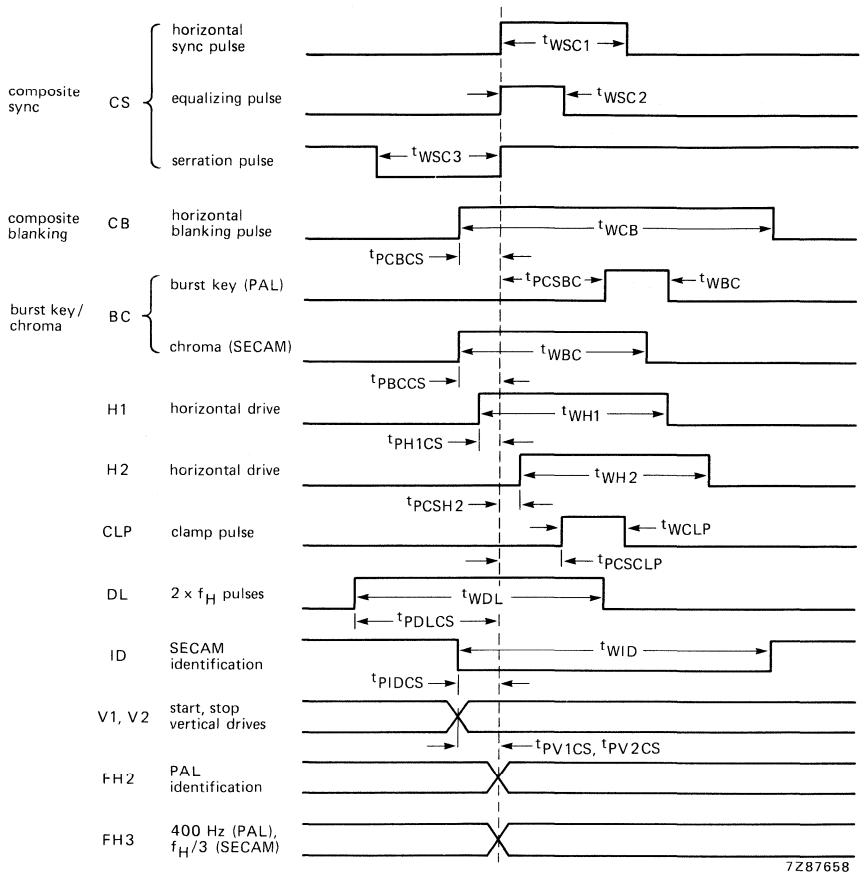


Fig. 9 Waveform timings: PAL/CCIR; SECAM; 624-line modes.

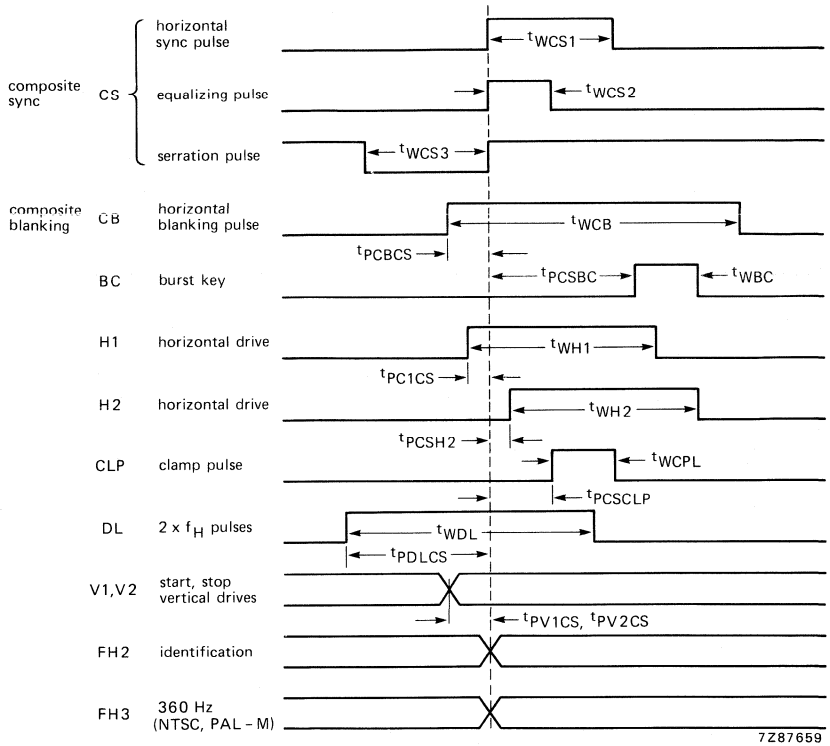


Fig. 10 Waveform timings: NTSC; PAL-M; 524-line modes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5 to + 15	V
Input voltage range	V_I	−0,5 to (V_{DD} + 0,5)*	V
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,5 to (V_{DD} + 0,5)*	V
Output current	$\pm I_O$	max. 10	mA
Power dissipation per output	P_O	max. 100	mW
Total power dissipation per package	P_{tot}	max. 200	mW
Operating ambient temperature range	T_{amb}	−25 to + 70	°C
Storage temperature range	T_{stg}	−55 to + 150	°C

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{DD} = 5,7 to 7,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5,7	–	7,5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °V	I_{IR}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	$-I_{IR}$	–	–	1	μA
Outputs (except PH and OSC0)					
Output voltage HIGH at $-I_{OH}$ = 0,5 mA	V_{OH}	V_{DD} − 0,5	–	–	V
Output voltage LOW at I_{OL} = 0,5 mA	V_{OL}	–	–	0,4	V
Output PH					
Output voltage HIGH at $-I_{OH}$ = 0,9 mA	V_{OH}	V_{DD} − 0,5	–	–	V
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V	I_{OR}	–	–	5	μA
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{OR}	–	–	1	μA
Output leakage current at V_O = 0 V; V_{DD} = 7,5 V	$-I_{OR}$	–	–	5	μA
Output leakage current at V_O = 0 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	$-I_{OR}$	–	–	1	μA
Output OSCO					
Output voltage HIGH at V_{OSCI} = 0 V; $-I_{OH}$ = 0,9 mA	V_{OH}	V_{DD} - 0,5	–	–	V
Output voltage LOW at V_{OSCI} = V_{DD}; I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V

parameter	symbol	min.	typ.	max.	unit
Input/output DL (open drain)*					
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V	I_{OR}	–	–	5	μA
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{OR}	–	–	1	μA
Load resistance (Fig. 4)					
at V_{DD} = 5,7 V	R_L	1,4	–	–	kΩ
at V_{DD} = 7,5 V	R_L	0,82	–	–	kΩ
Time constant (Fig. 4)					
at V_{DD} = 5,7 V	R_LC_L	–	–	19	ns
at V_{DD} = 7,5 V	R_LC_L	–	–	13	ns
Oscillator frequency (Fig. 4)					
Maximum oscillator frequency at V_{DD} = 5,7 V	f_{OSCI}	5,1	–	–	MHz

*** An external pull-up resistor (3,9 kΩ) must be connected between DL and V_{DD}. The time constant R_LC_L must not exceed the values given.**

APPLICATION INFORMATION

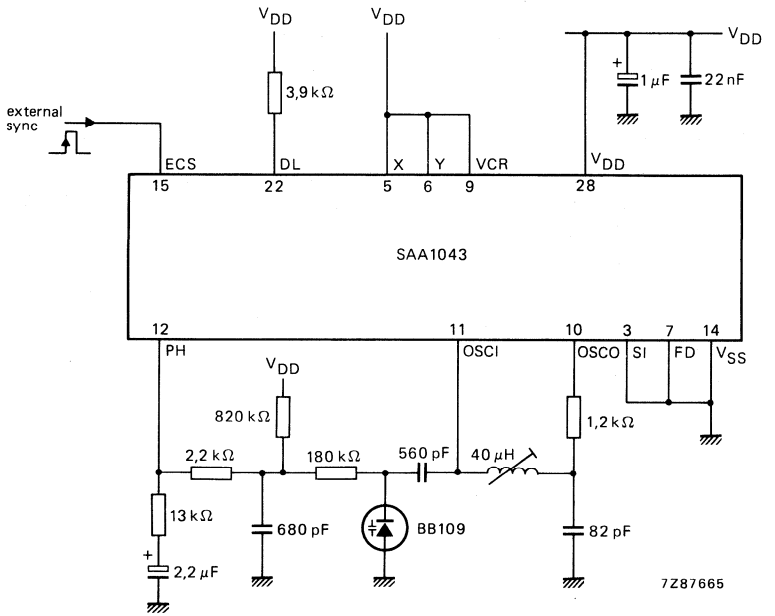


Fig. 11 Synchronizing circuit using passive filter network.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

SUBCARRIER COUPLER

GENERAL DESCRIPTION

The SAA1044 maintains the correct relationship between subcarrier and horizontal scan frequencies when an exact coupling is required. It is for use in combination with sync generator SAA1043 for application in colour video sources (cameras, film-scanners and similar equipments).

Features

- Provides exact relationship between subcarrier and horizontal scan frequencies
- Accommodates all standard frequencies
- Facilitates GENLOCK (general locking) applications

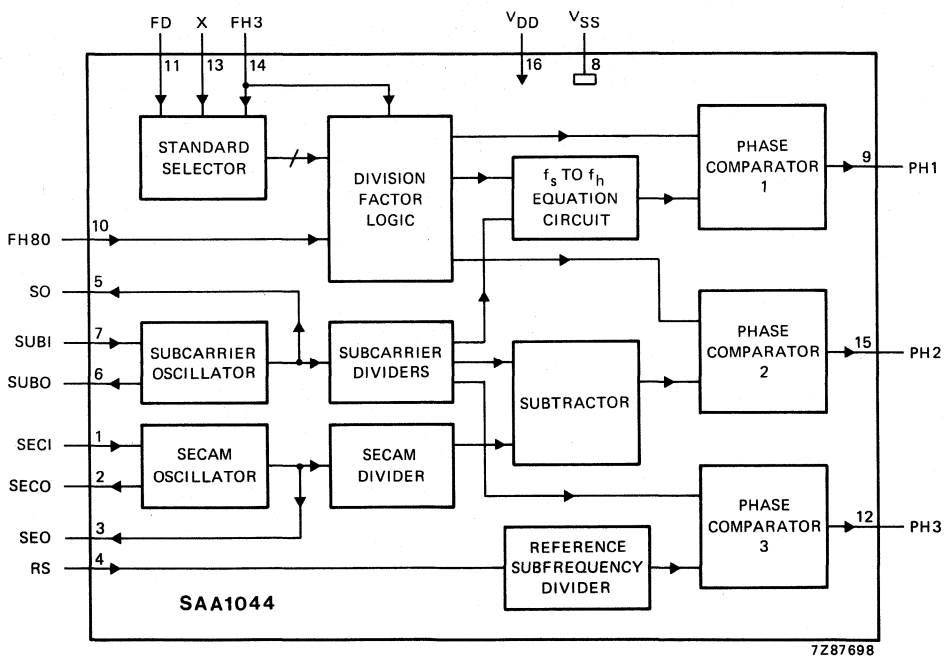


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

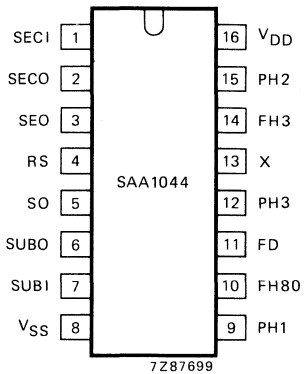


Fig. 2 Pinning diagram.

PINNING

1	SECI	SECAM oscillator input ($272f_H$)
2	SECO	SECAM oscillator output ($272f_H$)
3	SEO	inverted SECAM oscillator output
4	RS	reference subfrequency
5	SO	inverted subcarrier oscillator output
6	SUBO	subcarrier oscillator output
7	SUBI	subcarrier oscillator input
8	V_{SS}	negative supply voltage (ground)
9	PH1	phase comparator 1 output (FH80/SUBI)
10	FH80	1,25 MHz input (from SAA1043)
11	FD	standard programming input
12	PH3	phase comparator 3 output (RS/SUBI)
13	X	standard programming input
14	FH3	standard programming input (from SAA1043)
15	PH2	phase comparator 2 output (SECI/FH80)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Programming of operating standard

The standard required for operation is programmed using the inputs FD, X and FH3 as shown in Table 1.

Table 1 Programming of operating standard

standard	FD	X	FH3	relationship of subcarrier frequency (f_S) to horizontal scan frequency (f_H)
PAL	0	1	400 Hz	$f_S = 283{,}7516f_H$
SECAM	0	0	don't care	$f_S = 282f_H$
PAL-N	1	1	400 Hz	$f_S = 229{,}2516f_H$
PAL-M	1	0	1	$f_S = 227{,}25f_H$
NTSC	1	0	0	$f_S = 227{,}5f_H$

Positive logic: 1 = HIGH; 0 = LOW

Subcarrier/horizontal scan frequency relationship

The input FH80 from SAA1043 is the reference for horizontal scan frequency (f_H). This frequency is reduced by a factor determined by the selected operating standard to give a value of $8f_H$ (PAL, SECAM) or $10f_H$ (PAL-N, PAL-M, NTSC) to phase comparator 1. The subcarrier frequency (f_S) is manipulated to provide a comparable value at the second input to the phase comparator. When the frequencies of the two inputs to phase comparator 1 are equal, the relationship between f_H and f_S is as shown in Table 1.

Phase comparator 1 functions with an exclusive-OR phase detector circuit and provides an output which may be used to control a voltage-controlled oscillator (VCO) via a low-pass filter. The VCO reference can be the subcarrier or the horizontal scan frequency and the filter can be active or passive, depending on application.

A second subcarrier oscillator circuit is provided for SECAM operation. The operating frequency of this is centred on $272f_H$ to give, when $f_S = 282f_H$, comparable values of $5f_H$ at the two inputs to phase comparator 2. A second VCO loop can be used to control the SECAM oscillator frequency.

The high degrees of accuracy and stability required for GENLOCK applications are met by phase comparator 3. This compares the internal subcarrier and external reference frequencies. To adjust the phase over 2π, this comparator has a linear characteristic over 4π. The output signal PH3 has a period time of $f_S/4$ and a duty cycle of between 12,5% and 62,5% giving a sensitivity of 240 mV/rad. Errors due to temperature variation are minimized by symmetrical circuit and chip design.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}		−0,5 to + 15	V
Input voltage range	V_I	−0,5 to	$(V_{DD} + 0,5)$*	V
Input current	$\pm I_I$	max.	10	mA
Output voltage range	V_O	−0,5 to	$(V_{DD} + 0,5)$*	V
Output current	$\pm I_O$	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}		−25 to + 70	°C
Storage temperature range	T_{stg}		−55 to + 150	°C

HANDLING

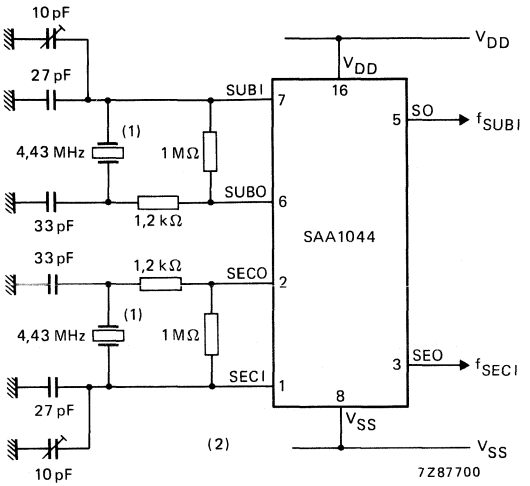
Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{DD} = 5,7 to 7,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

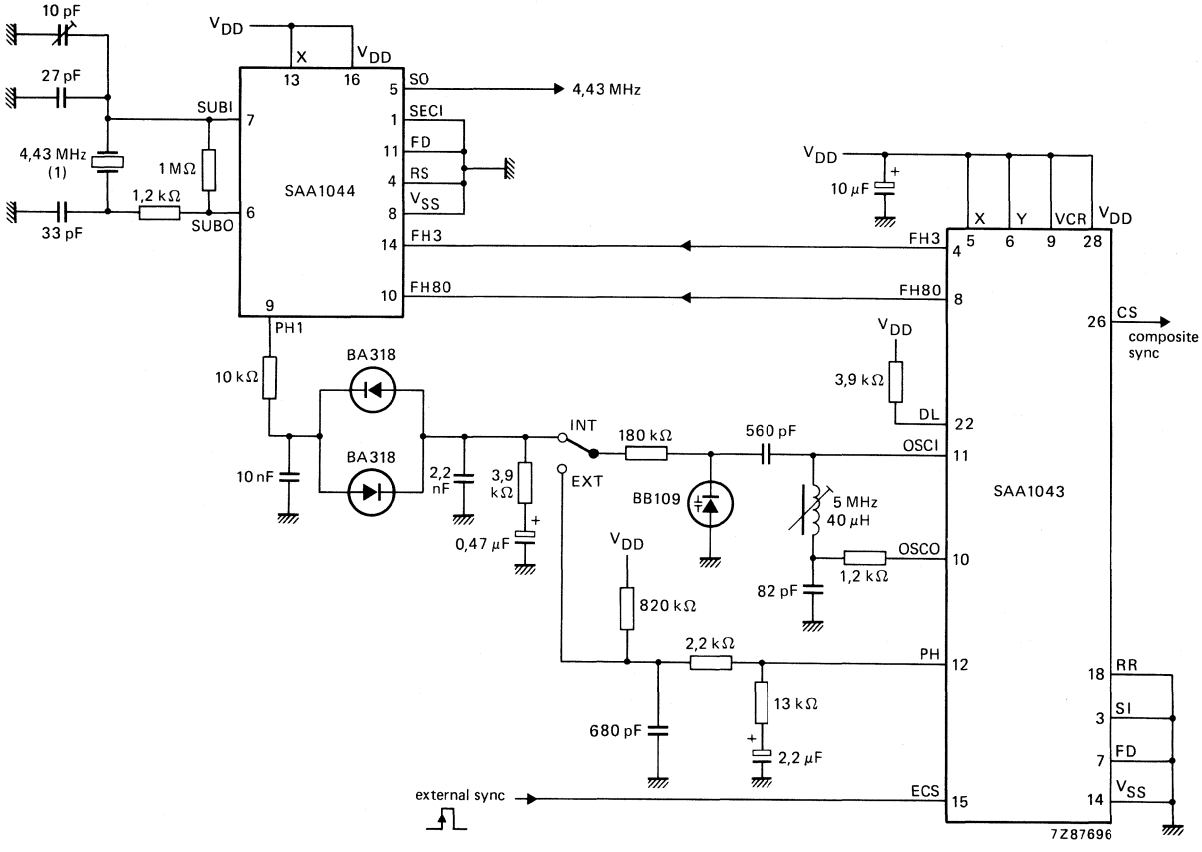
parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5,7	–	7,5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{IR}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	$-I_{IR}$	–	–	1	μA
Outputs (except SECO and SUBO)					
Output voltage HIGH at $-I_{OH}$ = 0,5 mA	V_{OH}	V_{DD} −0,5	–	–	V
Output voltage LOW at I_{OL} = 0,5 mA	V_{OL}	–	–	0,4	V
Outputs SECO and SUBO					
Output voltage HIGH at $-I_{OH}$ = 0,9 mA	V_{OH}	V_{DD} −0,5	–	–	V
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V
Oscillator frequency (Fig. 3)					
Maximum oscillator frequency at V_{DD} = 5,7 V	f_{SUBI} / f_{SECI}	5,1	–	–	MHz



(1) Catalogue number of crystal: 4322 143 04040.
(2) Inputs not shown are don't care.

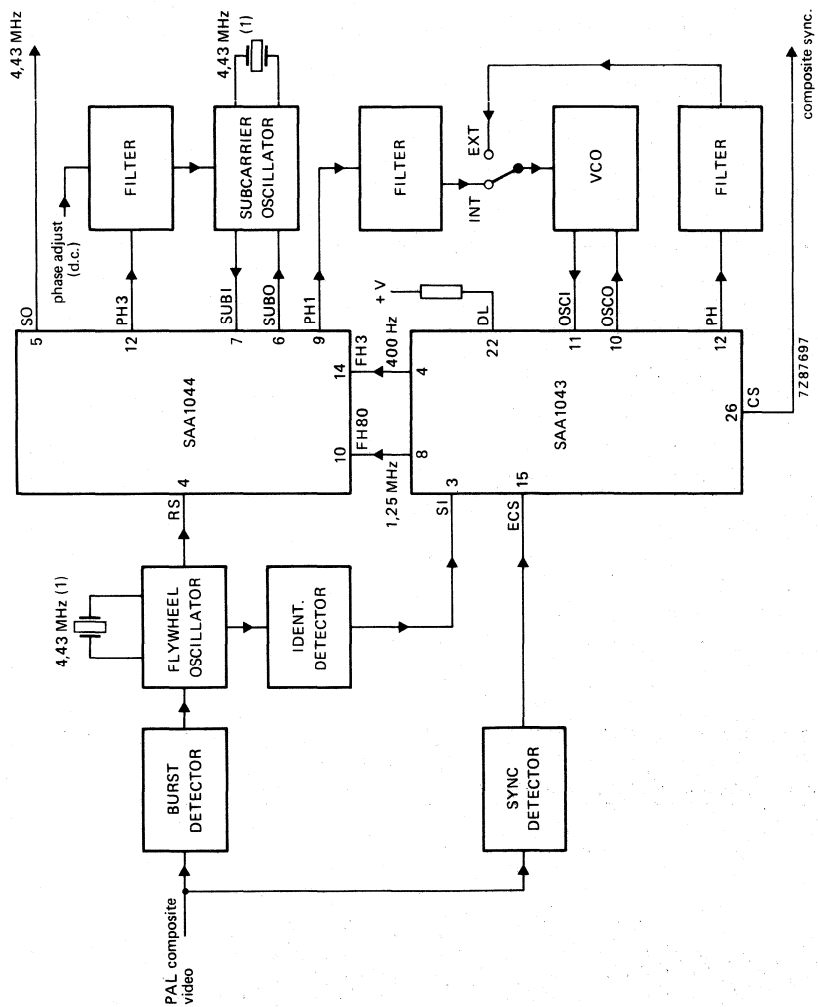
Fig. 3 Test set-up for oscillator frequency measurement.

APPLICATION INFORMATION



(1) Catalogue number of crystal: 4322 143 04040.

Fig. 4 Subcarrier coupling for PAL application; external synchronization is selected with switch in EXT condition.



(1) Catalogue number of crystal: 4322 143 04040.

Fig. 5 Subcarrier coupling for PAL GENLOCK application.

RADIO TUNING PLL FREQUENCY SYNTHESIZER

The SAA1057 is a single chip frequency synthesizer IC in I^2L technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.

Features

- On-chip prescaler with up to 120 MHz input frequency.
- On-chip AM and FM input amplifiers with high sensitivity (30 mV and 10 mV respectively).
- Low current drain (typically 16 mA for AM and 20 mA for FM) over a wide supply voltage range (3,6 V to 12 V).
- On-chip amplifier for loop filter for both AM and FM (up to 30 V tuning voltage).
- On-chip programmable current amplifier (charge pump) to adjust the loop gain.
- Only one reference frequency for both AM and FM.
- High signal purity due to a sample and hold phase detector for the in-lock condition.
- High tuning speed due to a powerful digital memory phase detector during the out-lock condition.
- Tuning steps for AM are: 1 kHz or 1,25 kHz for a VCO frequency range of 512 kHz to 32 MHz.
- Tuning steps for FM are: 10 kHz or 12,5 kHz for a VCO frequency range of 70 MHz to 120 MHz.
- Serial 3-line bus interface to a microcomputer.
- Test/features.

QUICK REFERENCE DATA

Supply voltage ranges	V_{CC1}	3,6 to 12	V
	V_{CC2}	3,6 to 12	V
	V_{CC3}	V_{CC2} to 31	V
Supply currents	$I_{CC1} + I_{CC2}$	typ. 18	mA
	I_{CC3}	typ. 0,8	mA
Input frequency ranges			
at pin FAM	f_{FAM}	512 kHz to 32	MHz
at pin FFM	f_{FFM}	70 to 120	MHz
Maximum crystal input frequency	f_{XTAL}	> 4	MHz
Operating ambient temperature range	T_{amb}	−25 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

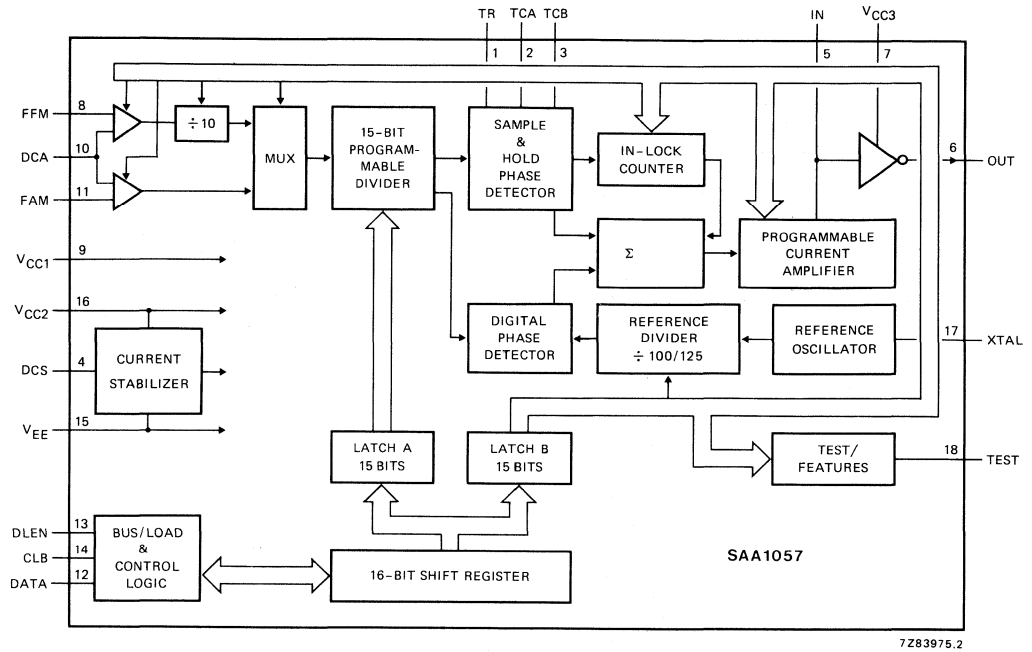


Fig. 1 Block diagram.

GENERAL DESCRIPTION

The SAA1057 performs the entire PLL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.
The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signals.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input.
- A 15-bit programmable divider for selecting the required frequency.
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1,25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1,25 kHz for AM, and 10 kHz and 12,5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the tuning system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig. 3). Latch B contains the control information.

OPERATION DESCRIPTION

Control information

The following functions can be controlled with the data word bits in latch B. For data word format and bit position see Fig. 3.

FM — FM/AM selection; '1' = FM, '0' = AM

REFH — reference frequency selection; '1' = 1,25 kHz, '0' = 1 kHz (sample and hold phase detector)

CP3, CP2, CP1, CP0 — control bits for the programmable current amplifier (see section Characteristics)

SB2 — enables last 8 bits (SLA to T0) of data word B; '1' = enables, '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically

SLA — load mode of latch A; '1' = synchronous, '0' = asynchronous

PDM1, PDM0 — phase detector mode

PDM1	PDM0	digital phase detector
0	X	automatic on/off
1	0	on
1	1	off

BRM — bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on

T3 — test bit; must be programmed always '0'

T2 — test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin

T1 — test bit; must be programmed always '0'

T0 — test bit; selects the output of the programmable counter to the TEST pin

T3	T2	T1	T0	TEST (pin 18)
0	0	0	0	1
0	1	0	0	reference frequency
0	0	0	1	output programmable counter
0	1	0	1	output in-lock counter '0' = out-lock '1' = in-lock

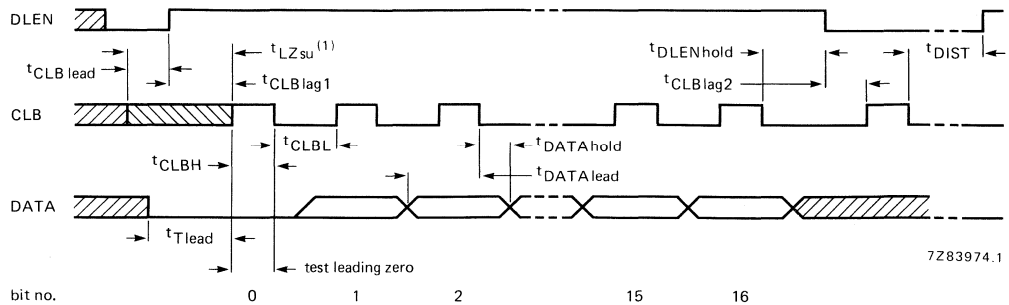


Fig. 2 BUS format.

(1) During the zero set-up time (t_{LZsu}) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I^2C bus is used for other devices on the same data and clock lines.

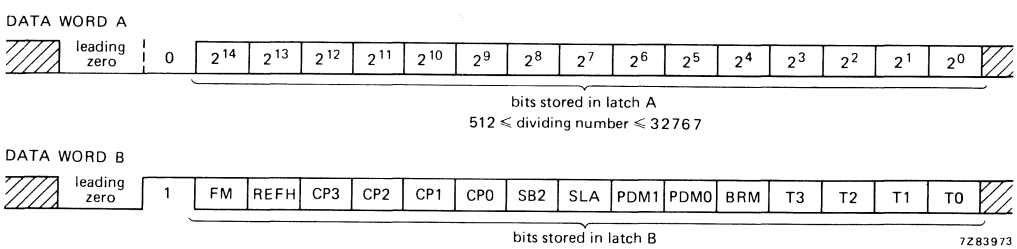


Fig. 3 Bit organization of data words A and B.

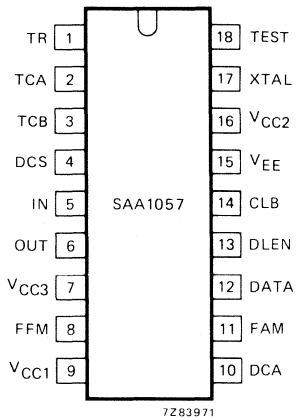


Fig. 4 Pinning diagram.

PINNING

1	TR	resistor/capacitors for sample and hold circuit
2	TCA	
3	TCB	
4	DCS	decoupling of supply
5	IN	input of output amplifier
6	OUT	output of output amplifier
7	V_{CC3}	positive supply voltage of output amplifier
8	FFM	FM signal input
9	V_{CC1}	positive supply voltage of high frequency logic part
10	DCA	decoupling of input amplifiers
11	FAM	AM signal input
12	DATA	BUS
13	DLEN	
14	CLB	
15	V_{EE}	ground
16	V_{CC2}	positive supply voltage of low frequency logic part and analogue part
17	XTAL	reference oscillator input
18	TEST	test output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; logic and analogue part	V_{CC1}; V_{CC2}	−0,3 to 13,2 V
Supply voltage; output amplifier	V_{CC3}	V_{CC2} to + 32 V
Total power dissipation	P_{tot}	max. 800 mW
Operating ambient temperature range	T_{amb}	−30 to + 85 °C
Storage temperature range	T_{stg}	−65 to + 150 °C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltages	V_{CC1}	3,6	5	12	V	
	V_{CC2}	3,6	5	12	V	
	V_{CC3}	V_{CC2}	–	31	V	
Supply currents*						
AM mode	I_{tot}	–	16	–	mA	$I_{tot} = I_{CC1} + I_{CC2}$ in-lock: BRM = '1'; PDM = '0'
FM mode	I_{tot}	–	20	–	mA	
	I_{CC3}	0,3	0,8	1,2	mA	I_{OUT} = 0
Operating ambient temperature	T_{amb}	−25	–	+ 80	°C	
RF inputs (FAM, FFM)						
AM input frequency	f_{FAM}	512 kHz	–	32	MHz	
FM input frequency	f_{FFM}	70	–	120	MHz	
Input voltage at FAM	$V_{i\ (rms)}$	30	–	500	mV	
Input voltage at FFM	$V_{i\ (rms)}$	10	–	500	mV	
Input resistance at FAM	R_i	–	2	–	kΩ	
Input resistance at FFM	R_i	–	135	–	Ω	
Input capacitance at FAM	C_i	–	3,5	–	pF	
Input capacitance at FFM	C_i	–	3	–	pF	
Voltage ratio allowed between selected and non-selected input	V_s/V_{ns}	–	−30	–	dB	
Crystal oscillator (XTAL)						see note 1
Maximum input frequency	f_{XTAL}	4	–	–	MHz	
Crystal series resistance	R_s	–	–	150	Ω	
BUS inputs (DLEN, CLB, DATA)						
Input voltage LOW	V_{IL}	0	–	0,8	V	
Input voltage HIGH	V_{IH}	2,4	–	V_{CC1}	V	
Input current LOW	$-I_{IL}$	–	–	10	μA	V_{IL} = 0,8 V
Input current HIGH	I_{IH}	–	–	10	μA	V_{IH} = 2,4 V

* When the bus is in the active mode (see BRM in Control Information), 4,5 mA should be added to the figures given.

CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
BUS inputs timing (DLEN, CLB, DATA)						see also Fig. 2 and note 2
Lead time for CLB to DLEN	$t_{CLBlead}$	1	–	–	µs	
Lead time for DATA to the first CLB pulse	t_{Tlead}	0,5	–	–	µs	
Set-up time for DLEN to CLB	$t_{CLBlag1}$	5	–	–	µs	
CLB pulse width HIGH	t_{CLBH}	5	–	–	µs	
CLB pulse width LOW	t_{CLBL}	5	–	–	µs	
Set-up time for DATA to CLB	$t_{DATAlead}$	2	–	–	µs	
Hold time for DATA to CLB	$t_{DATAhold}$	0	–	–	µs	
Hold time for DLEN to CLB	$t_{DLENhold}$	2	–	–	µs	
Set-up time for DLEN to CLB load pulse	$t_{CLBlag2}$	2	–	–	µs	
Busy time from load pulse to next start of transmission	t_{DIST}	5	–	–	µs	next transmission after word 'B' to other device
Busy time						or
asynchronous mode	t_{DIST}	0,3	–	–	ms	next transmission
synchronous mode	t_{DIST}	1,3	–	–	ms	to SAA1057 after word 'A' (see also note 5)
Sample and hold circuit (TR, TCA, TCB)						see also notes 3; 4
Minimum output voltage	V_{TCA}, V_{TCB}	–	1,3	–	V	
Maximum output voltage	V_{TCA}, V_{TCB}	–	–	V_{CC2}–0,7	V	
Capacitance at TCA (external)	C_{TCA}	–	–	2,2	nF	REFH = '1'
	C_{TCA}	–	–	2,7	nF	REFH = '0'
Discharge time at TCA	t_{dis}	–	–	5	µs	REFH = '1'
	t_{dis}	–	–	6,25	µs	REFH = '0'
Resistance at TR	R_{TR}	100	–	–	Ω	external
Voltage at TR during discharge	V_{TR}	–	0,7	–	V	
Capacitance at TCB	C_{TCB}	–	–	10	nF	external
Bias current into TCA, TCB	I_{bias}	–	–	10	nA	in-lock

CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Programmable current amplifier (PCA)						
Output current of the dig. phase detector	$\pm I_{dig}$	–	0,4	–	mA	
Current gain of PCA						
CP3 CP2 CP1 CP0						
P1 0 0 0 0	G_{P1}	–	0,023	–		$V_{CC2} \geqslant 5$ V (only for P1)
P2 0 0 0 1	G_{P2}	–	0,07	–		
P3 0 0 1 0	G_{P3}	–	0,23	–		
P4 0 1 1 0	G_{P4}	–	0,7	–		
P5 1 1 1 0	G_{P5}	–	2,3	–		
Ratio between the output current of S/H into PCA and the voltage on C_{TCB}	S_{TCB}	–	1,0	–	μA/V	
Offset voltage on TCB	ΔV_{TCB}	–	–	1	V	in-lock
Output amplifier (IN,OUT)						
Input voltage	V_{IN}	–	1,3	–	V	in-lock; equal to internal reference voltage
Output voltages						
minimum	V_{OUT}	–	–	0,5	V	$-I_{OUT}$ = 1 mA
maximum	V_{OUT}	$V_{CC3}-2$	–	–	V	I_{OUT} = 1 mA
maximum	V_{OUT}	$V_{CC3}-1$	–	–	V	I_{OUT} = 0,1 mA
Maximum output current	$\pm I_{OUT}$	5	–	–	mA	V_{OUT} = ½ V_{CC3}
Test output (TEST)*						
Output voltage LOW	V_{TL}	–	–	0,5	V	
Output voltage HIGH	V_{TH}	–	–	12	V	
Output current OFF	I_{Toff}	–	–	10	μA	V_{TH}
Output current ON	I_{Ton}	150	–	–	μA	V_{TL}
Ripple rejection**						
at f_{ripple} = 100 Hz						
$\Delta V_{CC1}/\Delta V_{OUT}$		–	77	–	dB	
$\Delta V_{CC2}/\Delta V_{OUT}$		–	70	–	dB	
$\Delta V_{CC3}/\Delta V_{OUT}$		–	60	–	dB	$V_{OUT} \leqslant V_{CC3}-3$ V

* Open collector output.

** Measured in Fig. 6.

NOTES

1. Pin 17 (XTAL) can also be used as input for an external clock.
   The circuit for that is given in Fig. 5. The values given in Fig. 5 are a typical application example.

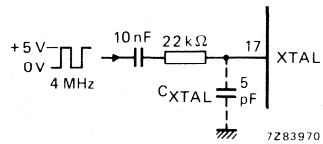


Fig. 5 Circuit configuration showing external 4 MHz clock.

2. See BUS information in section 'operation description'.
3. The output voltage at TCB and TCA is typically ½ V_{CC2}+0,3 V when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula ½ V_{CC2}+0,3 V.
4. Crystal oscillator frequency f_{XTAL} = 4 MHz.
5. The busy-time after word "A" to another device which has more clock pulses than the SAA1057 (> 17) must be the same as the busy-time for a next transmission to the SAA1057.
   When the other device has a separate DLEN or has less clock pulses than the SAA1057 it is not necessary to keep to this busy-time, 5 μs will be sufficient.

APPLICATION INFORMATION

Initialize procedure

Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.
For the complete initialization (defining all control bits) a transmission of word B should follow. This means that the IC is ready to accept word A.

Synchronous/asynchronous operation

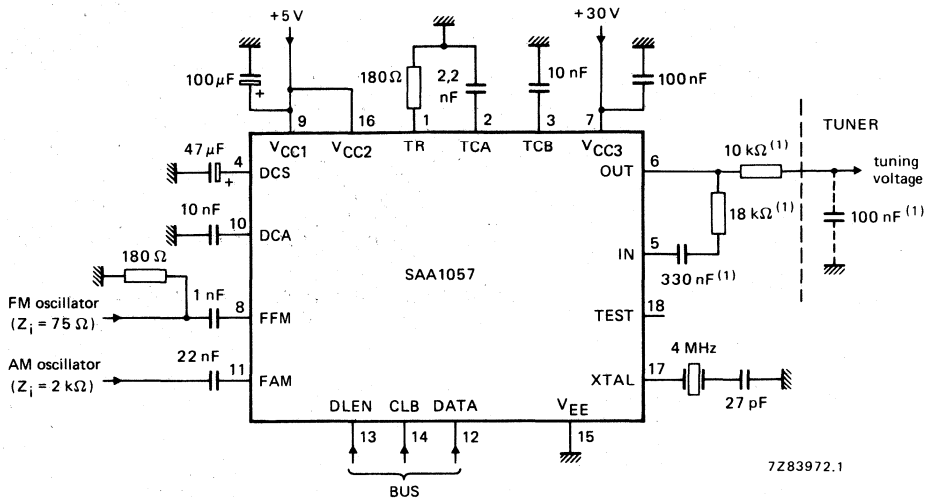
Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g. search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

Restrictions to the use of the programmable current amplifier

The lowest current gain (0,023) must not be used in the in-lock condition when the supply voltage V_{CC2} is below 5 V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition (see also section 'Characteristics').

Transient times of the bus signals

When the SAA1057 is operating in a system with continuous activity on the bus lines, the transient times at the bus inputs should not be less than 100 ns. Otherwise the signal-to-noise ratio of the tuning voltage is reduced.



(1) Values depend on the tuner diode characteristics.

Fig. 6 Application example of the SAA1057PLL frequency synthesizer module.

LED DISPLAY/INTERFACE CIRCUIT

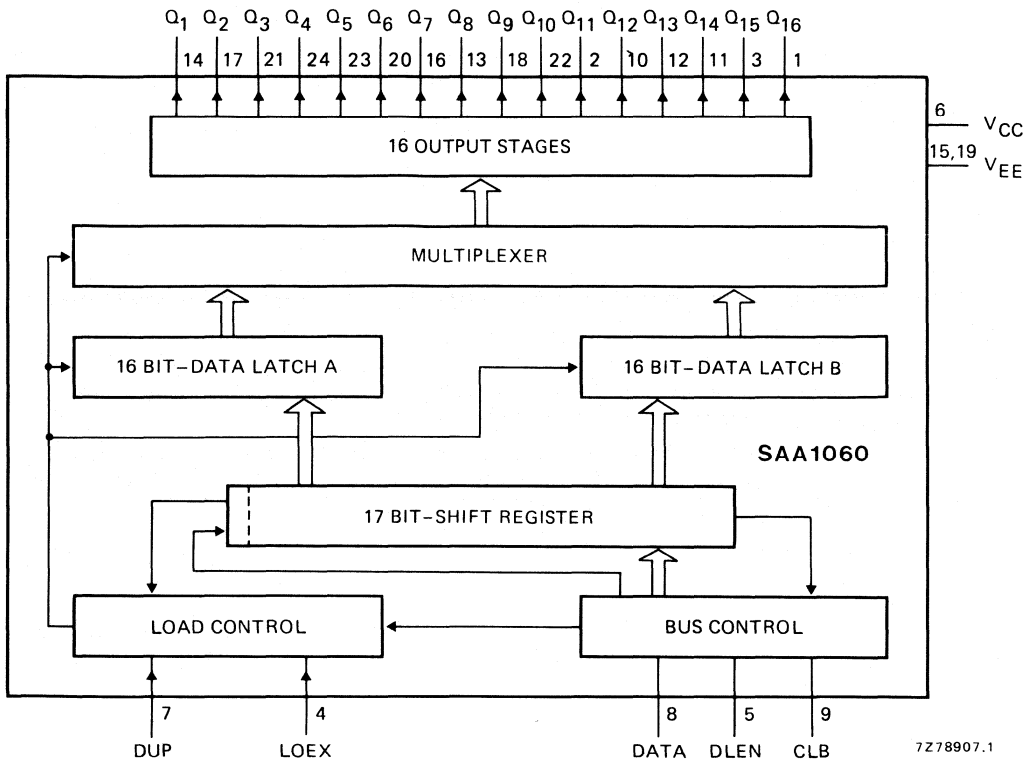


Fig. 1 Block diagram.

Features

- Driving 7, 14, 16-segment displays.
- Driving linear displays, bar graph displays for analogue functions.
- Serial to parallel decoder.
- Bus control for the selection of 18-bit words.
- 2 x 16-bit latch.
- Duplex operation for two modes of output: static (16 bit) or dynamic (2 x 16 bit).
- Data transfer control.
- 2 outputs for higher output current (80 mA).

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	4 to 6	V
Operating ambient temperature range	T_{amb}	−20 to + 80	°C
Maximum input frequency	f_I	typ. 50	kHz
Supply current	I_{CC}	typ. 60	mA
Output current	I_Q	< 40	mA
Output current (Q_8 and Q_{16} only)	I_Q	< 80	mA

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

GENERAL DESCRIPTION

The integrated circuit SAA1060 is primarily designed to drive the display unit of a digital tuning system. It can also be used as a 16-bit serial to parallel decoder. Since the device has no decoder (this is handled by a microcomputer), it has many applications:

- driving 7-segment displays
- driving 14-segment displays
- driving linear displays, e.g. pointer, bar graph
- static output of switch-functions
- digital to analogue converter, with external R-2R network
- extension of the number of outputs for microprocessors or microcomputers.

Data transmission is initiated by means of a burst of clock pulses (CLB), a data line enable signal (DLEN) and the data signal (DATA). The bus control circuit distinguishes between interference and valid data by checking word length (17 bits) and the leading zero. This allows different bus information to be supplied on the same bus lines for other circuits (e.g. SAA1056 with 16 bits).

The last bit (bit 17) of the data word contains the information which of the two internal latches will be loaded. The input LOEX determines if the latched data of selected latches is presented directly to the outputs, or synchronized with the data select signal DUP.

The output stages are n-p-n transistors with open collectors. The current capability is designed for the requirements of duplex operation. Two of the outputs (Q_8 and Q_{16}) are arranged for double current, so that 2 x 2 segments can be connected in parallel.

OPERATION DESCRIPTION

Data inputs (DLEN, DATA)

The SAA1060 processes serially the 18-bit data words synchronized with the clock burst (CLB) and applied to the data input DATA. A command will be accepted only when the data line enable input (DLEN) is HIGH (see Fig. 3).

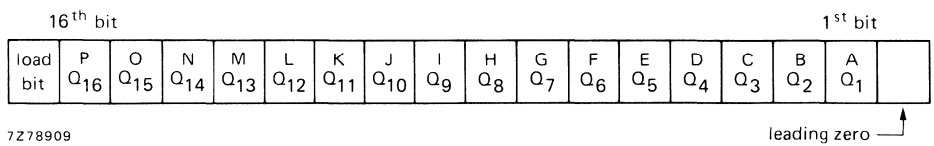


Fig. 2 Organization of a data word.

Condition for 17th bit:
0 = load data latch B
1 = load data latch A

The loading of the accepted information in one of the data latches is done by the 19th clock pulse, when DLEN is LOW.

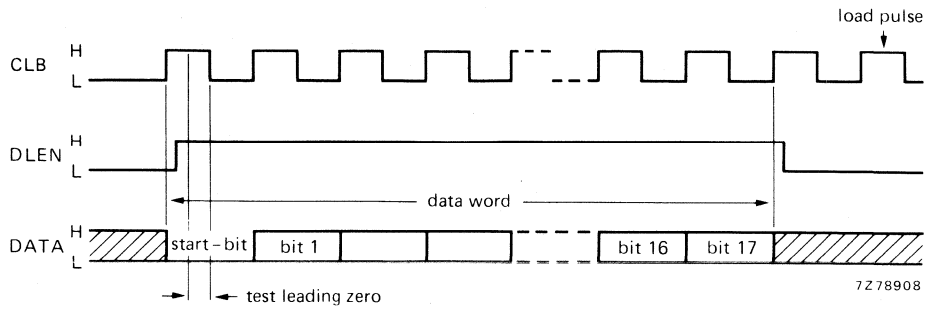


Fig. 3 Pulse diagram of the 16-bit data transmission.

Each data word must start with a leading zero. The SAA1060 checks the data word for the correct length (18 bits) and also for the leading zero.
The actual data is switched directly to the appropriate outputs. For switching on a segment, a '0' (LOW) is necessary at the appropriate data bit.

Data selection input (DUP)

The logic states at input DUP determine which of the two latch contents can be found on the output.

0 = latch A contents
1 = latch B contents

Load control input (LOEX)

Input LOEX determines the operation mode in which the device is able to work.

0 = duplex mode, i.e. output synchronized with the duplex signal
1 = d.c. mode, i.e. output direct from the by DUP selected data latch.

When operating in duplex mode at 50 Hz, the time between two data words to be transmitted must be > 21 ms.

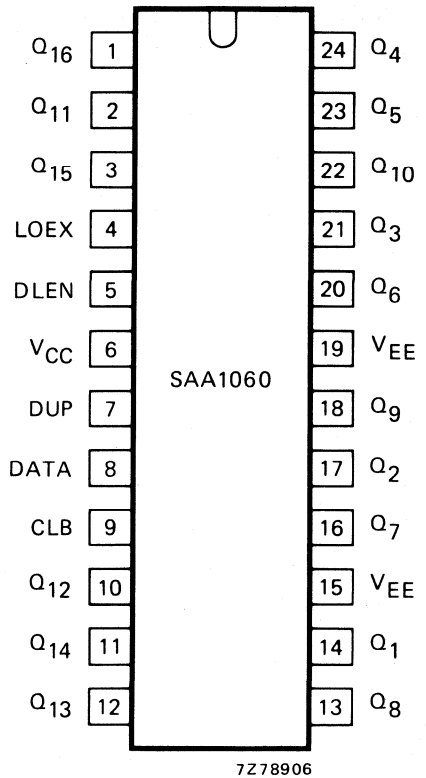


Fig. 4 Pinning diagram.

RATINGS (V_{EE} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{CC}	−0,3 to + 7	V
Total power dissipation	P_{tot}	max. 900	mW
Operating ambient temperature range	T_{amb}	−20 to + 80	°C
Storage temperature range	T_{stg}	−25 to + 125	°C

CHARACTERISTICS

V_{EE} = 0; T_{amb} = 25 °C; unless otherwise specified

	V_{CC} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{CC}	4	5	6	V	
Supply current	5	I_{CC}	–	60	–	mA	
Inputs DATA, CLB, DLEN, LOEX							
input voltage HIGH	5	V_{IH}	2	–	5	V	
input voltage LOW	5	V_{IL}	–	–	1	V	
input current LOW	5	$-I_{IL}$	–	–	20	μA	V_I = 0
maximum input frequency	5	f_I	–	50	–	kHz	
Input DUP							
input voltage HIGH	5	V_{IH}	0,8	–	12	V	
input voltage LOW	5	V_{IL}	–6	–	0,4	V	
input current HIGH	5	I_{IH}	0,01	–	12	mA	
maximum input frequency	5	f_I	–	50	–	kHz	
Outputs Q_1 to Q_7, Q_9 to Q_{15}							
output voltage HIGH	5	V_{QH}	–	–	16,8	V	I_{QH} = 0
output voltage LOW	5	V_{QL}	–	–	0,5	V	I_{QL} = 40 mA
output current LOW							
duplex mode	5	I_{QL}	–	–	60	mA	peak value at sinusoidal voltage
d.c. mode	5	I_{QL}	–	20	40	mA	
Outputs Q_8 and Q_{16}							
output voltage HIGH	5	V_{QH}	–	–	16,8	V	I_{QH} = 0
output voltage LOW	5	V_{QL}	–	–	0,5	V	I_{QL} = 80 mA
output current LOW							
duplex mode	5	I_{QL}	–	–	120	mA	peak value at sinusoidal voltage
d.c. mode	5	I_{QL}	–	40	80	mA	

OUTPUT PORT EXPANDER

The SAA1061 is a MOS N-channel output port expander circuit, which converts serial input data into parallel output information. The IC is used in combination with a microcomputer.

Features

- Bus control for the selection of 18-bit words.
- 16-bit latch and low-ohmic driver outputs.
- Pin compatible with the SAA1060, except the SAA1061 has no duplex mode.
- Address selection inputs; up to four SAA1061 circuits can be operated from a common CBUS.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	typ.	5 V
Operating ambient temperature range	T_{amb}		−20 to +80 °C
Supply current	I_{DD}	typ.	9 mA
Output current per output	I_O	typ.	15 mA

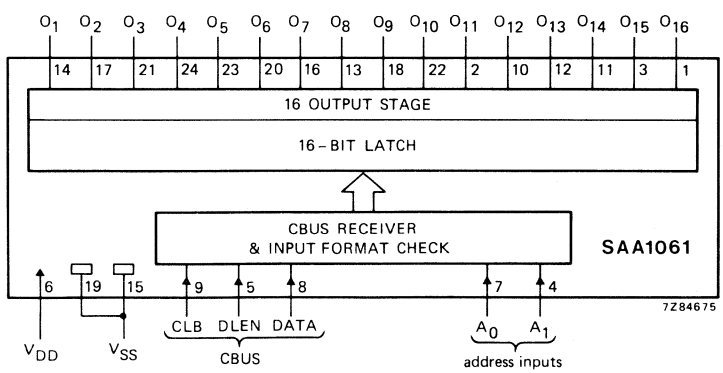


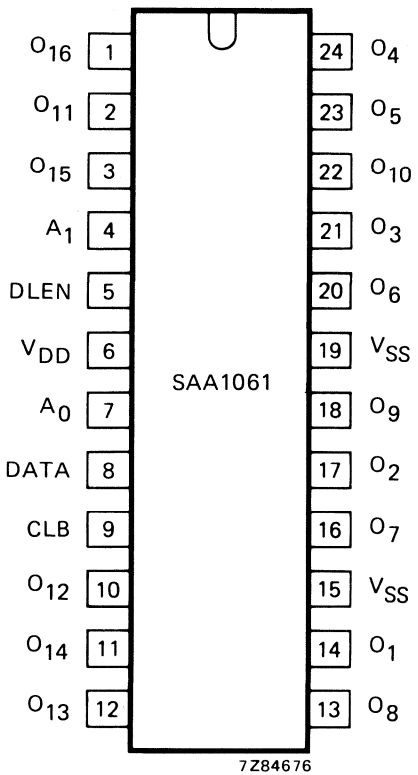
Fig. 1 Block diagram.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).



PINNING

6	V_{DD}	positive supply (+5 V)
15, 19	V_{SS}	ground (0 V)

Inputs

8	DATA	data word	CBUS
9	CLB	clock burst	CBUS
5	DLEN	data line enable	CBUS
7	A_0	address bit S0	
4	A_1	address bit S1	

Outputs

14	O_1	driver outputs O_1 to O_{16} corresponding with the data bits 1 to 16 of the data word
17	O_2	
21	O_3	
24	O_4	
23	O_5	
20	O_6	
16	O_7	
13	O_8	
18	O_9	
22	O_{10}	
2	O_{11}	
10	O_{12}	
12	O_{13}	
11	O_{14}	
3	O_{15}	
1	O_{16}	

Fig. 2 Pinning diagram.

GENERAL DESCRIPTION

The SAA1061 is an addressable output port expander for use in microcomputer controlled systems. It converts serial input data into parallel output information. The circuit comprises a CBUS receiver, logic to check input format, a 16-bit serial/parallel converter, latches and drivers for the parallel outputs.

This universal device can be used for e.g.:

- static output of switch-functions
- extension of the number of outputs for microcomputers or microprocessors
- driving maximum 16-segment LEDs; e.g. 7, 4 or 16-segment displays
- driving linear displays (pointer, bar graph)
- digital to analogue conversion with external resistor network.

The data is transmitted via the 3-line CBUS from the microcomputer. If the data transmission is valid, the data are transferred by a load pulse via the latch to the driver output. Each data transmission is checked for word length (18-bit) by the on-chip word format control circuitry. This allows different bus information to be supplied on the same bus lines for other circuits.

The address inputs A_0 and A_1 determine four address possibilities. A data transmission only takes place if the programmed addresses correspond with the address bits S0 and S1.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to +7,5	V
Input voltage range	V_I	−0,3 to +15	V
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,3 to +16,5	V
Output current per output	$\pm I_O$	max. 20	mA
Power dissipation per output	P_O	max. 7,5	mW
Total power dissipation per package	P_{tot}	max. 300	mW
Operating ambient temperature range	T_{amb}	−20 to +80	°C
Storage temperature range	T_{stg}	−20 to +125	°C

CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 5 V; T_{amb} = −20 to +80 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltage	V_{DD}	4,5	5	5,5	V	
Supply current	I_{DD}	–	–	20	mA	
Inputs CLB, DLEN, DATA, A_0, A_1						T_{amb} = 25 °C
Input voltage LOW	V_{IL}	−0,3	–	0,8	V	
Input voltage HIGH	V_{IH}	2,0	–	15	V	
Input leakage current	I_{IR}	–	–	1	μA	V_I = −0,3 to +15 V
Outputs O_1 to O_{16} (open drain)						
Output voltage LOW	V_{OL}	–	–	0,65	V	I_{OL} = 15 mA
Output leakage current HIGH	I_{OH}	–	–	20	μA	V_{OH} = 16,5 V
Rise and fall times	t_r, t_f	–	–	10	μs	V_{OL} = 1,5 V; V_{OH} = 13,5 V
CBUS timing						
Rise and fall times	t_r, t_f	–	–	2	μs	see Fig. 3
Data set-up time DATA → CLB	t_{SUDA}	400	–	–	ns	
Data hold time DATA → CLB	t_{HDDA}	250	–	–	ns	
Enable set-up time DLEN → CLB	t_{SUEN}	400	–	–	ns	
Disable set-up time CLB → DLEN	t_{SUDI}	600	–	–	ns	
Set-up time DLEN → CLB (load pulse)	t_{SULD}	400	–	–	ns	
CLB pulse width HIGH/LOW	t_{WH}, t_{WL}	450	–	–	ns	

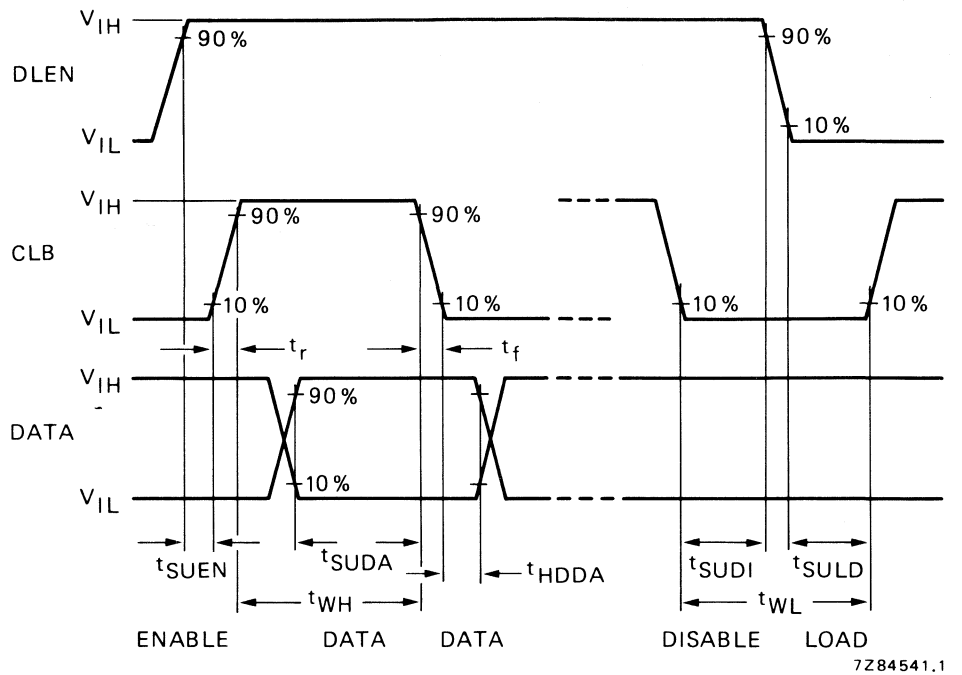


Fig. 3 CBUS timing.

OPERATION DESCRIPTION

1. CBUS transmission

The data words are entered via a serial CBUS interface. A clock burst of 18 clock periods is used to transmit the 16-bit data word, plus 2 identifier bits.

Serial data words, which are synchronized with the clock burst (CLB), are accepted if the enable input DLEN is HIGH at the same time. Each transmission is checked for word length (number of clock pulses during DLEN is HIGH) and the address bits S0 and S1.

The valid data flag is only set if:
1. Word length is correct; 2 address bits and 16 data bits.
2. Address bits S0 and S1 correspond with A_0 and A_1.

Loading the information into the selected latch register is done by the load pulse (first clock pulse after the HIGH-to-LOW transition of DLEN) if the address bits correspond with A_0 and A_1. The load pulse or a new LOW-to-HIGH transition of DLEN resets the valid data flag. Only after the valid data flag is reset, will new data be accepted.

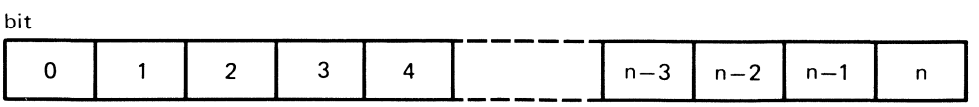


Fig. 4 Data word organization.

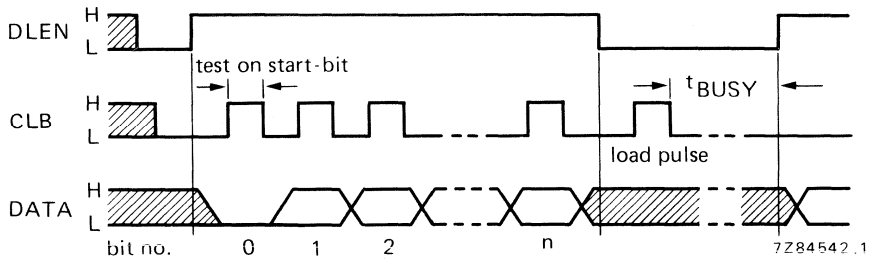


Fig. 5 CBUS data transmission.

Definitions to Figs 4 and 5:

- Word length: number of clock pulses during DLEN is active (HIGH); n + 1 bits = 18 bits.
- Bit number 0 is for the SAA1061 S0.
- Data bits: bit numbers 1 to n-1 (16-bits); bit no. n is S1.
- Load pulse: first clock pulse after DLEN returns to inactive (LOW).

2 Address inputs A_0 and A_1

The 1st bit (bit S0) and the 18th bit (bit S1) of the data word are the address bits.
Data is accepted only if the addresses correspond to the programmed addresses at inputs A_0 and A_1, that is for:

A_0 = S0 and A_1 = S1.

3 Data outputs O_1 to O_{16}

The outputs O_1 to O_{16} correspond with the data bits 1 to n-1 (16-bits). The open drain driver outputs (O_1 to O_{16}) are switched to ground (O_n = LOW), if the corresponding data bit is LOW,

4 Power-on reset

The circuit generates internally a reset-cycle after switching on the supply and the outputs become high-ohmic (HIGH).

LCD DISPLAY/INTERFACE CIRCUIT

GENERAL DESCRIPTION

The SAA1062A is designed to drive a Liquid Crystal Display (LCD) of a digital tuning system. It contains a shift register with programmable length (18 or 21 bits), latches, both synchronized or static, exclusive-OR segment drivers (17 or 20 bits), an l.f. oscillator and a backplane driver for the LCD. The circuit is designed to be driven by a 3 bus structure from a microcomputer and can also be used as a programmable 17 or 20 bits serial-to-parallel decoder. It is also capable of storing 40 bits of information.

Features

- Driving 7 to 20-segment displays.
- Driving linear displays.
- Serial to parallel decoder of digital signals.
- Bus control for the selection of 18/21-bit words.
- 17/20-bit latch.
- A.C. segment drive.
- On-chip oscillator.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	4,2 to 5,5	V
Operating ambient temperature range	T_{amb}	−20 to + 70	°C
Maximum input frequency	f_i	typ. 50	kHz
Supply current	I_{CC}	typ. 3,5	mA
Output current (Q_1 to Q_{20})	I_Q	> 60	μA

PACKAGE OUTLINES

SAA1062A : 28-lead DIL; plastic (SOT-117).
SAA1062AT: 28-lead mini-pack; plastic (SO-28; SOT-136A).

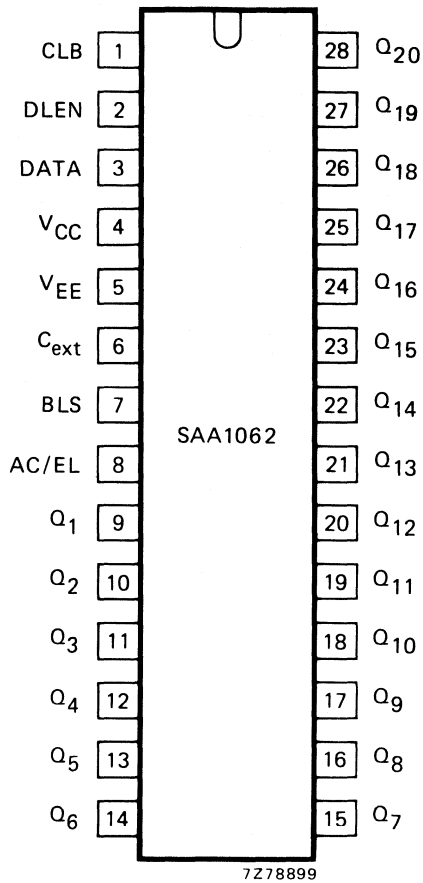


Fig. 1 Pinning diagram.

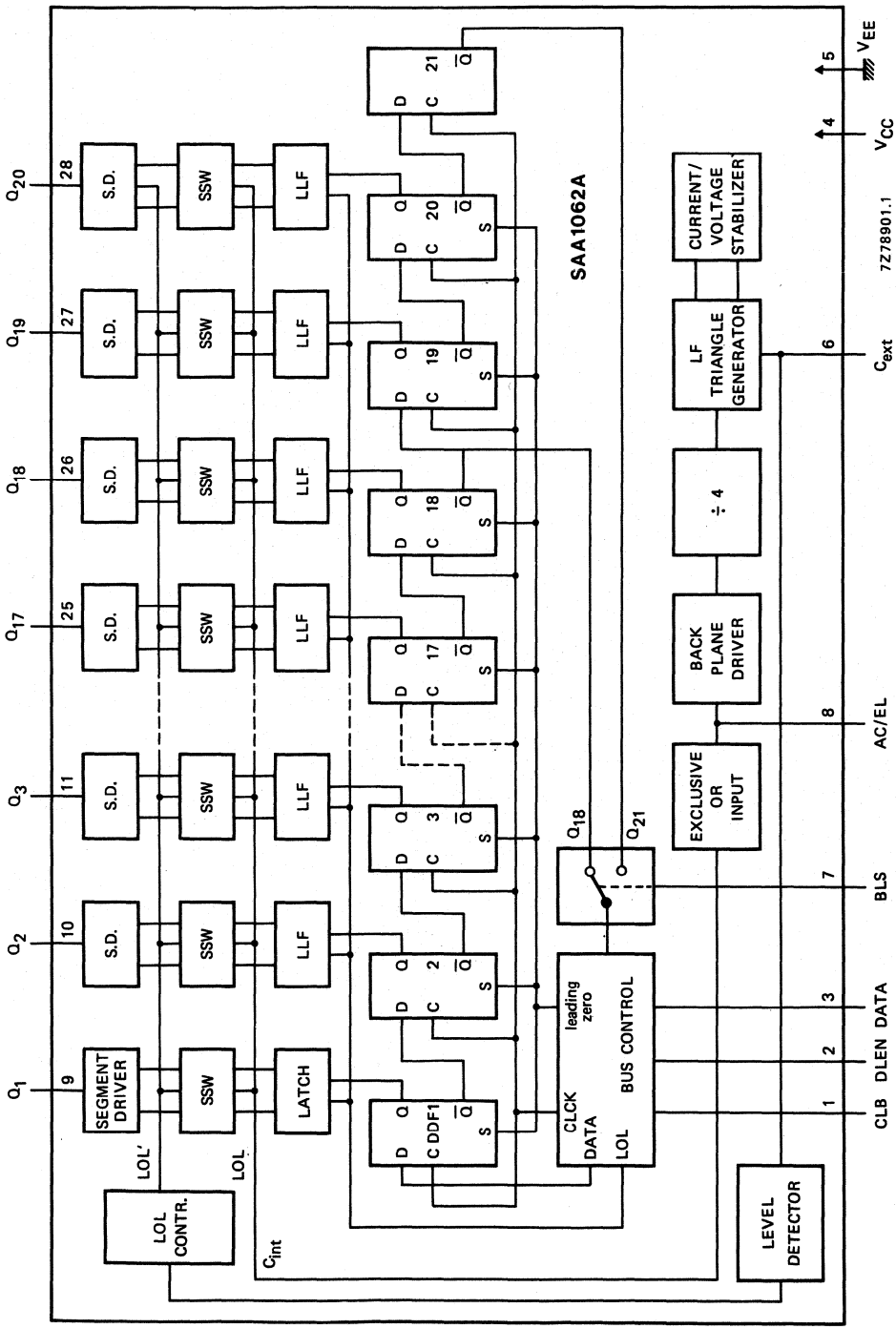


Fig. 2 Block diagram.

OPERATION DESCRIPTION

The input information for this device consists of a data bus with 18 or 21 bits words, an external clock synchronized with the data bus and an enable signal. The organization of these signals is given in Fig. 3. These signals are handled by the BUS CONTROL circuit in which the decision is made whether these signals are valid for the device. It contains a leading zero detector (start condition of reception) and a data-length control. Leading zero is detected when the data signal is LOW and the DLEN signal is HIGH, during the first HIGH period of the clock signal. During the HIGH period of DLEN, the length control determines if the clock signal consists of the programmed number of pulses (18 or 21). This last function permits the user to supply other information on the same signal lines.

Furthermore the bus control prevents the device from accepting inferferences on the signal lines. While leading zero is detected, the shift register is set and for a proper leading zero the following data is shifted into this register. The Q_n position of the first bit of the register is shifted into the last bit, if the length of the data and the clock input are correct. Incorrect length of the information is detected by checking the value of the last bit of the programmed register. If the data transmission has been accepted properly, the bus control stage generates a valid pulse (LOL).

This pulse enables the load control circuit to load the contents of the register into the output latch immediately. On the first edge of the backplane driver signal "AC out/EL in" following on this "LOL" pulse, the new information of this latch is transferred to the output driver which also contains a latch. With this ability it is possible to load the device with 20 bits and also to transfer this data to the segment outputs. Furthermore, the SR can be reloaded by a second complete load procedure without a load enable clock pulse. This causes the SR to contain 20 bits and the output latches another 20 bits of information.

The output driver also contains an EXCLUSIVE-OR which is driven by the backplane driver signal and the latch output. The segment driver output signal is in phase with the output of the backplane driver when the input data is HIGH ("1") and 180^o out-of-phase when the input data is LOW ("0").

In the static or slave mode, the backplane output can be used as input by connecting pin 6 to ground or V_{CC}. The IC now can operate as a static driver or as a synchronized slave.

The l.f. oscillator consists of a triangle generator of the I-2I principle. It only needs an external capacitor to fix the frequency. As both amplitude and current are temperature compensated, this frequency is more or less independent of pn temperature. An internal switching signal of this generator is divided by 4 to attain a symmetrical output for the backplane driver (pin 8) of nominal 60 Hz for an external capacitor of 22 nF.

The backplane driver is able to drive a 40 bits display.

The bit length of the shift register is programmed with BLS (Bit Length Selector) (pin 7). If BLS is kept LOW the DATA bit length is 20; for BLS open or HIGH a DATA bit length of 17 is selected.

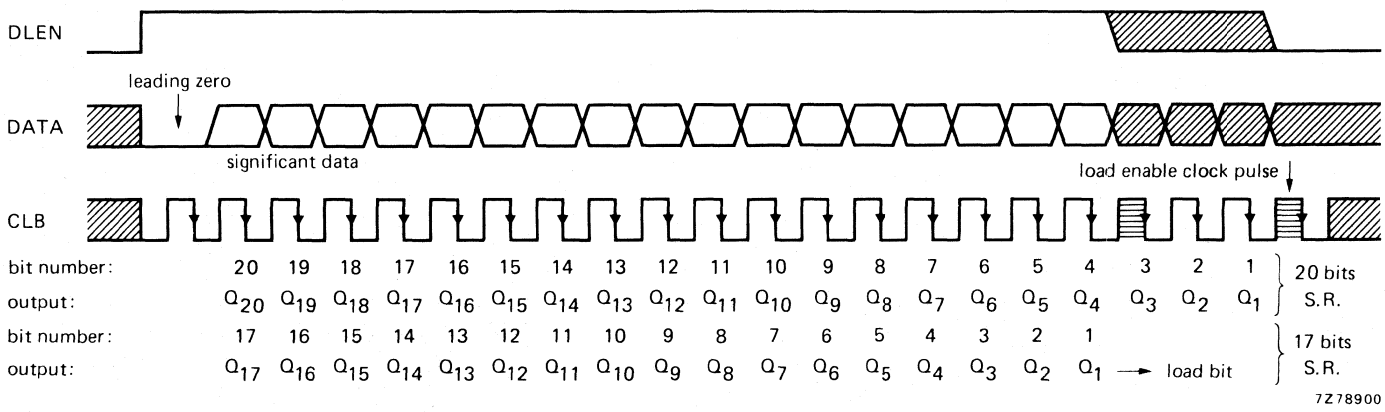


Fig. 3 Organization of 18 and 21 bit words; DATA = LOW means segment 'on'.

RATINGS (V_{EE} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	6 V
Total power dissipation at T_{amb} = 100 °C derate linearly with 0,02 W/°C	P_{tot}	max.	500 mW
Operating ambient temperature range	T_{amb}		−25 to + 125 °C
Storage temperature range	T_{stg}		−55 to + 125 °C

CHARACTERISTICS

V_{EE} = 0; V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		condition
Supply voltage	V_{CC}	4,2	5	5,5	V	
Supply current	I_{CC}	–	3,5	–	mA	
Inputs CLB, DLEN, DATA, BLS						
input voltage HIGH	V_{IH}	1,6	–	V_{CC}	V	
input voltage LOW	V_{IL}	−1	–	+ 0,8	V	
maximum input frequency	f_I	–	50	–	kHz	
Input C_{ext}						
input voltage HIGH	V_{IH}	4,6	–	–	V	static mode
input voltage LOW	V_{IL}	−0,1	–	0,4	V	sync. slave mode
input current HIGH	I_{IH}	–	–	180	μA	
input current LOW	I_{IL}	–	–	−40	μA	
Input AC/EL (in slave mode)						
input voltage HIGH	V_{IH}	2,7	–	V_{CC}	V	
input voltage LOW	V_{IL}	−0,4	–	2,3	V	
Output C_{ext} (oscillator mode)						
oscillator frequency	f_{osc}	120	240	360	Hz	C = 22 nF
Output stage backplane (AC/EL)						
output current sink/source	I_O	2,4	–	–	mA	
Output Q_1 to Q_{20}						
output current sink/source	I_O	60	–	–	μA	
d.c. rest voltage between pin 8 (AC/EL) and one of the segment drivers (see Fig. 4)						
segment 'on' situation		–	–	25	mV	
segment 'off' situation		–	–	25	mV	

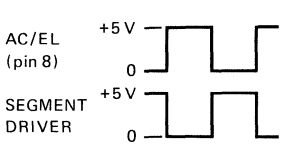


Fig. 4 AC/EL and segment driver pulses.
The d.c. voltage for segment 'on' is about 5 V.

MICROPROCESSOR CONTROLLED STEREO SOUND GENERATOR FOR SOUND EFFECTS AND MUSIC SYNTHESIS

GENERAL DESCRIPTION

The SAA1099 is a monolithic integrated circuit designed for generation of stereo sound effects and music synthesis.

Features

- Six frequency generators
  - eight octaves per generator
  - 256 tones per octave
- Two noise generators
- Six noise/frequency mixers
- Twelve amplitude controllers
- Two envelope controllers
- Two 6-channel mixers/current sink analogue output stages
- TTL input compatible
- Readily interfaces to 8-bit microcontroller
- Minimal peripheral components
- Simple output filtering

Applications

- Consumer games systems
- Home computers
- Electronic organs
- Arcade games
- Toys
- Chimes/alarm clocks

QUICK REFERENCE DATA

Supply voltage (pin 18)	V_{DD}	typ.	5 V
Supply current (pin 18)	I_{DD}	typ.	70 mA
Reference current (pin 6)	I_{ref}	typ.	250 μA
Total power dissipation	P_{tot}		500 mW
Operating ambient temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

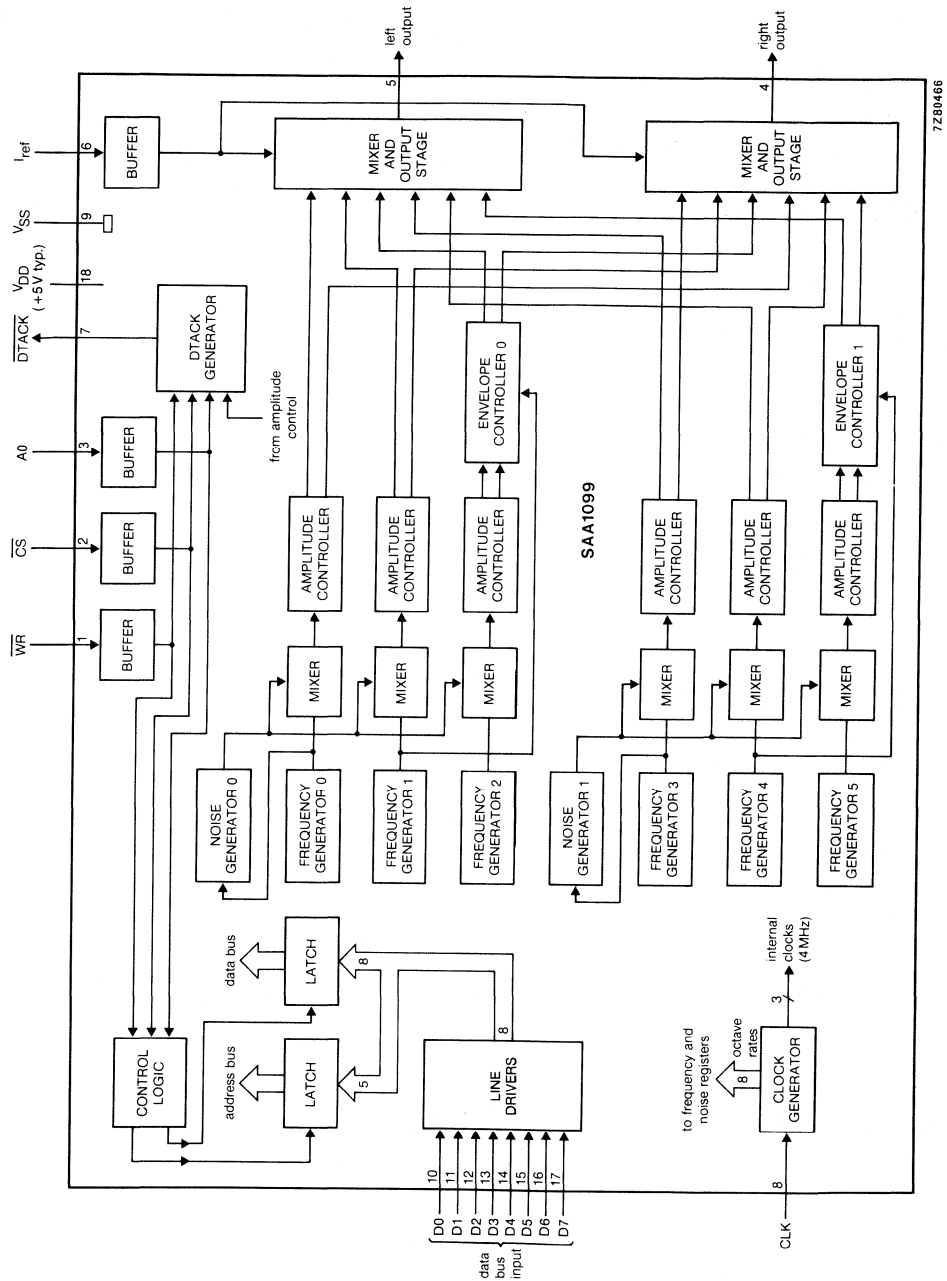


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

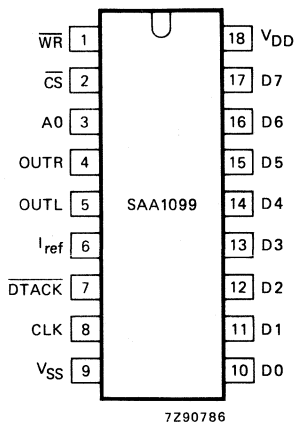


Fig. 2 Pinning diagram.

PIN DESIGNATION

1	$\overline{WR}$	**Write Enable**: active LOW input which operates in conjunction with $\overline{CS}$ and A0 to allow writing to the internal registers.
2	$\overline{CS}$	**Chip Select**: active LOW input to identify valid $\overline{WR}$ inputs to the chip. This input also operates in conjunction with $\overline{WR}$ and A0 to allow writing to the internal registers.
3	A0	**Control/Address select**: input used in conjunction with $\overline{WR}$ and $\overline{CS}$ to load data to the control register (A0 = 0) or the address buffer (A0 = 1).
4	OUTR	**Right channel output**: a 7-level current sink analogue output for the 'right' component. This pin requires an external load resistor.
5	OUTL	**Left channel output**: a 7-level current sink analogue output for the 'ieft' component. This pin requires an external load resistor.
6	I_{ref}	**Reference current supply**: used to bias the current sink outputs.
7	$\overline{DTACK}$	**Data Transfer Acknowledge**: open drain output, active LOW to acknowledge successful data transfer. On completion of the cycle $\overline{DTACK}$ is set to inactive.
8	CLK	**Clock**: input for an externally generated clock at a nominal frequency of 8 MHz.
9	V_{SS}	**Ground**: 0 V.
10-17	D0-D7	**Data**: Data bus input.
18	V_{DD}	**Power supply**: + 5 V typical.

FUNCTIONAL DESCRIPTION

The following sections provide a detailed functional description of the SAA1099 as shown in the block diagram, Fig. 1.

Frequency generators

Six frequency generators can each select one of 8 octaves and one of 256 tones within an octave. A total frequency range of 31 Hz to 7,81 kHz is available. The outputs may also control noise or envelope generators. All frequency generators have an enable bit which switches them on and off, making it possible to preselect a tone and to make it inaudible when required. The frequency generators may be synchronized using the frequency reset bit.

The frequency ranges per octave are:

Octave	Frequency range
0	31 Hz to 61 Hz
1	61 Hz to 122 Hz
2	122 Hz to 244 Hz
3	245 Hz to 488 Hz
4	489 Hz to 977 Hz
5	978 Hz to 1,95 kHz
6	1,96 kHz to 3,91 kHz
7	3,91 kHz to 7,81 kHz

Noise generators

The two noise generators both have a programmable output. This may be a software controlled noise via one of the frequency controlled generators or one of three pre-defined noises. There is no tone produced by the frequency generator when it is controlling the noise generator. The noise produced is based on double the frequency generator output, i.e. a range of 61 Hz to 15,6 kHz.

In the event of a pre-defined noise being chosen, the output of noise generator 0 can be mixed with frequency generator 0, 1 and 2; and the output of noise generator 1 can be mixed with frequency generator 3, 4 and 5. In order to produce an equal level of noise and tone outputs (when both are mixed) the amplitude of the tone is increased. The three pre-defined noises are based on a clock frequency of 7,8 kHz, 15,6 kHz or 31,25 kHz.

Noise/frequency mixers

Six noise/frequency mixers each with four selections

- Channel off
- Frequency only
- Noise only
- Noise and frequency

Each mixer channel has one of the frequency generator outputs fed to it, three channels use noise generator 0 and the other three use noise generator 1.

Amplitude controllers

Each of the six channel outputs from the mixer is split up into a right and left component giving effectively twelve amplitude controllers. An amplitude of 16 possible levels is assigned to each of the twelve signals. With this configuration a stereo effect can be achieved by varying only the amplitude component. The moving of a sound from one channel to the other requires, per tone, only one update of the amplitude register contents.

When an envelope generator is used, the amplitude levels are restricted. The number of levels available is then reduced to eight. This is achieved by disabling the least significant bit (LSB) of the amplitude control.

Envelope controllers

Two of the six tone generators are under envelope control. This applies to both the left and right outputs from the tone generator.
The envelope has the following eight possible modes:

- Amplitude is zero
- Single attack
- Single decay
- Single attack-decay (triangular)
- Maximum amplitude
- Continuous attack
- Continuous decay
- Continuous attack-decay

The timing of the envelope controllers is programmable using one of the frequency generators (see Fig. 1). When the envelope mode is selected for a channel its control resolution is halved for that channel from 16 levels to 8 levels by rounding down to the nearest even level.
There is also the capability of controlling the 'right' component of the channel with inverse of the 'left' component, which remains as programmed.

A direct enable permits the start of an envelope to be defined, and also allows termination of an envelope at any time. The envelope rate may be controlled by a frequency channel (see Fig. 1), or by the microprocessor writing to the address buffer register. If the frequency channel controlled is OFF (NE = FE = 0) the envelope will appear at the output, which provides an alternative 'non-square' tone capability. In this event the frequency will be the envelope rate, which provided the rate is from the frequency channel, will be a maximum of 1 kHz. Higher frequencies of up to 2 kHz can be obtained by the envelope resolution being halved from 16 levels to 8 levels. Rates quoted are based on the input of a 8 MHz clock.

Six-channel mixers/current sink analogue output stages

Six channels are mixed together by the two mixers allowing each one to control one of six equally weighted current sinks, to provide a seven level analogue output.

Command/control select

In order to simplify the microprocessor interface the command and control information is multiplexed. To select a register in order to control frequencies, amplitudes, etc. the command-register has to be loaded. The contents of this register determines to which register the data is written in the next control-cycle. If a continuous update of the control-register is necessary, only the control-information has to be written (the command-information does not change).
If the command/control select (A0) is logic 0, the byte transfer is control; if A0 is logic 1, the byte transfer is command.

Interface to microprocessor

The SAA1099 is a data bus based I/O peripheral. Depending on the value of the command/control signal (A0) the $\overline{CS}$ and $\overline{WR}$ signals control the data transfer from the microprocessor to the SAA1099. The data-transfer-acknowledge ($\overline{DTACK}$) indicates that the data transfer is completed. When, during the write cycle, the microprocessor recognizes the $\overline{DTACK}$, the bus cycle will be completed by the processor.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)	V_{DD}	−0,3 to + 7,5	V
Maximum input voltage	V_I	−0,3 to + 7,5	V
at V_{DD} = 4,5 to 5,5 V	V_I	−0,5 to + 7,5	V
Maximum output current	I_O	max. 10	mA
Total power dissipation	P_{tot}	500	mW
Storage temperature range	T_{stg}	−55 to + 125	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Electrostatic handling*	V_{es}	−1000 to + 1000	V

* Equivalent to discharging a 250 μF capacitor through a 1 kΩ series resistor.

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	70	100	mA
Reference current (note 1)	I_{ref}	100	250	400	μA
INPUTS					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	−0,5	–	0,8	V
Input leakage current	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	10	pF
OUTPUTS					
$\overline{DTACK}$ (open drain; note 2)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Voltage on pin 7 (OFF state)	V_{7-9}	−0,3	–	6,0	V
Output capacitance (OFF state)	C_O	–	–	10	pF
Load capacitance	C_L	–	–	150	pF
Output leakage current (OFF state)	$-I_{LO}$	–	–	10	μA
Audio outputs (pins 4 and 5)					
With fixed I_{ref} (note 3)					
One channel on	I_{01}/I_{ref}	90	–	120	%
Six channels on	$I_{06}/6xI_{ref}$	85	–	110	%
With I_{ref} = 250 μA; R_L = 1,5 kΩ (± 5%)					
One channel on	I_{01}/I_{ref}	90	–	110	%
Six channels on	$I_{06}/6xI_{ref}$	85	–	105	%
Output current one channel on	I_{01}	225	–	275	μA
Output current six channels on	I_{06}	1,3	–	1,6	mA
With resistor supplying I_{ref} (note 4)					
Output current one channel on	I_{01}	150	–	350	μA
Output current six channels on	I_{06}	0,9	–	1,9	mA
Load resistance	R_L	600	–	–	Ω
D.C. leakage current all channels off	$-I_{LO}$	–	–	10	μA
Maximum current difference between left and right current sinks (note 5)	$\pm I_{Omax}$	–	–	15	%
Signal-to-noise ratio (note 6)	S/N	–	tbf	–	dB

A.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; timing measurements taken at 2,0 V for a logic 1 and 0,8 V for a logic 0 unless otherwise specified (see waveforms Figs 3 and 4)

parameter	symbol	min.	typ.	max.	unit
Bus interface timing (see Fig. 3)					
A0 set-up time to $\overline{CS}$ fall	t_{ASC}	0	–	–	ns
$\overline{CS}$ LOW to $\overline{WR}$ fall	t_{CSW}	30	–	–	ns
A0 set-up time to $\overline{WR}$ fall	t_{ASW}	50	–	–	ns
$\overline{WR}$ LOW time	t_{WL}	100	–	–	ns
Data bus valid to $\overline{WR}$ rise	t_{BSW}	100	–	–	ns
$\overline{DTACK}$ fall delay from $\overline{WR}$ fall (note 7)	t_{DFW}	0	–	85	ns
A0 hold time from $\overline{WR}$ HIGH	t_{AHW}	0	–	–	ns
$\overline{CS}$ hold time from $\overline{WR}$ HIGH	t_{CHW}	0	–	–	ns
Data bus hold time from $\overline{WR}$ HIGH	t_{DHW}	0	–	–	ns
$\overline{DTACK}$ rise delay from $\overline{WR}$ HIGH	t_{DRW}	0	–	100	ns
Bus cycle time (note 8)	t_{CY}	$4t_{CLK}$	–	–	
Bus cycle time (note 9)	t_{CY}	$16t_{CLK}$	–	–	
Clock input timing (see Fig. 4)					
Clock period	t_{CLK}	120	125	255	ns
Clock LOW time	t_{LOW}	55	–	–	ns
Clock HIGH time	t_{HIGH}	55	–	–	ns

Notes to the characteristics

1. Using an external constant current generator to provide a nominal I_{ref} or external resistor connected to V_{DD}.
2. This output is short-circuit protected to V_{DD} and V_{SS}.
3. Measured with I_{ref} a constant value between 100 and 400 μA; load resistance (R_L) allowed to match E12 (5%) in all applications via:

$$R_L = 0{,}6\ [I_{ref}]^{-1} - 16\ [I_{ref}]^{-0{,}5} \pm 12\%$$

4. Measured with R_{ref} = 10 kΩ (± 5%) connected between I_{ref} and V_{DD}; R_L = 1,5 kΩ (± 5%); OUTR and OUTL short-circuit protected to V_{SS}.
5. Left and right outputs must be driven with identical configuration.
6. Sample tested value only.
7. This timing parameter only applies when no wait states are required; otherwise parameter is invalid.
8. The minimum bus cycle time of four clock periods is for loading all registers except the amplitude registers.
9. The minimum bus cycle time of 16 clock periods is for loading the amplitude registers. In a system using $\overline{DTACK}$ it is possible to achieve minimum times of 500 ns. Without $\overline{DTACK}$ the parameter given must be used.

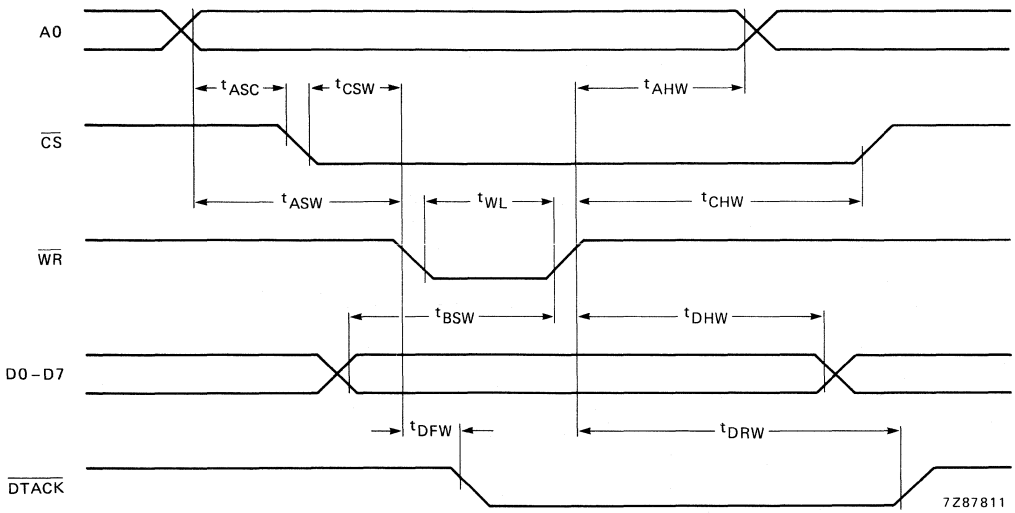


Fig. 3 Bus interface waveforms.

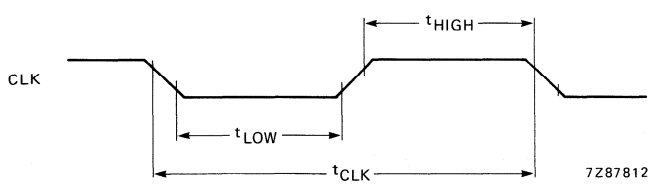


Fig. 4 Clock input waveform.

DEVELOPMENT DATA

APPLICATION INFORMATION

Device operation

The SAA1099 uses pulse width modulation to achieve amplitude and envelope levels. The twelve signals are mixed in an analogue format (6 'left' and 6 'right') before leaving the chip. The amplitude and envelope signals chop the output at a minimum rate of 62,5 kHz, compared with the highest tone output of 7,81 kHz. Simple external low-pass filtering is used to remove the high frequency components.

Rates quoted are based on the input of a 8 MHz clock.

A data bus based write only structure is used to load the on-board registers. The data bus is used to load the address for a register, and subsequently the data to that register. Once the address is loaded multiple data loads to that register can be performed.

The selection of address or data is made by the single address bit A0, as shown in register maps Table 1 and Table 2.

The bus control signals $\overline{WR}$ and $\overline{CS}$ are designed to be compatible with a wide range of microprocessors, a $\overline{DTACK}$ output is included to optimise the interface with an S68000 series microprocessor. In most bus cycles $\overline{DTACK}$ will be returned immediately, this applies to all register address load cycles and all except amplitude data load cycles. With respect to amplitude data, a number of wait cycles may need to be performed, depending on the time since the previous amplitude load. $\overline{DTACK}$ will indicate the number of required waits.

Register description (see Tables 2 and 3)

The amplitudes are assigned with 'left' and 'right' components in the same byte, on a channel by channel basis. The spare locations that are left between blocks of registers is to allow for future expansion, and should be written as zero's. The tone within an octave is defined by eight bits and the octave by three bits. Note that octaves are paired (0/1, 2/3 etc.). The frequency and noise enables are grouped together for ease of programming. The controls for noise 'colour' (clock rate) are grouped in one byte.

The envelope registers are positioned in adjacent locations. There are two types of envelope controls, direct acting controls and buffered controls. The direct acting controls always take immediate effect, and are:

- Envelope enable (reset)
- Envelope resolution (16/8 level)

The buffered controls are acted upon only at the times shown in Fig. 5 and control selection of:

- Envelope clock source
- Waveform type
- Inverted/non-inverted 'right' component

Table 1 External memory map

select	data bus inputs								operations
A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	D7	D6	D5	D4	D3	D2	D1	D0	data for internal registers
1	X	X	X	A4	A3	A2	A1	A0	internal register address

Where X = don't care state.

Table 2 Internal register map.

register address	data bus inputs D7	D6	D5	D4	D3	D2	D1	D0	operations
00	AR03	AR02	AR01	AR00	AL03	AL02	AL01	AL00	amplitude 0 right channel; left channel
01	1	1	1	1	1	1	1	1	amplitude 1 right/left
02	2	2	2	2	2	2	2	2	amplitude 2 right/left
03	3	3	3	3	3	3	3	3	amplitude 3 right/left
04	4	4	4	4	4	4	4	4	amplitude 4 right/left
05	5	5	5	5	5	5	5	5	amplitude 5 right/left
06	X	X	X	X	X	X	X	X	
07	X	X	X	X	X	X	X	X	
08	F07	F06	F05	F04	F03	F02	F01	F00	frequency of tone 0
09	1	1	1	1	1	1	1	1	frequency of tone 1
0A	2	2	2	2	2	2	2	2	frequency of tone 2
0B	3	3	3	3	3	3	3	3	frequency of tone 3
0C	4	4	4	4	4	4	4	4	frequency of tone 4
0D	F57	F56	F55	F54	F53	F52	F51	F50	frequency of tone 5
0E	X	X	X	X	X	X	X	X	
0F	X	X	X	X	X	X	X	X	
10	X	012	011	010	X	002	001	000	octave 1; octave 0
11	X	032	031	030	X	022	021	020	octave 3; octave 2
12	X	052	051	050	X	042	041	040	octave 5; octave 4
13	X	X	X	X	X	X	X	X	
14	X	X	FE5	FE4	FE3	FE2	FE1	FE0	frequency enable
15	X	X	NE5	NE4	NE3	NE2	NE1	NE0	noise enable
16	X	X	N11	N10	X	X	N01	N00	noise generator 1; noise generator 0
17	X	X	X	X	X	X	X	X	
18	E07	X	E05	E04	E03	E02	E01	E00	envelope generator 0
19	E17	X	E15	E14	E13	E12	E11	E10	envelope generator 1
1A	X	X	X	X	X	X	X	X	
1B	X	X	X	X	X	X	X	X	
1C	X	X	X	X	X	X	RST	SE	frequency reset (all channels) / sound enable (all channels)
1D	X	X	X	X	X	X	X	X	
1E	X	X	X	X	X	X	X	X	
1F	X	X	X	X	X	X	X	X	

Where:
All don't cares (X) should be written as zero's.
00 to 1F block of registers repeats eight times in the block between addresses 00 to FF (full internal memory map).

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

Table 3 Register description

bit	description
ARn3; ARn2; ARn1; ARn0 (n = 0,5)	4 bits for amplitude control of right channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
ALn3; ALn2; ALn1; ALn0 (n = 0,5)	4 bits for amplitude control of left channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
Fn7 to Fn0 (n = 0,5)	8 bits for frequency control of the six frequency generators 0 0 0 0 0 0 0 0 lowest frequency 1 1 1 1 1 1 1 1 highest frequency
On2; On1; On0 (n = 0,5)	3 bits for octave control 0 0 0 lowest octave (31 Hz to 61 Hz) 0 0 1 (61 Hz to 122 Hz) 0 1 0 (122 Hz to 244 Hz) 0 1 1 (245 Hz to 488 Hz) 1 0 0 (489 Hz to 977 Hz) 1 0 1 (978 Hz to 1,95 kHz) 1 1 0 (1,96 kHz to 3,91 kHz) 1 1 1 highest octave (3,91 kHz to 7,81 kHz)
FEn (n = 0,5)	frequency enable bit (one tone per generator) FEn = 0 indicates that frequency 'n' is off
NEn (n = 0,5)	noise enable bit (one tone per generator) NEn = 0 indicates that noise 'n' is off
Nn1; Nn0 (n = 0,1)	2 bits for noise generator control. These bits select the noise generator rate (noise 'colour') Nn1 Nn0 clock frequency 0 0 31,3 kHz 0 1 15,6 kHz 1 0 7,6 kHz 1 1 61 Hz to 15,6 kHz (frequency generator 0/3)

bit	description
En7; En5 to En0 (n = 0,1)	7 bits for envelope control En0 0 left and right component have the same envelope 1 right component has inverse of envelope that is applied to left component En3 En2 En1 0 0 0 zero amplitude 0 0 1 maximum amplitude 0 1 0 single decay 0 1 1 repetitive decay 1 0 0 single triangular 1 0 1 repetitive triangular 1 1 0 single attack 1 1 1 repetitive attack En4 0 4 bits for envelope control (maximum frequency = 977 Hz) 1 3 bits for envelope control (maximum frequency = 1,95 kHz) En5 0 internal envelope clock (frequency generator 1 or 4) 1 external envelope clock (address write pulse) En7 0 reset (no envelope control) 1 envelope control enabled
SE	SE sound enable for all channels (reset on power-up to 0) 0 all channels disabled 1 all channels enabled
RST	Reset signal to all frequency generators 0 all generators enabled 1 all generators reset and synchronized

Note

All rates given are based on the input of a 8 MHz clock.

APPLICATION INFORMATION (continued)

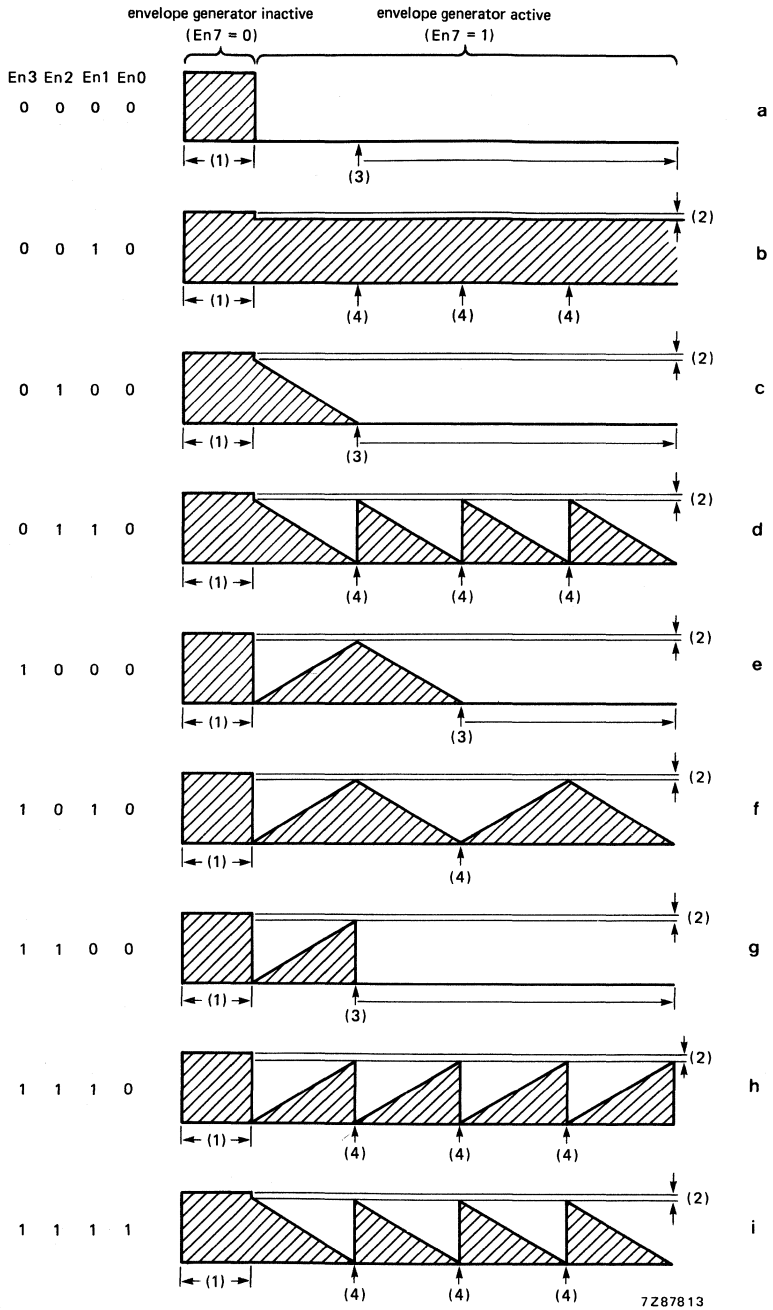


Fig. 5 Envelope waveforms.

Notes to Fig. 5

(1) The level at this time is under amplitude control only (En7 = 0; no envelope).

(2) When the generator is active (En7 = 1) the maximum level possible is 7/8ths of the amplitude level.

(3) After position (3) the buffered controls will be acted upon when loaded.

(4) At positions (4) the buffered controls will be acted upon if already loaded.

(5) Waveforms 'a' to 'h' show the left channel (En0 = 0; left and right components have the same envelope).
Waveform 'i' shows the right channel (En0 = 1; right component inverse of envelope applied to left).

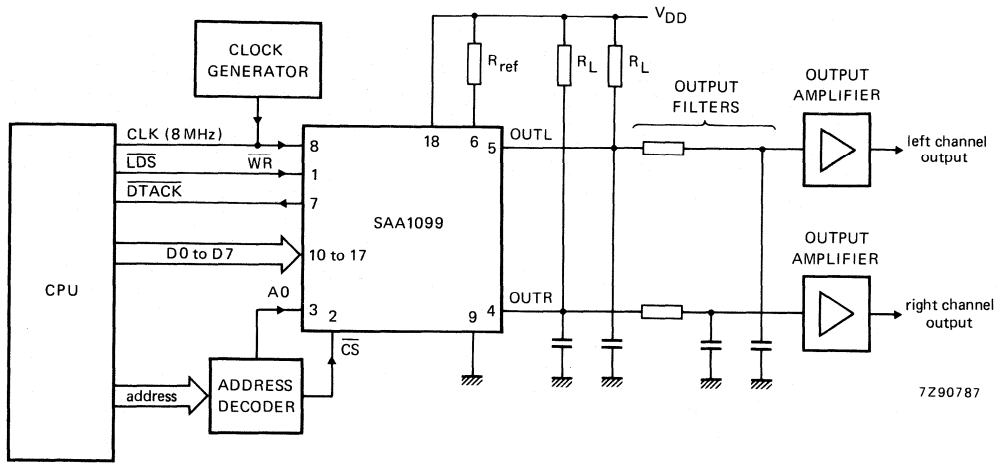


Fig. 6 Typical application circuit diagram.

TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I^2C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 100 mA in the ON state or sinking up to $-100\ \mu A$ in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I^2C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I^2C bus. A subaddressing system allows the connection of up to three circuits on the same I^2C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

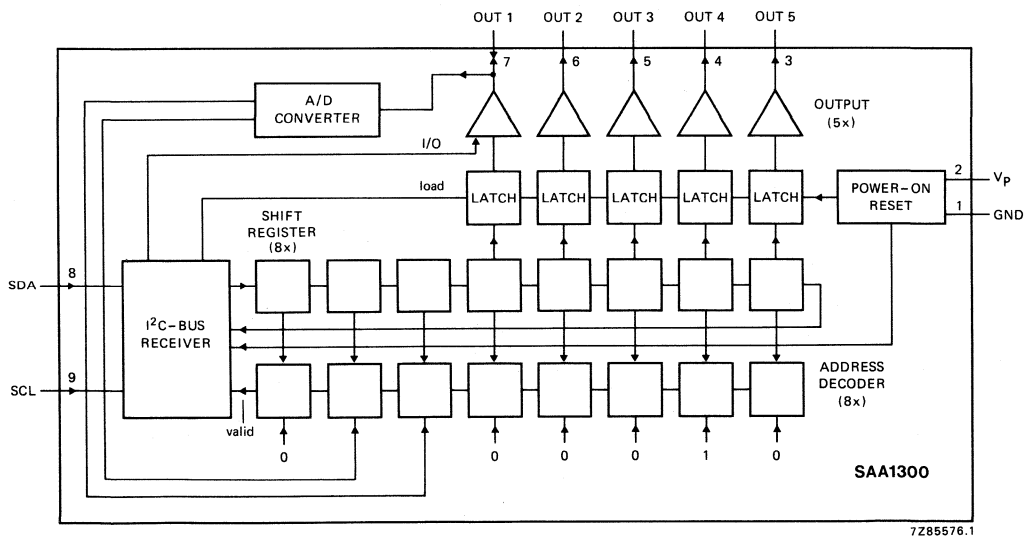


Fig. 1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142B).

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line (I^2C bus)
9	SCL	serial clock line (I^2C bus)

I^2C BUS INFORMATION

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max. 13,2	V
Input voltage range at SDA, SCL	V_I	−0,5 to + 13,7	V
Input voltage range at OUT 1	V_I	−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O	−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max. 20	mA
Input current at OUT 1	I_I	max. 20	mA
Total power dissipation	P_{tot}	max. 650	mW
Storage temperature range	T_{stg}	−40 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 80	°C

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 2)					
Supply voltage range	V_P	4	–	12	V
Supply current	I_P	–	10	–	mA
Power-on reset level output stage in "OFF" condition	V_{PR}	–	–	3,5	V
Maximum power dissipation*	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	2,8	–	V_P + 0,5	V
Input voltage LOW	V_{IL}	0	–	1,8	V
Input current HIGH	$-I_{IH}$	–	–	50	μA
Input current LOW	I_{IH}	–	–	0,1	μA
Acknowledge sink current	I_{ACK}	2,5	–	–	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source : "ON"	I_{Oso}	+ 100	–	+ 150	mA
Maximum output current; source : "ON" T_{amb} = 80 °C	I_{Oso}	60	–	–	mA
Output voltage HIGH at I_{Oso}	V_{OH}	–	–	V_P –2	V
Output current; sink: "OFF"	I_{Osi}	–100	–300	–	μA
Output voltage LOW at I_{Osi}	V_{OL}	–	–	100	mV
Output voltage MEDIUM at I_O = 12,5 mA	V_{OM}	–	–	V_P –0,5	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V

* Outputs must not be driven simultaneously at maximum source current.

REMOTE CONTROL TRANSMITTER

GENERAL DESCRIPTION

The SAA3004 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The SAA3004 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

The SAA3004 has the following features:

- Flashed or modulated transmission
- 7 sub-system addresses
- Up to 64 commands per sub-system address
- High-current remote output at $V_{DD} = 6$ V ($-I_{OH} = 40$ mA)
- Low number of additional components
- Key release detection by toggle bits
- Very low stand-by current ($< 2\ \mu A$)
- Operational current < 2 mA at 6 V supply
- Wide supply voltage range (4 to 11 V)
- Ceramic resonator controlled frequency (typ. 450 kHz)
- Encapsulation: 20-lead plastic DIL or 20-lead plastic mini-pack (SO-20)

PACKAGE OUTLINES

SAA3004P: 20-lead DIL; plastic (SOT-146C1).
SAA3004T: 20-lead mini-pack; plastic (SO-20; SOT-163AC3).

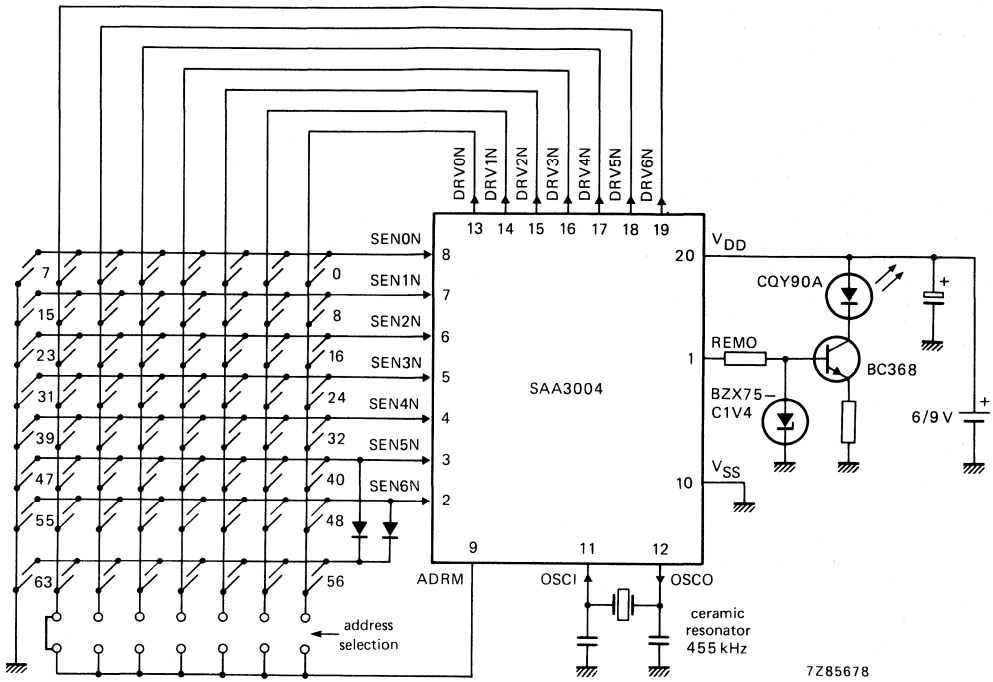


Fig. 1 Transmitter with SAA3004.

INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N)

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in Fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable.The sense inputs have P-channel pull-up transistors, so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

Address mode input (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode. This allows the definition of seven sub-system addresses as shown in Table 3. If driver DRV6N is connected to ADRM the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by presssing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnN with the highest number (n) defines the sub-system address, e.g. if driver DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in transmitters for more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4.

A change of the sub-system address will not start a transmission.

Remote control signal output (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in Tables 1 and 2.

The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see Fig. 3).

The format of the output data is given in Figs 2 and 3. In the flashed transmission mode the data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A, which are defined by the selected key.

In the modulated transmission mode the first toggle bit T1 is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence.

The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command.

The codes for the sub-system address and the selected key are given in Tables 3 and 4.

Oscillator input/output (OSCI and OSCO)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 400 kHz and 500 kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation

In the stand-by mode all drivers (DRV0N to DRV6N) are on. Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see Fig. 4) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch. In contradiction to the command code the sub-system address is sensed only within the *first* scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key-stroke sequence (see Fig. 5) the command code is always altered in accordance with the sensed key.

Multiple key-stroke protection

The keyboard is protected against multiple key-strokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see Fig. 5). In case of a multiple key-stroke the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix:

FUNCTIONAL DESCRIPTION (continued)

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored.
- SEN5N and SEN6N are not protected against multiple key-stroke on the same driver line, because this condition has been used for the definition of additional codes (code numbers 56 to 63).

Output sequence (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in Figs 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see Fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

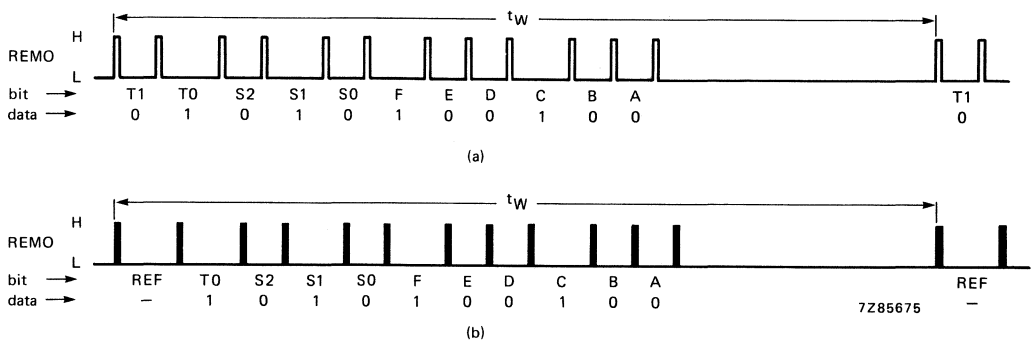
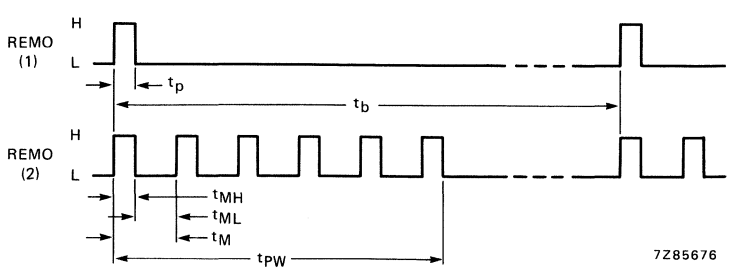


Fig. 2 Data format of REMO output; REF = reference time; T0 and T1 = toggle bits; S0, S1 and S2 = system address; A, B, C, D, E and F = command bits.
(a) flashed mode: transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed).
(b) modulated mode: transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).



(1) Flashed pulse.
(2) Modulated pulse ($t_{PW} = (5 \times t_M) + t_{MH}$.

Fig. 3 REMO output waveform.

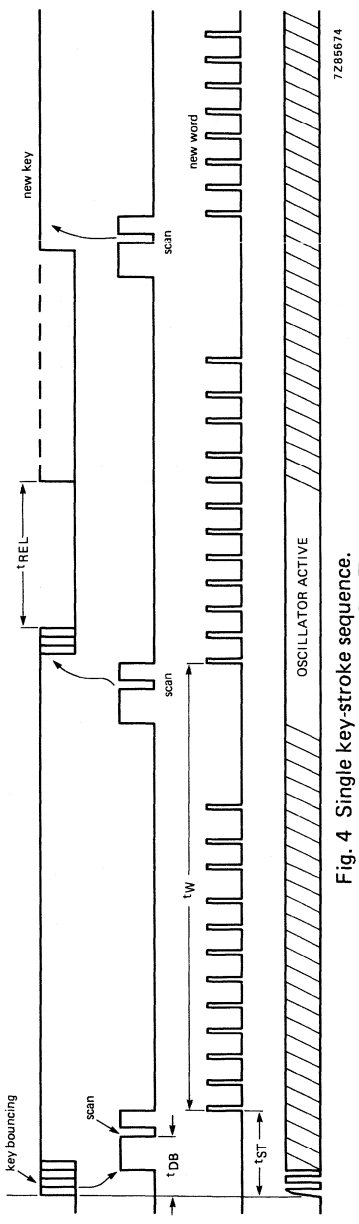


Fig. 4 Single key-stroke sequence.
Debounce time: $t_{DB} = 4$ to $9 \times T_O$.
Start time: $t_{ST} = 5$ to $10 \times T_O$.
Minimum release time: $t_{REL} = T_O$.
Word distance: t_W.

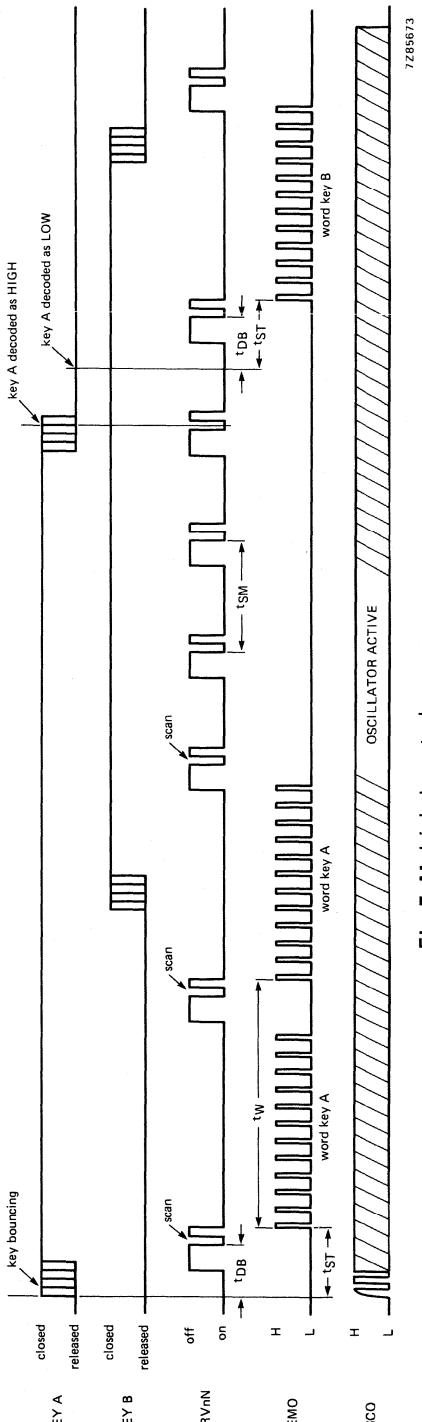


Fig. 5 Multiple key-stroke sequence.
Scan rate multiple key-stroke: $t_{SM} = 6$ to $10 \times T_O$.
For t_{DB}, t_{ST} and t_W see Fig. 4.

Table 1 Pulse train timing

mode	T_o ms	t_p μs	t_M μs	t_{ML} μs	t_{MH} μs	t_W ms
flashed	2,53	8,8	–	–	–	121
modulated	2,53	–	26,4	17,6	8,8	121

f_{osc}	455 kHz	$t_{osc} = 2{,}2\ \mu s$
t_p	$4 \times t_{osc}$	flashed pulse width
t_M	$12 \times t_{osc}$	modulation period
t_{ML}	$8 \times t_{osc}$	modulation period LOW
t_{MH}	$4 \times t_{osc}$	modulation period HIGH
T_o	$1152 \times t_{osc}$	basic unit of pulse distance
t_W	$55\,296 \times t_{osc}$	word distance

Table 2 Pulse train separation (t_b)

code	t_b
logic "0"	$2 \times T_o$
logic "1"	$3 \times T_o$
reference time	$3 \times T_o$
toggle bit time	$2 \times T_o$ or $3 \times T_o$

Table 3 Transmission mode and sub-system address selection

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode.

mode	sub-system address				driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	o						
A	2	0	0	1	X	o					
S	3	0	1	0	X	X	o				
H	4	0	1	1	X	X	X	o			
E	5	1	0	0	X	X	X	X	o		
D	6	1	0	1	X	X	X	X	X	o	
M											
O	0	1	1	1							o
D	1	0	0	0	o						o
U	2	0	0	1	X	o					o
L	3	0	1	0	X	X	o				o
A	4	0	1	1	X	X	X	o			o
T	5	1	0	0	X	X	X	X	o		o
E	6	1	0	1	X	X	X	X	X	o	o
D											

o = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 Key codes

matrix drive	matrix sense	code F	E	D	C	B	A	matrix position
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
*	SEN1N	0	0	1		**		8 to 15
*	SEN2N	0	1	0		**		16 to 23
*	SEN3N	0	1	1		**		24 to 31
*	SEN4N	1	0	0		**		32 to 39
*	SEN5N	1	0	1		**		40 to 47
*	SEN6N	1	1	0		**		48 to 55
*	SEN5N and SEN6N	1	1	1		**		56 to 63

* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5N/SEN6N.

** The C, B and A codes are identical to SEN0N as given above.

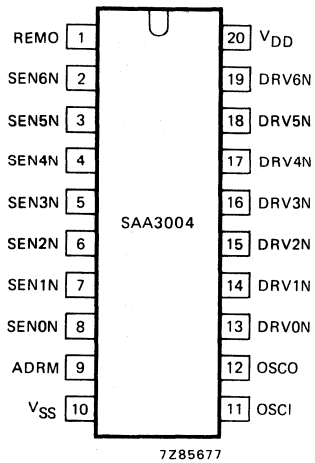


Fig. 6 Pinning diagram.

PINNING

1	REMO	remote data output
2	SEN6N	key matrix sense inputs
3	SEN5N	
4	SEN4N	
5	SEN3N	
6	SEN2N	
7	SEN1N	
8	SEN0N	
9	ADRM	address mode control input
10	V_{SS}	ground
11	OSCI	oscillator input
12	OSCO	oscillator output
13	DRV0N	key matrix drive outputs
14	DRV1N	
15	DRV2N	
16	DRV3N	
17	DRV4N	
18	DRV5N	
19	DRV6N	
20	V_{DD}	positive supply

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to +15		V
Input voltage range	V_I	−0,5 to V_{DD} +0,5		V
Output voltage range	V_O	−0,5 to V_{DD} +0,5		V
D.C. current into any input or output	±I	max.	10	mA
Peak REMO output current during 10 μs; duty factor = 1%	$-I_{(REMO)M}$	max.	300	mA
Power dissipation per package for T_{amb} = −20 to +70 °C	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−55 to +150		°C
Operating ambient temperature range	T_{amb}	−20 to +70		°C

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage						
T_{amb} = 0 to +70 °C	–	V_{DD}	4	–	11	V
Supply current; active						
f_{osc} = 455 kHz;	6	I_{DD}	–	1	–	mA
REMO output unloaded	9	I_{DD}	–	3	–	mA
Supply current; inactive						
(stand-by mode)	6	I_{DD}	–	–	2	μA
T_{amb} = 25 °C	9	I_{DD}	–	–	2	μA
Oscillator frequency						
(ceramic resonator)	4 to 11	f_{osc}	400	–	500	kHz
Keyboard matrix						
Inputs SEN0N to SEN6N						
Input voltage LOW	4 to 11	V_{IL}	–	–	0,2 x V_{DD}	V
Input voltage HIGH	4 to 11	V_{IH}	0,8 x V_{DD}	–	–	V
Input current	4	$-I_I$	10	–	100	μA
V_I = 0 V	11	$-I_I$	30	–	300	μA
Input leakage current						
V_I = V_{DD}	11	I_I	–	–	1	μA
Outputs DRV0N to DRV6N						
Output voltage "ON"						
I_O = 0,1 mA	4	V_{OL}	–	–	0,3	V
I_O = 1,0 mA	11	V_{OL}	–	–	0,5	V
Output current "OFF"						
V_O = 11 V	11	I_O	–	–	10	μA
Control input ADRM						
Input voltage LOW	–	V_{IL}	–	–	0,8 x V_{DD}	V
Input voltage HIGH	–	V_{IH}	0,2 x V_{DD}	–	–	V
Input current (switched P- and N-channel pull-up/ pull-down)						
Pull-up active	4	I_{IL}	10	–	100	μA
stand-by voltage: 0 V	11	I_{IL}	30	–	300	μA
Pull-down active	4	I_{IH}	10	–	100	μA
stand-by voltage: V_{DD}	11	I_{IH}	30	–	300	μA

CHARACTERISTICS (continued)

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Data output REMO						
Output voltage HIGH	6	V_{OH}	3	–	–	V
$-I_{OH}$ = 40 mA	9	V_{OH}	6	–	–	V
Output voltage LOW	6	V_{OL}	–	–	0,2	V
I_{OL} = 0,3 mA	9	V_{OL}	–	–	0,1	V
Oscillator						
Input current OSCI at V_{DD}	6	I_I	0,8	–	2,7	μA
Output voltage HIGH $-I_{OL}$ = 0,1 mA	6	V_{OH}	–	–	V_{DD}–0,6	V
Output voltage LOW I_{OH} = 0,1 mA	6	V_{OL}	–	–	0,6	V

LOW VOLTAGE INFRARED REMOTE CONTROL TRANSMITTER (RC-5)

GENERAL DESCRIPTION

The SAA3006 is intended as a general purpose (RC-5) infrared remote control system for use where only low supply voltages are available. The device can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified later in this publication (see KEY ACTIVITIES).

Features

- Low supply voltage requirements
- Very low current consumption
- For infrared transmission link
- Transmitter for 32 x 64 commands
- One transmitter controls 32 systems
- Transmission biphase technique
- Short transmission times; speed-up of system reaction time
- Single-pin oscillator input
- Input protection
- Test mode facility

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	2 to 7	V
Input voltage range	V_I	0,5 to (V_{DD} + 0,5)	V*
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,5 to (V_{DD} + 0,5)	V*
Output current	$\pm I_O$	max. 10	mA
Operating ambient temperature range	T_{amb}	−25 to +85	°C

* V_{DD} + 0,5 V not to exceed 9 V.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

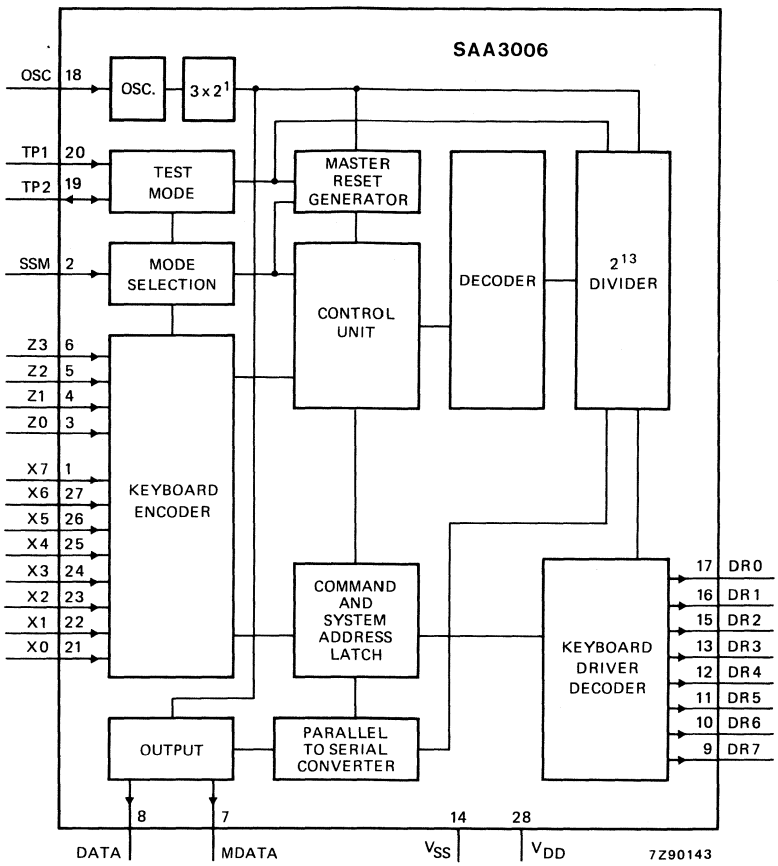


Fig. 1 Block diagram.

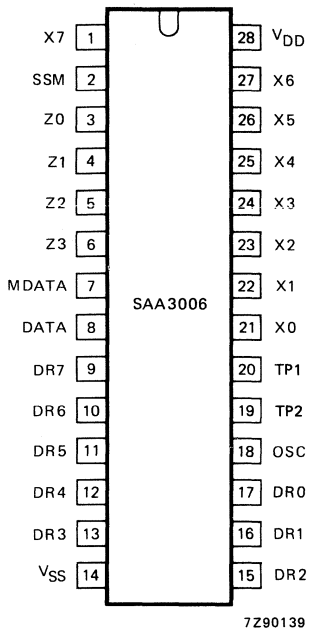
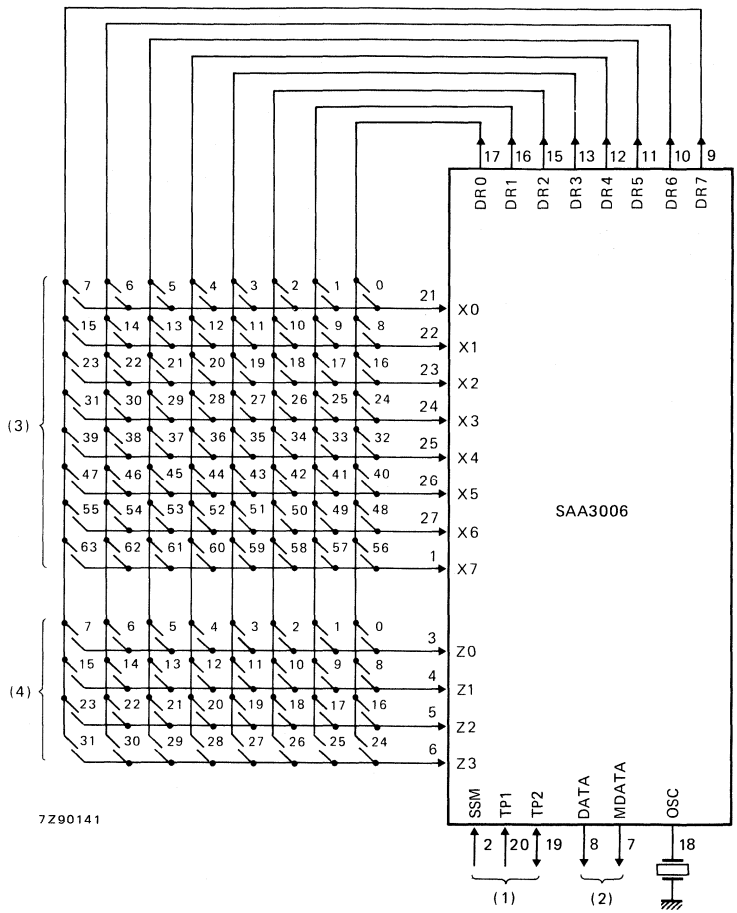


Fig. 2 Pinning diagram.

PINNING

14	V_{SS}	negative supply (ground)
28	V_{DD}	positive supply
21	X0	keyboard command inputs with P-channel pull-up transistors
22	X1	
23	X2	
24	X3	
25	X4	
26	X5	
27	X6	
1	X7	
3	Z0	keyboard system inputs with P-channel pull-up transistors
4	Z1	
5	Z2	
6	Z3	
2	SSM	system mode selection input
20	TP1	test input
19	TP2	test input/output
18	OSC	oscillator input
17	DR0	scan driver output with open drain N-channel transistors
16	DR1	
15	DR2	
13	DR3	
12	DR4	
11	DR5	
10	DR6	
9	DR7	
7	MDATA	remote signal outputs (3-state outputs)
8	DATA	



(1) Control inputs for operating modes, test modes and reset.
(2) Remote signal outputs.
(3) Keyboard command code matrix 8 x 8.
(4) Keyboard system code matrix 4 x 8.

Fig. 3 Keyboard interconnection.

FUNCTIONAL DESCRIPTION

Combined system mode (SSM = LOW)

The X and Z-lines are active HIGH in the quiescent state. Legal key operation either in the X-DR or Z-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the DR-outputs are switched off and two scan cycles are started, switching on the DR-outputs one by one. When a Z- or X-input senses a LOW level, a latch-enable signal is fed to the system address or command latches, depending on whether sensing was found in the Z- or X-input matrix. After latching a system address number, the device will generate the last command (i.e. all command bits '1') in the chosen system as long as the key is pressed. Latching of a command number causes the device to generate this command together with the system address number stored in the system address latch. Releasing the key will reset the internal action if no data is transmitted at that time. Once the transmission is started, the signal will be finished completely.

Single system mode (SSM = HIGH)

The X-lines are active HIGH in the quiescent state; the pull-up transistors of the Z-lines are switched off and the inputs are disabled. Only legal key operation in the X-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the pull-up transistors in the X-lines are switched off, those in the Z-lines are switched on during the first scan cycle. The wired connection in the Z-matrix is then translated into a system address number and stored in the system address latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again, while the transistors in the X-lines are switched on. The second scan cycle produces the command number which, after latching, is transmitted together with the system address number.

Inputs

The command inputs X0 to X7 carry a logical '1' in the quiescent state by means of an internal pull-up transistor. When SSM is LOW, the system inputs Z0 to Z3 also carry a logical '1' in the quiescent state by means of an internal pull-up transistor.

When SSM is HIGH, the transistors are switched off and no current flows via the wired connection in the Z-DR matrix.

Oscillator

The oscillator is formed by a ceramic resonator (catalogue number 2422 540 98021 or equivalent) feeding the single-pin input OSC. Direct connection is made for supply voltages in the range 2 to 5,25 V but it is necessary to fit a 10 kΩ resistor in series with the resonator when using supply voltages in the range 2,6 to 7 V.

Key-release detection

An extra control bit is added which will be complemented after key-release. In this way the decoder gets an indication that shows if the next code is to be considered as a new command. This is very important for multi-digit entry (e.g. by channel numbers or Teletext/Viewdata pages). The control bit will only be complemented after finishing at least one code transmission. The scan cycles are repeated before every code transmission, so that, even by 'take-over' of key operation during code transmission, the correct system and command numbers are generated.

FUNCTIONAL DESCRIPTION (continued)

Outputs

The output DATA carries the generated information according to the format given in Fig. 4 and Tables 2 and 3. The code is transmitted in biphase; definitions of logical '1' and '0' are given in Fig. 5.

The code consists of four parts:

- Start part formed by 2 bits (two times a logical '1');
- Control part formed by 1 bit;
- System part formed by 5 bits;
- Command part formed by 6 bits.

The output MDATA carries the same information as output DATA but is modulated on a carrier frequency of 1/12 of the oscillator frequency, so that each bit is presented as a burst of 32 pulses. To reduce power consumption, the carrier frequency has a 25% duty cycle.

In the quiescent state, both outputs are non-conducting (3-state outputs). The scan drivers DR0 to DR7 are of the open drain N-channel type and are conducting in the quiescent state of the circuit. After a legal key operation all the driver outputs go into the high ohmic state; a scanning procedure is then started so that the outputs are switched into the conducting state one after the other.

Reset action

The circuit will be reset immediately when a key release occurs during:

- debounce time;
- between two codes.

When a key release occurs during scanning of the matrix, a reset action will be accomplished if:

- the key is released while one of the driver outputs is in the low-ohmic '0' state;
- the key is released before detection of that key;
- there is no wired connection in the Z-DR matrix while SSM is HIGH.

Test pin

The test pins TP1 and TP2 are used for testing in conjunction with inputs Z2 and Z3 as shown in Table 1.

Table 1 Test functions

TP1	TP2	Z2	Z3	function
LOW	LOW	matrix input	matrix input	normal
LOW	HIGH	matrix input	matrix input	scan + output frequency six times faster than normal
HIGH	output $f_{OSC}{}^{6}$	LOW	LOW	reset
HIGH	output $f_{OSC}{}^{6}$	HIGH	HIGH	output frequency 3×2^{7} faster than normal

KEY ACTIVITIES

Every connection of one X-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating more than one X-input at a time is an illegal keyboard operation and no circuit action is taken (oscillator does not start).

When SSM is LOW, every connection of one Z-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating two or more Z-inputs, or Z-inputs and X-inputs, at one time is an illegal keyboard operation and no circuit action is taken.

When SSM is HIGH, a wired connection must be made between a Z-input and a DR-output. If no connection is made, the code is not generated.

When one X or Z-input is connected to more than one DR-output, the last scan signal is considered legal.

The maximum allowable value of the contact series resistance of the keyboard switches is 7 kΩ.

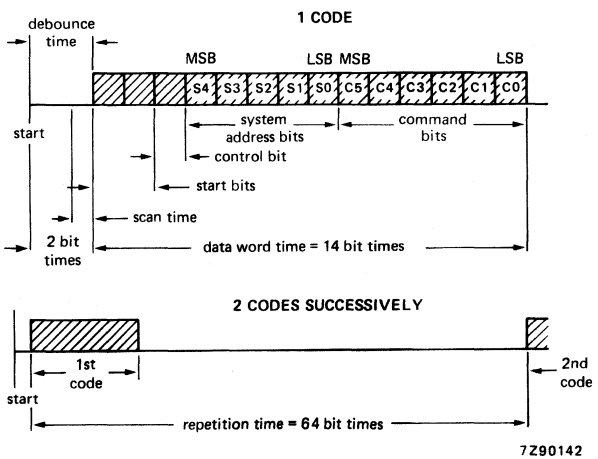


Fig. 4 DATA output format (RC-5).

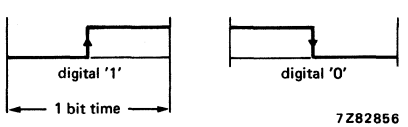


Fig. 5 Biphase transmission code; 1 bit time = $3 \times 2^8 \times T_{OSC}$ (typically 1,778 ms) where T_{OSC} is the oscillator period time.

Table 2 Command matrix X-DR

code no.	X-lines X.. 0	1	2	3	4	5	6	7	DR-lines DR.. 0	1	2	3	4	5	6	7	command bits C.. 5	4	3	2	1	0
0	●								●								0	0	0	0	0	0
1	●									●							0	0	0	0	0	1
2	●										●						0	0	0	0	1	0
3	●											●					0	0	0	0	1	1
4	●												●				0	0	0	1	0	0
5	●													●			0	0	0	1	0	1
6	●														●		0	0	0	1	1	0
7	●															●	0	0	0	1	1	1
8		●							●								0	0	1	0	0	0
9		●								●							0	0	1	0	0	1
10		●									●						0	0	1	0	1	0
11		●										●					0	0	1	0	1	1
12		●											●				0	0	1	1	0	0
13		●												●			0	0	1	1	0	1
14		●													●		0	0	1	1	1	0
15		●														●	0	0	1	1	1	1
16			●						●								0	1	0	0	0	0
17			●							●							0	1	0	0	0	1
18			●								●						0	1	0	0	1	0
19			●									●					0	1	0	0	1	1
20			●										●				0	1	0	1	0	0
21			●											●			0	1	0	1	0	1
22			●												●		0	1	0	1	1	0
23			●													●	0	1	0	1	1	1
24				●					●								0	1	1	0	0	0
25				●						●							0	1	1	0	0	1
26				●							●						0	1	1	0	1	0
27				●								●					0	1	1	0	1	1
28				●									●				0	1	1	1	0	0
29				●										●			0	1	1	1	0	1
30				●											●		0	1	1	1	1	0
31				●												●	0	1	1	1	1	1

code no.	X-lines X.. 0	1	2	3	4	5	6	7	DR-lines DR.. 0	1	2	3	4	5	6	7	command bits C.. 5	4	3	2	1	0
32					●				●								1	0	0	0	0	0
33					●					●							1	0	0	0	0	1
34					●						●						1	0	0	0	1	0
35					●							●					1	0	0	0	1	1
36					●								●				1	0	0	1	0	0
37					●									●			1	0	0	1	0	1
38					●										●		1	0	0	1	1	0
39					●											●	1	0	0	1	1	1
40						●			●								1	0	1	0	0	0
41						●				●							1	0	1	0	0	1
42						●					●						1	0	1	0	1	0
43						●						●					1	0	1	0	1	1
44						●							●				1	0	1	1	0	0
45						●								●			1	0	1	1	0	1
46						●									●		1	0	1	1	1	0
47						●										●	1	0	1	1	1	1
48							●		●								1	1	0	0	0	0
49							●			●							1	1	0	0	0	1
50							●				●						1	1	0	0	1	0
51							●					●					1	1	0	0	1	1
52							●						●				1	1	0	1	0	0
53							●							●			1	1	0	1	0	1
54							●								●		1	1	0	1	1	0
55							●									●	1	1	0	1	1	1
56								●	●								1	1	1	0	0	0
57								●		●							1	1	1	0	0	1
58								●			●						1	1	1	0	1	0
59								●				●					1	1	1	0	1	1
60								●					●				1	1	1	1	0	0
61								●						●			1	1	1	1	0	1
62								●							●		1	1	1	1	1	0
63								●								●	1	1	1	1	1	1

Table 3 System matrix Z-DR

system no.	Z-lines Z..				DR-lines DR..								system bits S..				
	0	1	2	3	0	1	2	3	4	5	6	7	4	3	2	1	0
0	●				●								0	0	0	0	0
1	●					●							0	0	0	0	1
2	●						●						0	0	0	1	0
3	●							●					0	0	0	1	1
4	●								●				0	0	1	0	0
5	●									●			0	0	1	0	1
6	●										●		0	0	1	1	0
7	●											●	0	0	1	1	1
8		●			●								0	1	0	0	0
9		●				●							0	1	0	0	1
10		●					●						0	1	0	1	0
11		●						●					0	1	0	1	1
12		●							●				0	1	1	0	0
13		●								●			0	1	1	0	1
14		●									●		0	1	1	1	0
15		●										●	0	1	1	1	1
16			●		●								1	0	0	0	0
17			●			●							1	0	0	0	1
18			●				●						1	0	0	1	0
19			●					●					1	0	0	1	1
20			●						●				1	0	1	0	0
21			●							●			1	0	1	0	1
22			●								●		1	0	1	1	0
23			●									●	1	0	1	1	1
24				●	●								1	1	0	0	0
25				●		●							1	1	0	0	1
26				●			●						1	1	0	1	0
27				●				●					1	1	0	1	1
28				●					●				1	1	1	0	0
29				●						●			1	1	1	0	1
30				●							●		1	1	1	1	0
31				●								●	1	1	1	1	1

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5	to	8,5	V
Input voltage range	V_I	−0,5	to	$(V_{DD}+0,5)$	V*
Input current	$+I_I$	max.		10	mA
Output voltage range	V_O	−0,5	to	$(V_{DD}+0,5)$	V*
Output current	$+I_O$	max.		10	mA
Power dissipation output OSC	P_O	max.		50	mW
Power dissipation per output (all other outputs)	P_O	max.		100	mW
Total power dissipation per package	P_{tot}	max.		200	mW
Operating ambient temperature range	T_{amb}	−25	to	+85	°C
Storage temperature range	T_{stg}	−55	to	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

* V_{DD} + 0,5 V not to exceed 9 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	2	–	7	V
Supply current at I_O = 0 mA for all outputs; X0 to X7 and Z3 at V_{DD}; all other inputs at V_{DD} or V_{SS}; excluding leakage current from open drain N-channel outputs; T_{amb} = 25 °C	7	I_{DD}	–	–	10	μA
Inputs						
Keyboard inputs X and Z with P-channel pull-up transistors						
Input current (each input) at V_I = 0 V; TP = SSM = LOW	2 to 7	$-I_I$	10	–	600	μA
Input voltage HIGH	2 to 7	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	2 to 7	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at T_{amb} = 25 °C; TP = HIGH; V_I = 7 V		I_{IR}	–	–	1	μA
V_I = 0 V		$-I_{IR}$	–	–	1	μA
SSM, TP1 and TP2						
Input voltage HIGH	2 to 7	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	2 to 7	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at T_{amb} = 25 °C; V_I = 7 V		I_{IR}	–	–	1	μA
V_I = 0 V		$-I_{IR}$	–	–	1	μA
OSC						
Input leakage current at T_{amb} = 25 °C; V_I = 0 V; TP1 = HIGH; Z2 = Z3 = LOW	2 to 7	$-I_I$	–	–	2	μA

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Outputs						
DATA and MDATA						
Output voltage HIGH at $-I_{OH}$ = 0,4 mA	2 to 7	V_{OH}	V_{DD} −0,3	–	–	V
Output voltage LOW at I_{OL} = 0,6 mA	2 to 7	V_{OL}	–	–	0,3	V
Output leakage current at:						
V_O = 7 V		I_{OR}	–	–	10	μA
V_O = 0 V		$-I_{OR}$	–	–	20	μA
T_{amb} = 25 °C;						
V_O = 7 V		I_{OR}	–	–	1	μA
V_O = 0 V		$-I_{OR}$	–	–	2	μA
DR0 to DR7, TP2						
Output voltage LOW at I_{OL} = 0,3 mA	2 to 7	V_{OL}	–	–	0,3	V
Output leakage current at V_O = 7 V	7	I_{OR}	–	–	10	μA
at V_O = 7 V						
T_{amb} = 25 °C		I_{OR}	–	–	1	μA
OSC						
Oscillator current at OSC = V_{DD}	7	I_{OSC}	4,5	–	30	μA
Oscillator						
Maximum oscillator frequency at C_L = 40 pF (Figs 6 and 7)	2	f_{OSC}	–	–	450	kHz
Free-running oscillator frequency at T_{amb} = 25 °C	2	f_{OSC}	10	–	120	kHz

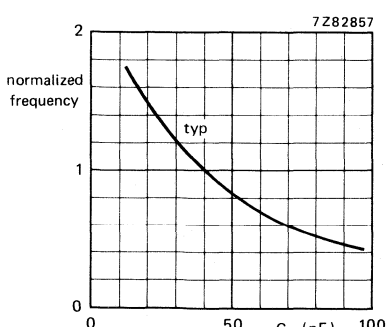


Fig. 6 Typical normalized input frequency as a function of the load (keyboard) capacitance.

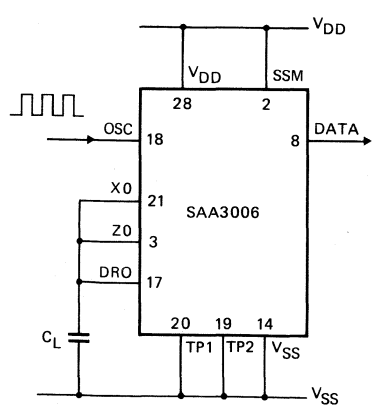


Fig. 7 Test circuit for measurement of maximum oscillator frequency.

INFRARED REMOTE CONTROL TRANSCODER (RC-5)

GENERAL DESCRIPTION

The SAA3028 is intended for use in general purpose (RC-5) remote control systems. The main function of this integrated circuit is to convert RC-5 biphase coded signals into equivalent binary values. Two input circuits are available: one for RC-5 coded signals only; the other is selectable to accept (1) RC-5 coded signals only, or (2) RC-5 (extended) coded signals only. The input used is that at which an active code is first detected. Coded signals not in RC-5/RC-5(ext) format are rejected. Data input and output is by serial transfer, the output interface being compatible for I^2C bus operation.

Features

- Converts RC-5 or RC-5(ext) biphase coded signals into binary equivalents
- Two data inputs, one fixed (RC-5), one selectable (RC-5/RC-5(ext))
- Rejects all codes not in RC-5/RC-5(ext) format
- I^2C output interface capability
- Power-off facility
- Master/slave addressable for multi-transmitter/receiver applications in RC-5(ext) mode
- Power-on-reset for defined start-up

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	4,5 to	5,5 V
Supply current (quiescent) at V_{DD} = 5,5 V; T_{amb} = 25 °C	I_{DD}	max.	200 μA
Operating ambient temperature range	T_{amb}	−25 to	+85 °C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

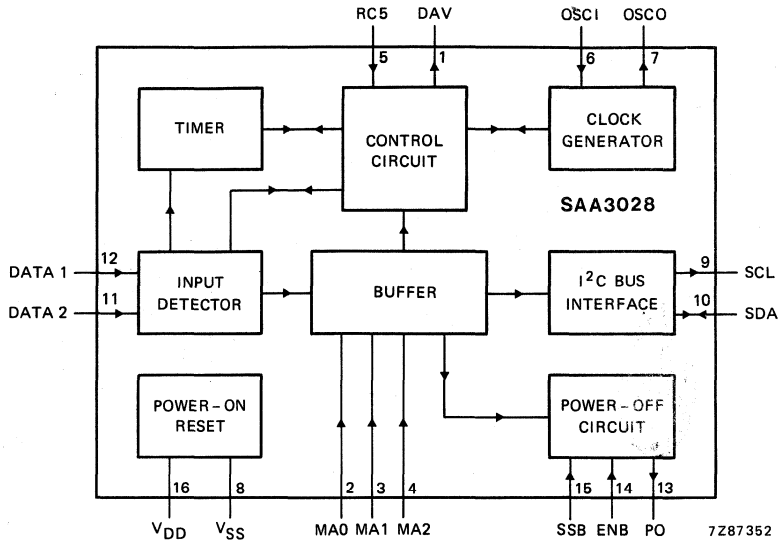


Fig. 1 Block diagram.

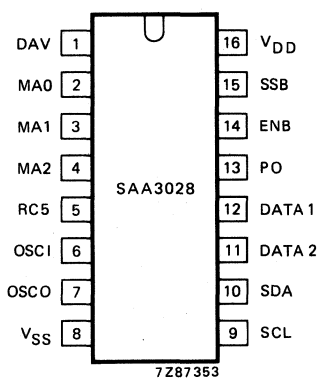


Fig. 2 Pinning diagram.

PINNING

1	DAV	data valid output with open drain N-channel transistor
2	MA0	master address inputs
3	MA1	master address inputs
4	MA2	master address inputs
5	RC5	data 2 input select
6	OSCI	oscillator input
7	OSCO	oscillator output
8	V_{SS}	negative supply (ground)
9	SCL	serial clock line (I^2C bus)
10	SDA	serial data line (I^2C bus)
11	DATA 2	data 2 input
12	DATA 1	data 1 input
13	PO	power-off signal output with open drain N-channel transistor
14	ENB	enable input
15	SSB	set standby input
16	V_{DD}	positive supply (+5 V)

FUNCTIONAL DESCRIPTION

Input function

The two data inputs are accepted into the buffer as follows:

- DATA 1. Only biphase coded signals which conform to the RC-5 format are accepted at this input.
- DATA 2. This input performs according to the logic state of the select input RC5. When RC5 = HIGH, DATA 2 input will accept only RC-5 coded signals. When RC5 = LOW, DATA 2 input will accept only RC-5(ext) coded signals.

The input detector selects the input, DATA 1 or DATA 2, in which a HIGH to LOW transition is first detected. The selected input is then accepted by the buffer for code conversion. All signals received that are not in the RC-5 or RC-5(ext) format are rejected.

Formats of RC-5 and RC-5(ext) biphase coded signals are shown in Figs 3 and 4 respectively; the codes commence from the left of the formats shown. The bit-times of the biphase codes are defined in Fig. 5.

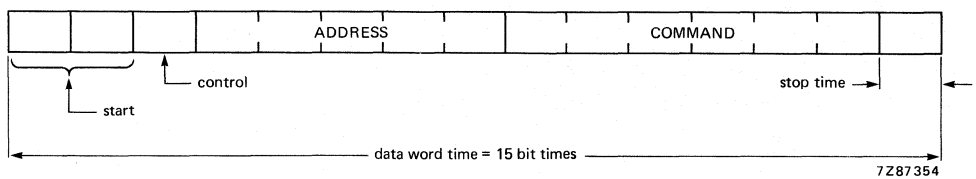


Fig. 3 RC-5 code format: the first start bit is used only for detection and input gain-setting; stop time = 1,5 bit-times (nominal).

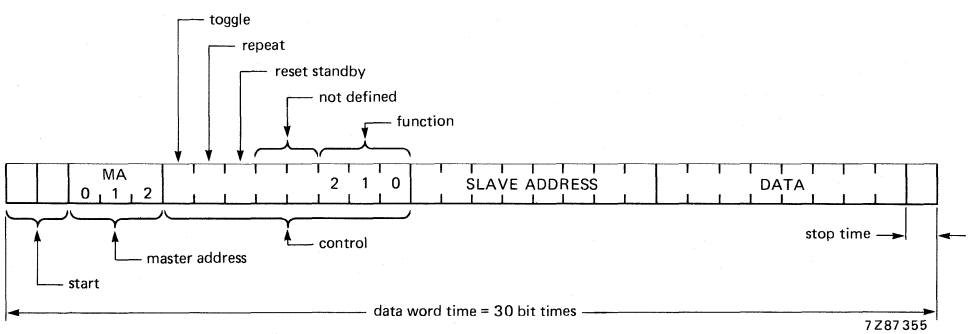


Fig. 4 RC-5(extended) code format: the first start bit is used only for detection and input gain-setting; stop time = 1,5 bit-times (nominal).

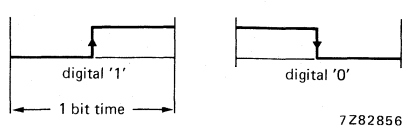


Fig. 5 Biphase code definition: RC-5 bit-time = $2^7 \times T_{OSC}$ = 1,778 ms (typical); RC-5(ext) bit-time = $2^6 \times T_{OSC}$ = 0,89 ms (typical), where T_{OSC} = the oscillator period time.

FUNCTIONAL DESCRIPTION (continued)

More information is added to the input data held in the buffer in order to make it suitable for transmission via the I^2C interface. The information now held in the buffer is as follows:

RC-5 buffer contents		RC-5(ext) buffer contents	
• data valid indicator	1 bit	• data valid indicator	1 bit
• format indicator	1 bit	• format indicator	1 bit
• input indicator	1 bit	• input indicator	1 bit
• control	1 bit	• master address	3 bits
• address data	5 bits	• control	8 bits
• command data	6 bits	• slave address	8 bits
		• data	8 bits

The information assembled in the buffer is subjected to the following controls before being made available at the I^2C interface:

ENB = HIGH — Enables the set standby input SSB.

SSB = LOW — Causes power-off output PO to go HIGH.

PO = HIGH — This occurs when the set standby input SSB = LOW and allows the existing values in the buffer to be overwritten by the new binary equivalent values. After ENB = LOW, SSB is don't care.

PO = LOW — This occurs according to the type of code being processed, as follows:

RC-5. When the binary equivalent value is transferred to the buffer.

RC-5(ext). When the reset standby bit is active and the master address bits are equal in value to the MA0, MA1, MA2 inputs.

At power-on, PO is reset to LOW.

DAV = HIGH — This occurs when the buffer contents are valid. If the buffer is not empty, or an output transfer is taking place, then the new binary values are discarded.

Output function

The data is assembled in the buffer in the format shown in Fig. 6 for RC-5 binary equivalent values, or in the format shown in Fig. 7 for RC-5(ext) binary equivalent values. The data is output serially, starting from the left of the formats shown in Figs 6 and 7.

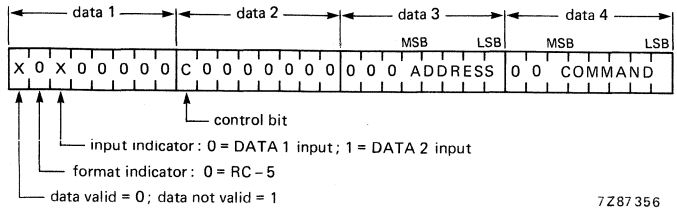


Fig. 6 RC-5 binary equivalent value format.

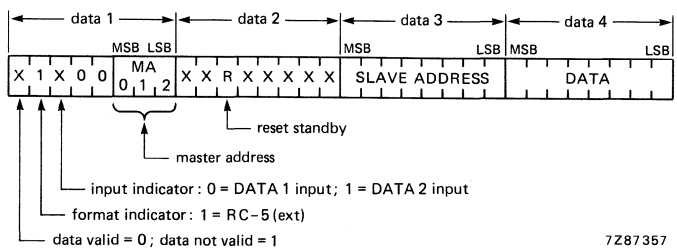


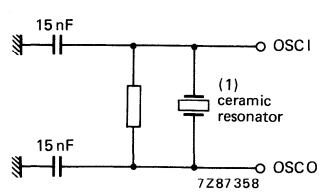
Fig. 7 RC-5(ext) binary equivalent value format.

The output signal DAV, derived in the buffer from the data valid bit, is provided to facilitate use of the transcoder on an interrupt basis. This output is reset to LOW during power-on.

The I^2C interface allows transmission on a bidirectional, two-wire I^2C bus. The interface is a slave transmitter with a built-in slave address, having a fixed 7-bit binary value of 0100110. Serial output of the slave address onto the I^2C bus starts from the left-hand bit.

Oscillator

The oscillator can comprise a ceramic resonator circuit as shown in Fig. 8. The typical frequency of oscillation is 455 kHz.



(1) Catalogue number of ceramic resonator: 2422 540 98008.

Fig. 8 Oscillator circuit.

FUNCTIONAL DESCRIPTION (continued)

I^2C bus transmission

Formats for I^2C transmission in low and high speed modes are shown respectively in Figs 9 and 10.

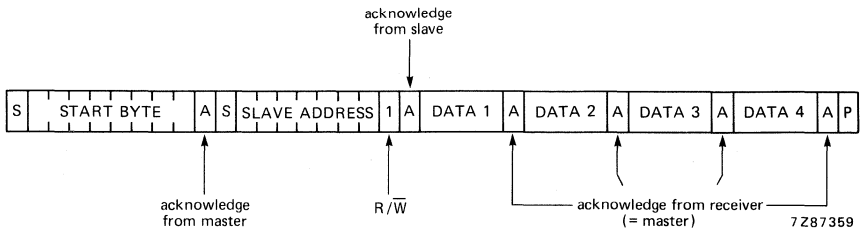


Fig. 9 Format for transmission in I^2C low speed mode.

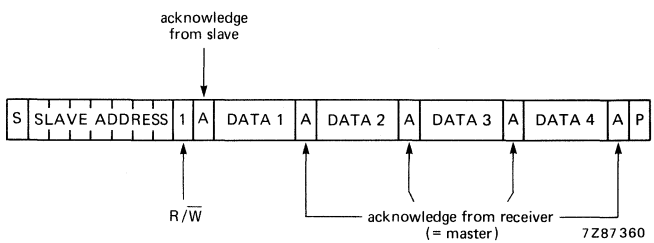


Fig. 10 Format for transmission in I^2C high speed mode.

Note to Figures 9 and 10

When R/$\overline{W}$ bit = 0; the slave generates a NACK (negative acknowledge), leaves the data line HIGH and waits for a stop (P) condition.

When the receiver generates a NACK; the slave leaves the data line HIGH and waits for P (the slave acting as if all data has been transmitted).

When all data has been transmitted, the data line remains HIGH and the slave waits for P.

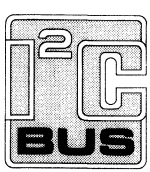
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5 to	+15	V
Input voltage range	V_I	−0,5 to	(V_{DD} + 0,5)	V*
Input current	$\pm I_I$	max.	10	mA
Output voltage range	V_O	−0,5 to	(V_{DD} + 0,5)	V*
Output current	$\pm I_O$	max.	10	mA
Power dissipation output OSCO	P_O	max.	50	mW
Power dissipation per output (all other outputs)	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}	−25 to	+85	°C
Storage temperature range	T_{stg}	−55 to	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").



Purchase of Philips I²C components conveys a licence under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	4,5	–	5,5	V
Supply current; quiescent at T_{amb} = 25 °C	5,5	I_{DD}	–	–	200	μA
Inputs						
MA0, MA1, MA2, DATA 1, DATA 2, RC5, SCL, ENB, SSB, OSCI						
Input voltage HIGH	4,5 to 5,5	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	4,5 to 5,5	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 5,5 V; T_{amb} = 25 °C	5,5	I_I	–	–	1	μA
Input leakage current at V_I = 0 V; T_{amb} = 25 °C;	5,5	$-I_I$	–	–	1	μA
Outputs						
DAV, PO						
Output voltage LOW at I_{OL} = 1,6 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 5,5 V; T_{amb} = 25 °C	5,5	I_{OR}	–	–	1	μA
OSCO						
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	4,5 to 5,5	V_{OH}	V_{DD} − 0,5	–	–	V
Output voltage LOW at I_{OL} = 0,3 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at T_{amb} = 25 °C; V_O = 5,5 V	5,5	I_{OR}	–	–	1	μA
V_O = 0 V	5,5	I_{OR}	–	–	1	μA
SDO						
Output voltage LOW at I_{OL} = 2 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 5,5 V; T_{amb} = 25 °C	5,5	I_{OR}	–	–	1	μA
Oscillator						
Max. oscillator frequency (Fig. 8)	4,75	f_{OSCI}	500	–	–	kHz

TELETEXT TIMING CHAIN

The SAA5020 is an MOS N-channel integrated circuit which performs the timing functions for a teletext system.
The SAA5020 is a 24-lead device which provides the necessary timing signals to the teletext page memory and to the Character Generator (SAA5050 series). It works in conjunction with the Video Processor Circuit (SAA5030) and the Teletext Acquisition and Control Circuit (SAA5040 series). The operation of the SAA5020 maintains the synchronisation between the teletext system and the incoming video signal.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5 V
Supply current	I_{DD}	typ.	20 mA
Operating ambient temperature range	T_{amb}	−20 to +70	°C

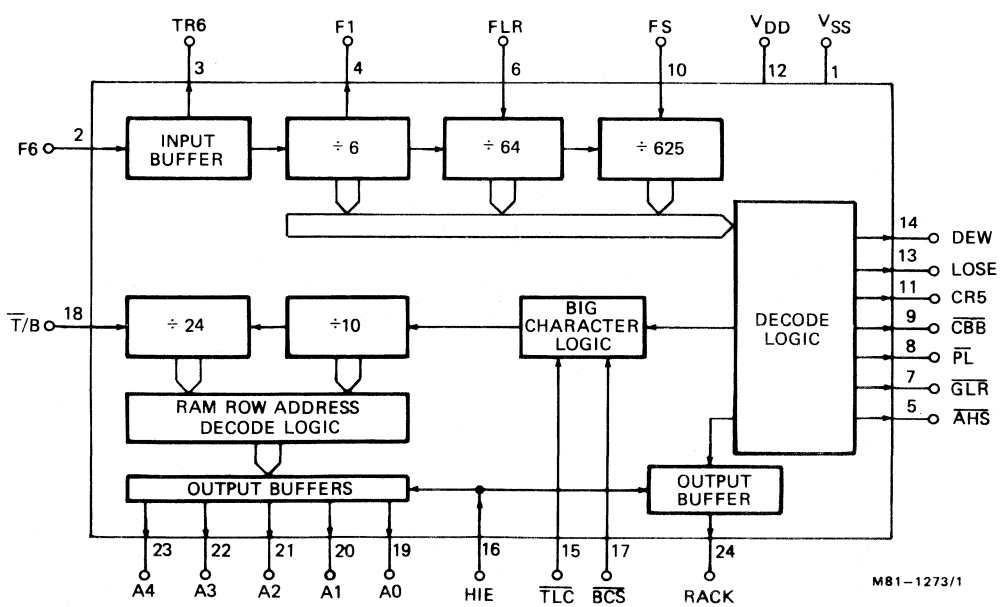


Fig.1 Block diagram

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A)

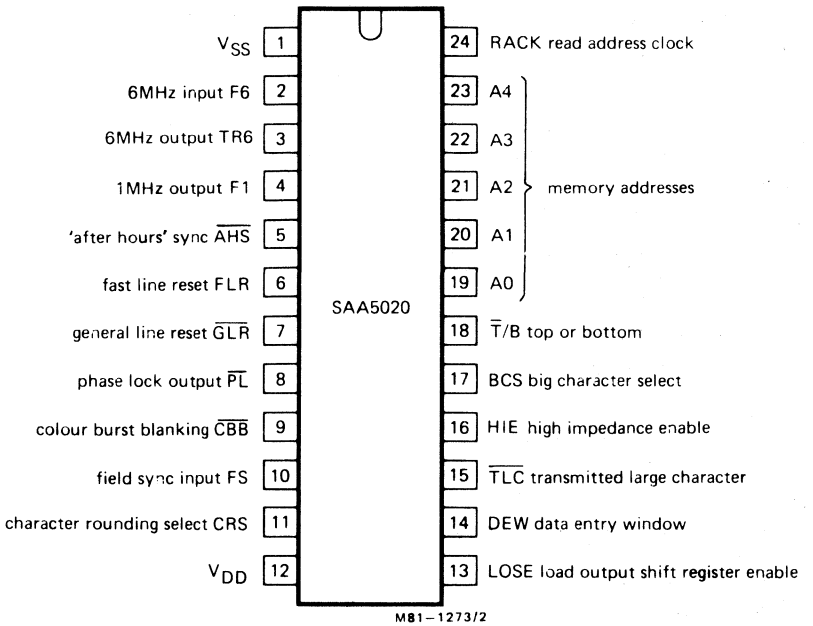


Fig.2 Pinning diagram

DESCRIPTION

The basic input to the SAA5020 is a 6 MHz clock signal from the Video Processor Circuit (SAA5030). This clock signal is buffered and is available as an output. A divide-by-six counter produces the character rate of 1 MHz. This is followed by a divide-by-64 to produce the line rate and a further divide by 312/313 to derive the field rate.

The line rate is also divided by 10 to clock a divide-by-24 counter for the teletext memory row addresses. Logic is incorporated to enable the selection of big character display, and to enable the display of transmitted large characters. An output is provided to enable character rounding for normal height characters. A composite sync. signal ($\overline{AHS}$) is available as an output which can be used to synchronise the display time bases.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. (See Handling MOS Devices).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Voltages (with respect to pin 1)

			min.	max.	
Supply voltage	(pin 12)	V_{DD}	−0.3	7.5	V
Input voltage	All inputs (pins 2, 6, 10, 15, 16, 17, 18)	V_I	−0.3	7.5	V

RATINGS (continued)

		min.	typ.	max.	
Output voltage (pins 3, 4, 5, 7, 11, 13, 14)	V_O	−0.3		7.5	V
(pins 16, 19, 20, 21, 23, 24)	V_O	−0.3		7.5	V
(pins 8, 9)	V_O	−0.3		13.2	V
Temperatures					
Storage temperature range	T_{stg}		−20 to +125		°C
Operating ambient temperature range	T_{amb}		−20 to +70		°C

CHARACTERISTICS

Supply voltage (pin 12)	V_{DD}	4.5	–	5.5	V
The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.					
Supply current	I_{DD}	–	20	50	mA
Inputs					
6 MHz - F6 (pin 2)					
Input voltage; HIGH	V_{IH}	3.5	–	6.5	V
Input voltage; LOW	V_{IL}	Note 1	–	0	V
Rise time (between 0 V and 3.5 V levels)	t_r	–	–	25	ns
Fall time (between 0 V and 3.5 V levels)	t_f	–	–	20	ns
Mark/space ratio (measured at 1.5 V level)		40:60	–	56:44	
Input leakage current (V_I = 5.5 V)	I_{IR}	0.2	–	2	μA
All other inputs FLR (pin 6), FS (pin 10), $\overline{\text{TLC}}$ (pin 15), HIE (pin 16), BCS (pin 17), $\overline{\text{T}}$/B (pin 18)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Input leakage current (V_I = 5.5 V)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Outputs					
TR6 (pin 3)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.75	–	V_{DD}	V
Output load capacitance	C_L	–	–	15	pF
Output rise time (Note 2)	t_r	–	–	30	ns
Output fall time (Note 2)	t_f	–	–	30	ns
Mark/space ratio		40:60	–	–	

		min.	typ.	max.	
F1 (pin 4)					
Output voltage; LOW (I_{OL} = 100 μA) Note 4	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.75	–	V_{DD}	V
Output load capacitance	C_L	–	–	35	pF
Output rise time } Note 2	t_r	–	–	50	ns
Output fall time } Note 2	t_f	–	–	30	ns
Mark/space ratio		–	–	60:40	
Delay time (measured from rising edge of TR6) Note 3	t_d	7	–	60	ns
$\overline{\text{AHS}}$ (pin 5)					
Output voltage; LOW (I_{OL} = 100 μA) Note 5	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	30	pF
Output rise time } Note 2	t_r	–	–	100	ns
Output fall time } Note 2	t_f	–	–	100	ns
Delay time (falling edge measured from F1 rising edge) Note 3		0	–	300	ns
$\overline{\text{GLR}}$ (pin 7)					
Output voltage; LOW (I_{OL} = 0.9 mA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	40	pF
Output rise time } Note 2	t_r	–	–	60	ns
Output fall time } Note 2	t_f	–	–	50	ns
Delay time Note 3	t_d	0	–	200	ns
$\overline{\text{PL}}$ (pin 8) (Open drain)					
Output voltage; LOW (I_{OL} = 2 mA)	V_{OL}	–	–	1.0	V
Output current in off state (V_O = 6 V)	I_O	–	–	10	μA
Output load capacitance	C_L	–	–	30	pF
Output fall time Note 2	t_f	–	–	100	ns
Delay time Note 3	t_d	0	–	250	ns
$\overline{\text{CBB}}$ (pin 9) (Open drain)					
Output voltage; LOW (I_{OL} = 1 mA)	V_{OL}	0	–	1.0	V
Output current in off state (V_O = 6 V)	I_O	–	–	10	μA
Output load capacitance	C_L	–	–	30	pF
Output fall time Note 2	t_f	–	–	200	ns
Delay time Note 3	t_d	0	–	250	ns
CRS (pin 11)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	30	pF
Output rise time } Note 2	t_r	–	–	1	μs
Output fall time } Note 2	t_f	–	–	1	μs

		min.	typ.	max.	
LOSE (pin 13)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	30	pF
Output rise time (Note 2)	t_r	–	–	50	ns
Output fall time (Note 2)	t_f	–	–	50	ns
Delay time (measured from F1 falling edge) Note 3	t_d	0	–	250	ns
DEW (pin 14)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	VDD	V
Output load capacitance	C_L	–	–	42	pF
Output rise time (Note 2)	t_r	–	–	200	ns
Output fall time (Note 2)	t_f	–	–	200	ns
Delay time (measured from falling edge of $\overline{CBB}$) Note 3	t_d	7.5		8.5	μs
A0,A1,A2 (pins 19, 20 and 21) 3-state					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	85	pF
Output rise time (Note 2)	t_r	–	–	1	μs
Output fall time (Note 2)	t_f	–	–	1	μs
Delay time (measured from falling edge of $\overline{CBB}$) Note 3	t_d	–	–	10	μs
Leakage current in 'off' state (V_O = 5.5 V)	I_{IR}	–	–	10	μA
High impedance switching time					
Into high impedance state		0	–	0.9	μs
From high impedance state		1	–	2.9	μs
A3,A4 (pin 22 and 23) 3-state					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.4	V
All other parameters are as for A_0 to A_2					
RACK (pin 24) 3-state					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	40	pF
Output rise time (Note 2)	t_r	–	–	60	ns
Output fall time (Note 2)	t_f	–	–	300	ns
Delay time (measured from dalling edge of F1) Note 3	t_d	150	–	280	ns
Leakage current in 'off' state (V_O = 5.5 V)	I_{IR}	–	–	10	μA
High impedance switching time					
Into high impedance state		1	–	2.9	μs
From high impedance state		0	–	0.9	μs

CHARACTERISTICS (continued)

Notes

1. This input incorporates an internal clamping diode, nominal $V_{IL(min)} = -0.5$ V.

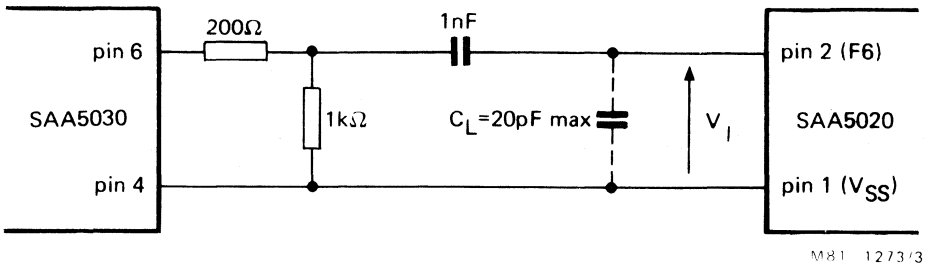


Fig.3 Capacitive coupling network for F6

2. Rise and fall times are measured between the 0.8 V and 2.0 V levels unless otherwise stated.
3. All delay times are measured from the rising edge of F1 unless otherwise stated.
   All delay times are measured at the 1.5 V level on the input to either the 2.0 V level on the rising edge of the output of the 0.8 V level on the falling edge of the output.
4. I_{OL} may be increased to 1 mA if load capacitance is less than 10 pF.
5. I_{OL} may be increased to 1.6 mA. Delay time will be increased to 350 ns max.

APPLICATION DATA

The function is quoted against the corresponding pin number.

For details of output waveforms see Fig.5

Pin No.

1. **V_{SS} Ground – 0 V**
2. **F6**

   This input is the 6 MHz master clock signal and is used to derive the basic timings for the teletext display. It contains an internal diode clamp.
3. **TR6**

   This output is the 6 MHz character dot rate clock signal for the SAA5050 Teletext Character Generator.
4. **F1**

   This output is a 1 MHz character repetition rate clock signal for the SAA5040 Teletext Acquisition and Control device and the SAA5050 Teletext Character Generator.
   This output is synchronous with TR6, with a positive-going edge occuring at time zero of the line.
5. **$\overline{\text{AHS}}$ After hours sync**

   This output signal is an internally generated TV compound sync signal which may be used to synchronise the display (Fig.4).
6. **FLR Fast line reset**

   This input from the SAA5030 Video Processor is used to reset the internal TV line rate counter. It is a positive-going pulse of approximately 4.6 μs duration, and occurs during initial set-up of the phase-locked system.

7. **$\overline{\text{GLR}}$ General line reset**

   This output is a TV line frequency signal used for reset and clock functions in the SAA5040 Teletext Acquisition and Control device, and the SAA5050 Teletext Character Generator. It is a 1 μs negative-going pulse commencing 5 μs from the start of each line.

8. **$\overline{\text{PL}}$ Phase lock**

   This line frequency output signal to the SAA5030 Video Processor is used to phase lock the 6 MHz display system clock to the incoming television video signal. It is a 4 μs negative-going pulse commencing at 62 μs into line.

9. **$\overline{\text{CBB}}$ Colour burst blanking**

   This output signal is used to reset internal data processing and sync circuits within the SAA5030 Video Processor. It is an 8 μs negative-going pulse starting at time zero of the line.

10. **FS Field sync**

    This input signal from the SAA5030 Video Processor is used to reset the field rate counter, to maintain correct field sync with incoming video.

11. **CRS Character rounding select**

    This output signal to the SAA5050 Teletext Character Generator is required for correct character rounding of small characters within the character generator. The output is HIGH for even fields (0-313 lines) and LOW for odd fields (314-625 lines).

12. **V_{DD} + 5 V Supply**

    This is the power supply input to the circuit.

13. **LOSE Load output shift register enable**

    This output signal to the SAA5050 Teletext Character Generator is used to reset internal control character flip-flops prior to the start of each display line. This signal also defines the character display period. It is a positive-going pulse of duration 40 μs after the start of the line and occurs on lines 49 to 288 and 362 to 601 only.

14. **DEW Data entry window**

    This output defines the period during which data may be extracted from the incoming television signal and written into the page memory. This signal is required by the SAA5040 Teletext Acquisition and Control device and the SAA5050 Teletext Character Generator. This is a positive-going pulse commencing at the end of line 5 and finishing at end of line 22 and similarly for lines 318 and 335.

15. **$\overline{\text{TLC}}$ Transmitted large character**

    This input from the SAA5050 Teletext Character Generator is to enable the correct display of large characters under broadcast control. It is HIGH for normal character display and must be taken LOW for large character display.

16. **HIE High impedance enable**

    This input when taken HIGH will switch the address and address clock (RACK) outputs to their high impedance state. For normal teletext operation this input should be connected to the DEW output (pin 14).

APPLICATION DATA (continued)

17. **$\overline{\text{BCS}}$ Big character select**

This input from the SAA5040 Teletext Acquisition and Control circuit is used to enable the correct display of large characters. It must be HIGH for normal character display and taken LOW for large character display.

18. **$\overline{\text{T}}$/B Top or bottom select**

This input from the SAA5040 Teletext Acquisition and Control device controls the RAM row address logic for correct operation of page display when large character display has been selected under user control. It must be LOW for the top half to be displayed, and HIGH for the bottom half.

19, 20
21, 22
23 **A0 to A4 Memory addresses**

These 3-state outputs to the teletext memory provide the RAM row addresses during the display period (i.e. TV lines 49 to 288 - 362 to 601 inclusive). These outputs switch to the high impedance state when HIE (pin 16) is taken HIGH. All address outputs are LOW during line 40.
During display period the outputs provide a binary count sequence which is increased every ten lines in small character mode and every twenty lines in large character mode. If any row contains transmitted large characters the address is incremented by two after 20 lines.

24. **RACK Read address clock**

This 3-state output is a 1 MHz clock occuring during the display period of the line only. This output is used to clock the external RAM address counter during the display period. The output will switch to the high impedance state when HIE (pin 16) is taken HIGH. The clock starts with a positive edge 14.65 μs from the start of a line and finishes with a negative-going edge at 53.15 μs.

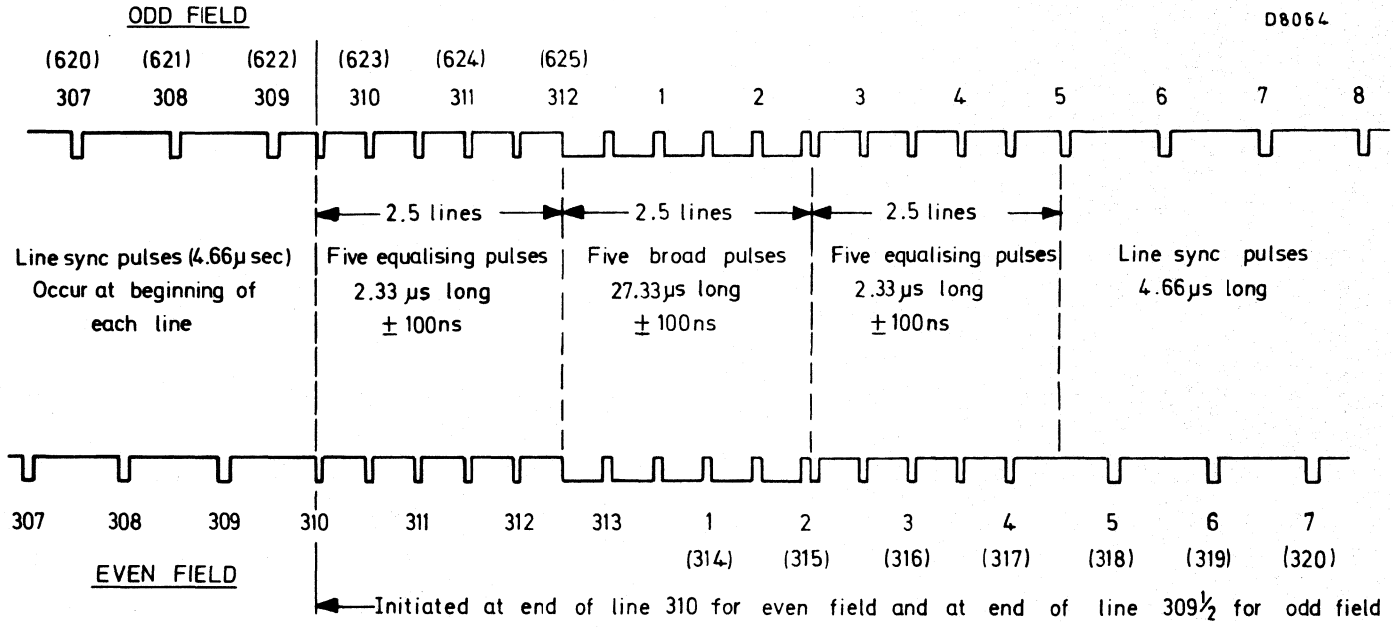


Fig.4 After hours sync waveforms ($\overline{AHS}$)

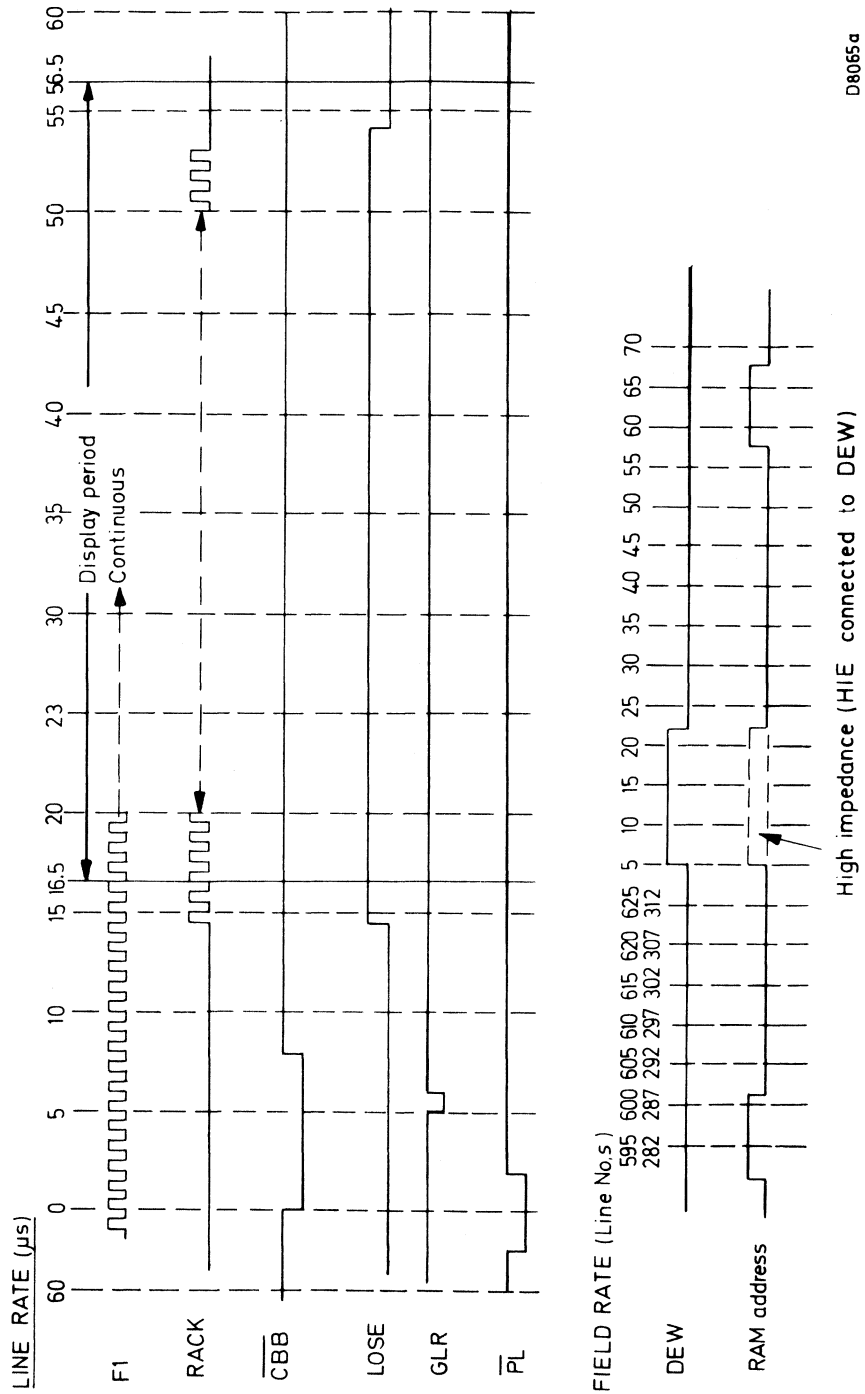


Fig.5 SAA5020 Output waveforms

TELETEXT TIMING CHAIN FOR USA 525 LINE SYSTEM

GENERAL DESCRIPTION

The SAA5025D is a MOS N-channel integrated circuit which performs the timing functions for a Teletext system. It provides the necessary timing signals to extract data from a memory and produce a display according to the USA 525 line television standard (system M).
The SAA5025D may be used in conjunction with the SAA5030 (Teletext video processor; VIP) the SAA5050 (Teletext character generator; TROM), the SAA5040B (Teletext acquisition control; TAC) and the SAA5045 (Gearing and Address Logic Array; GALA).

Features

- Designed to operate with USA 525 line television standard (system M)
- For 24 row (8 TV lines per row) x 40 character display
- Big character select input for double height characters
- Composite sync signal output for display time-base synchronization

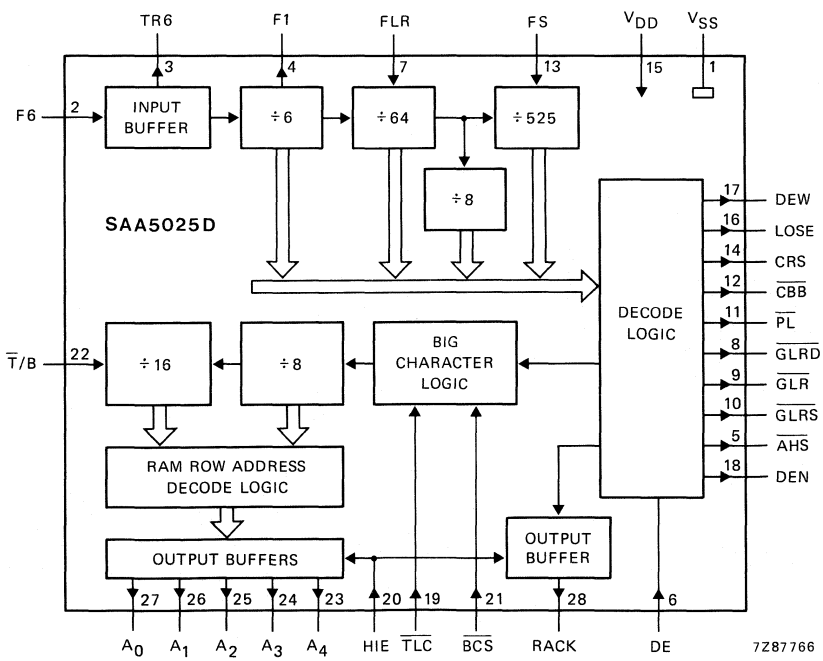


Fig. 1 Block diagram.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117D).

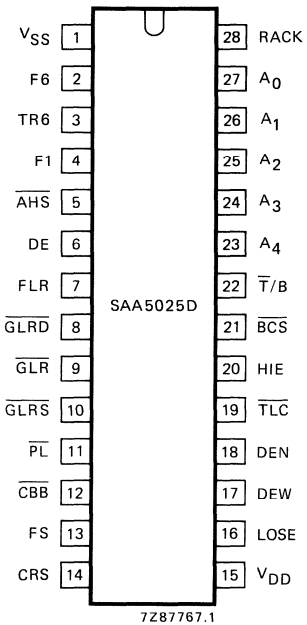


Fig. 2 Pinning diagram.

PINNING

1	V_{SS}	ground
2	F6	6,0419 MHz clock input
3	TR6	6,0419 MHz clock output
4	F1	1,007 MHz clock output
5	$\overline{AHS}$	after hours sync output
6	DE	display enable input
7	FLR	fast line reset input
8	$\overline{GLRD}$	general line reset delay output
9	$\overline{GLR}$	general line reset output
10	$\overline{GLRS}$	general line reset starting output
11	$\overline{PL}$	phase lock open drain output
12	$\overline{CBB}$	colour burst blanking output
13	FS	field (picture) sync input
14	CRS	character rounding select output
15	V_{DD}	positive supply (+ 5 V)
16	LOSE	load output shift register enable output
17	DEW	data entry window output
18	DEN	display enable output (negative-going)
19	$\overline{TLC}$	transmitted large characters input
20	HIE	high impedance enable input
21	$\overline{BCS}$	big character select input
22	$\overline{T}/B$	top/bottom select input
23	A_4	memory row address outputs (3-state)
24	A_3	
25	A_2	
26	A_1	
27	A_0	
28	RACK	read address clock output

FUNCTIONAL DESCRIPTION

The basic input to the SAB5025D is a 6,0419 MHz clock signal (e.g. from SAA5030). The clock input (F6) is buffered and also available as an output at TR6 to provide a dot rate clock. The signal at F6 is divided by 6 to produce the 1,007 MHz character rate clock at output F1, which is in turn divided by 64 to produce the line period of 63,556 μs. A divide-by-262 or 263 counter, clocked at line rate, produces a field (picture) period of 16,683 ms (average) i.e. 33,366 ms for divide-by-525. The display format is 40 characters per row for 24 rows (1 row is 8 TV lines).

A big character select ($\overline{BSC}$) input is provided and it enables double-height characters (16 TV lines per row) to be displayed. The top or bottom select ($\overline{T}/B$) input must be used in conjunction with $\overline{BCS}$ to select either the top half or bottom half of the page to be displayed on the television screen.

A composite sync ($\overline{AHS}$) output is available for synchronizing the display timebase. A high-impedance enable (HIE) input is included to switch the read address clock (RACK) and the memory row address (A_0 to A_4) outputs into their high-impedance states.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,3	+ 7,5	V
Input voltage range (note 1)	V_I	−0,3	+ 7,5	V
High-impedance state output voltage	V_{OHZ}	−0,3	+ 7,5	V
Open drain output voltage	V_{ODD}	−0,3	+ 13,2	V
Electrostatic charge protection on all inputs and outputs (notes 2 and 3)		1000	–	V
Total power dissipation per package	P_{tot}	–	275	mW
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Storage temperature range	T_{stg}	−20	+ 125	°C

Notes to ratings

1. See also characteristics on F6 input and Fig. 10.
2. Equivalent to discharging a 250 pF capacitor through a 1 kΩ series resistor.
3. N.B.: the SAA5025D is not protected against TV tube flash-over.
4. All outputs are TTL compatible.

DEVELOPMENT DATA

CHARACTERISTICS

T_{amb} = 25 °C; F6 input frequency = 6,041957 MHz; unless otherwise specified

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	4,5	5,0	5,5	V
Supply current	5	I_{DD}	5	–	50	mA
Inputs						
Input leakage currents						
F6	5,5	I_I	0,2	–	10	μA
	0	$-I_I$	–	–	10	μA
FLR, $\overline{TLC}$, FS, HIE, $\overline{BCS}$, $\overline{T}$/B, DE	0 to 5,5	$\pm I_I$	–	–	10	μA
Input capacitance; all inputs	5	C_I	–	–	7	pF
HIGH level input voltages						
F6; see Fig. 10	5	V_{IH}	2,7	–	6,5	V
FLR, $\overline{TLC}$, FS, HIE, $\overline{BCS}$, $\overline{T}$/B, DE	5	V_{IH}	2,0*	–	5,5	V
LOW level input voltage all inputs; see Fig. 10	5	V_{IL}	–	–	0,8*	V
Input rise and fall time F6; see Fig. 6	0 and 2,7	t_r; t_f	–	–	30	ns
Input F6 duty factor (see Fig. 10)	5	δ	40	50	56	%

* These values give no noise immunity.

DEVELOPMENT DATA

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Outputs						
Output node capacitance all outputs	5	C_O	–	–	7	pF
Output leakage current high-impedance state; A_0 to A_4, RACK	0 to 5,5	$\pm I_O$	–	–	10	μA
Output leakage current open drain; $\overline{PL}$, $\overline{CBB}$	6	I_O	–	–	10	μA
Output TR6 6,041957 MHz clock						
HIGH level output voltage $-I_{OH} = 100\ \mu A$	5	V_{OH}	2,75	–	V_{DD}	V
LOW level output voltage $I_{OL} = 100\ \mu A$	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	15	pF
Output rise and fall times see Fig. 7	5	t_r; t_f	–	–	30	ns
Duty factor at 1,5 V level depends on input F6 see F6 data and Fig. 10	5	δ	40	–	60	%
Output F1 1,007 MHz clock						
HIGH level output voltage $-I_{OH} = 100\ \mu A$	5	V_{OH}	2,75	–	V_{DD}	V
LOW level output voltage $I_{OL} = 400\ \mu A$	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	40	pF
Output rise and fall times see Fig. 7	5	t_r; t_r	–	–	50	ns
Propagation delays from rising edge of TR6; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	7	–	60	ns
Duty factor at 1,5 V level	5	δ	45	50	52	%

CHARACTERISTICS (continued)

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Output $\overline{AHS}$ see Fig. 6						
HIGH level output voltage $-I_{OH} = 200\ \mu A$	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage $I_{OL} = 1{,}6$ mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	30	pF
Output rise and fall times see Fig. 7	5	t_r; t_f	–	–	100	ns
Propagation delay from rising edge of F1; see Fig. 8; LOW-to-HIGH	5	t_{PLH}	0	–	350	ns
Outputs $\overline{GLR}$, $\overline{GLRD}$, $\overline{GLRS}$ see Fig. 3						
HIGH level output voltage $-I_{OH} = 100\ \mu A$	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage $I_{OL} = 0{,}8$ mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	40	pF
Output rise and fall times see Fig. 7	5	t_r t_f	– –	– –	70 50	ns ns
Propagation delay from rising edge of F1; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	0	–	300	ns
Output $\overline{PL}$ see Fig. 3						
LOW level output voltage $I_{OL} = 2$ mA	5	V_{OL}	0	–	1,0	V
Output load capacitance	5	C_L	–	–	30	pF
Output fall time; see Fig. 7	5	t_f	–	–	100	ns
Propagation delay from rising edge of F1; see Fig. 8; LOW-to-HIGH	5	t_{PLH}	0	–	250	ns

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Output $\overline{CBB}$ see Fig. 3						
LOW level output voltage I_{OL} = 2 mA	5	V_{OL}	0	–	1,0	V
Output load capacitance	5	C_L	–	–	30	pF
Output fall time; see Fig. 7	5	t_f	–	–	200	ns
Propagation delay from rising edge of F1; see Fig. 8; LOW-to-HIGH	5	t_{PLH}	0	–	250	ns
Output CRS						
HIGH level output voltage $-I_{OH}$ = 100 μA	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage I_{OL} = 100 μA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	30	pF
Output rise and fall times see Fig. 7	5	t_r; t_f	–	–	1	μs
Output LOSE see Fig. 3						
HIGH level output voltage $-I_{OH}$ = 100 μA	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage I_{OL} = 100 μA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	30	pF
Output rise and fall times; see Fig. 7	5	t_r; t_f	–	–	50	ns
Propagation delay from rising edge of F1; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	0	–	1	μs

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Output DEN						
HIGH level output voltage $-I_{OH} = 200\ \mu A$	5	V_{OH}	2,4	–	–	V
LOW level output voltage $I_{OL} = 100\ \mu A$	5	V_{OL}	–	–	0,4	V
Output load capacitance	5	C_L	–	–	30	pF
Output rise and fall times	5	t_r; t_f	–	–	50	ns
Propagation delay from rising edge of F1; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	–	–	250	ns
Output DEW see Fig. 4						
HIGH level output voltage $-I_{OH} = 200\ \mu A$	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage $I_{OL} = 1,6$ mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	50	pF
Output rise and fall times	5	t_r; t_f	–	–	200	ns
Propagation delay from rising edge of $\overline{CBB}$; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	6,5	6,96	7,5	μs

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Outputs A_0 to A_4 see Fig. 4						
HIGH level output voltage $-I_{OH} = 100\ \mu A$	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage $I_{OL} = 1{,}6$ mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	85	pF
Output rise and fall times	5	t_r; t_f	–	–	1	μs
Propagation delay from falling edge of $\overline{CBB}$; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	6,5	–	9,0	μs
Propagation delay from rising edge of HIE to high-impedance state; see Fig. 9	5	t_{PHZ}; t_{PLZ}	0	–	0,9	μs
Propagation delay from falling edge of HIE to normal active state; see Fig. 9	5	t_{PZH}; t_{PZL}	1	–	2,9	μs
Output RACK see Figs 3 and 4						
HIGH level output voltage $-I_{OH} = 100\ \mu A$	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage $I_{OL} = 1{,}6$ mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	40	pF
Output rise and fall times see Fig. 7	5	t_r t_f	– –	– –	60 300	ns ns
Propagation delay from falling edge of F1; see Fig. 8; HIGH-to-LOW	5	t_{PHL}	150	–	280	ns
Propagation delay from rising edge of HIE to high-impedance state; see Fig. 9	5	t_{PHZ}; t_{PLZ}	1	–	2,9	μs
Propagation delay from falling edge of HIE to normal active state; see Fig. 9	5	t_{PZH}; t_{PZL}	0	–	0,9	μs

DEVELOPMENT DATA

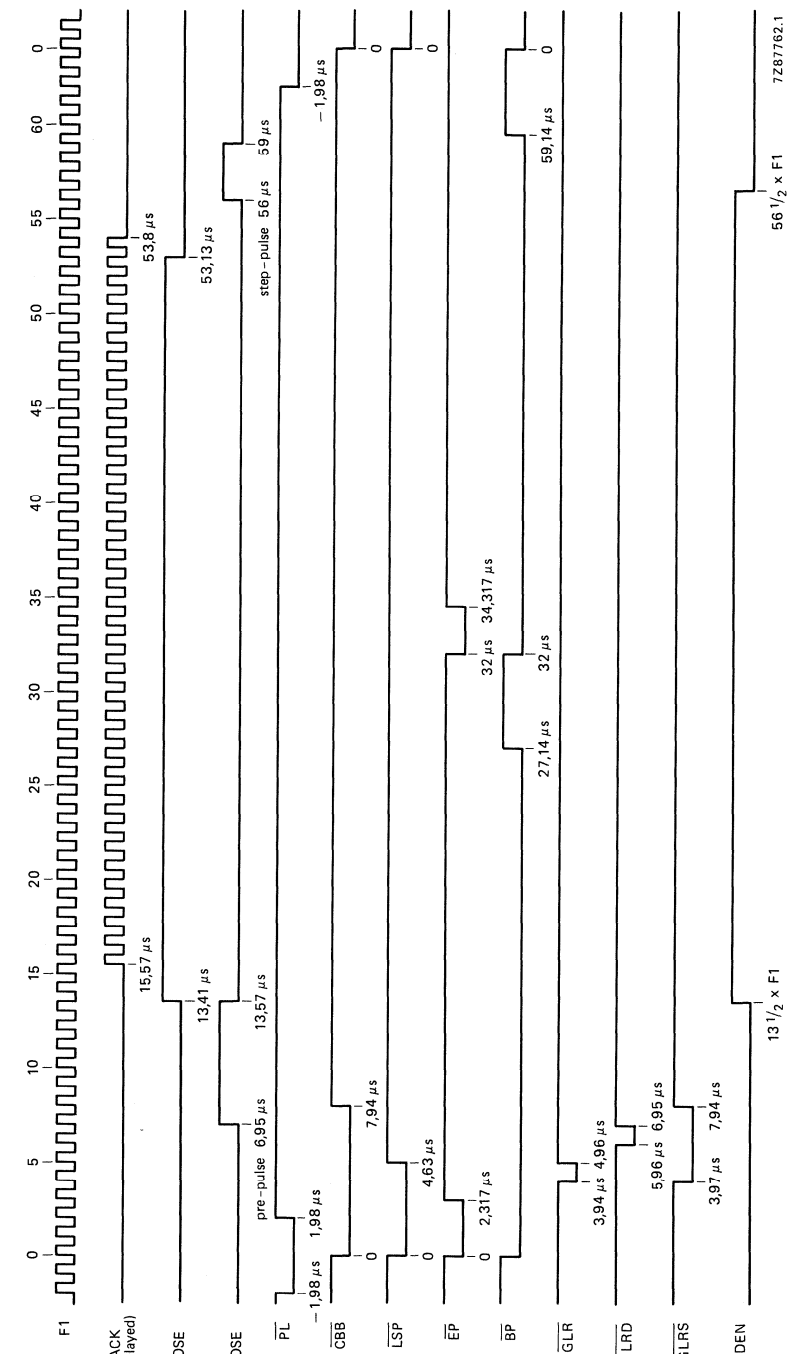


Fig. 3 Timing diagram showing the line-rate signals.

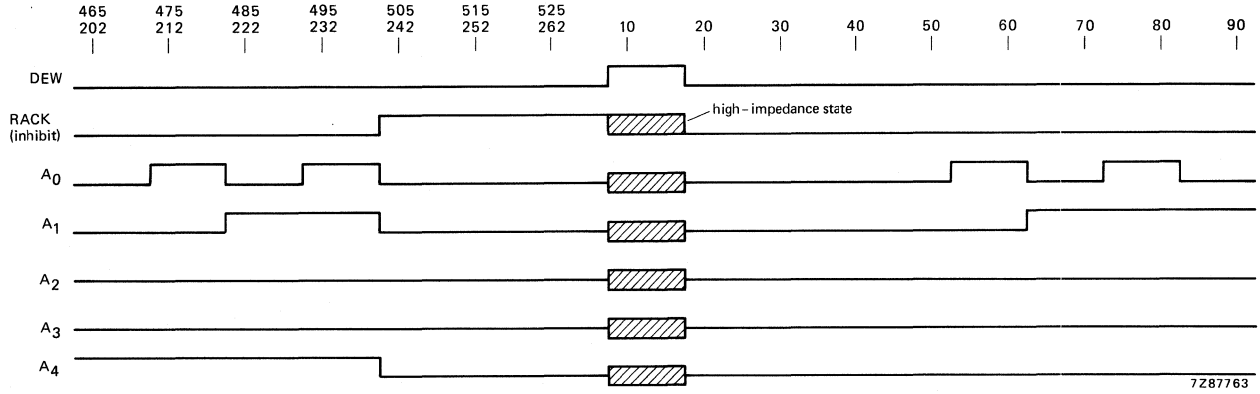


Fig. 4 Timing diagram showing the decoded signals from the field (picture) counters.

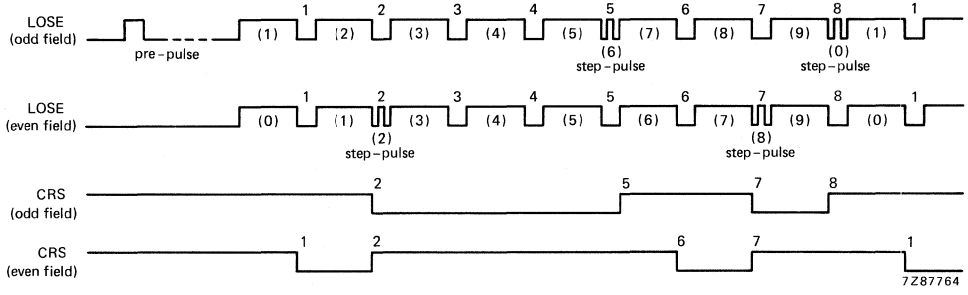


Fig. 5 Timing diagram showing the field-rate signals.

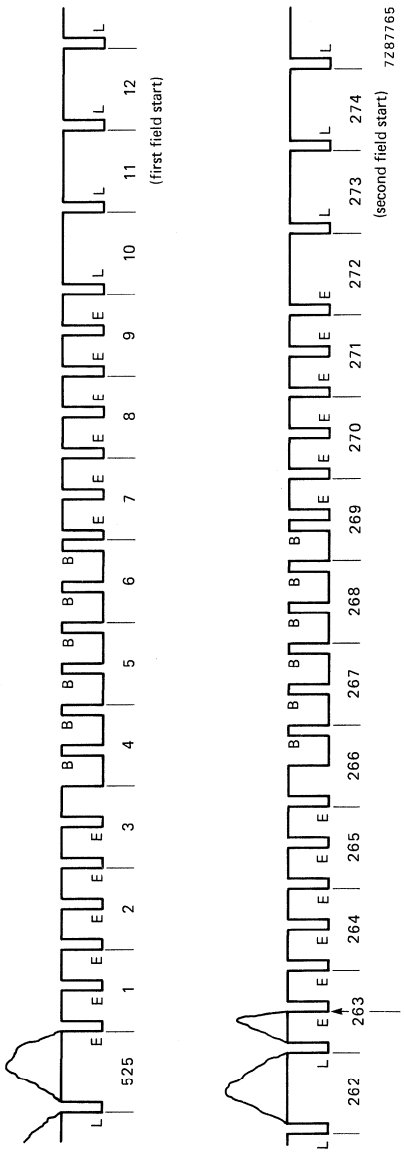
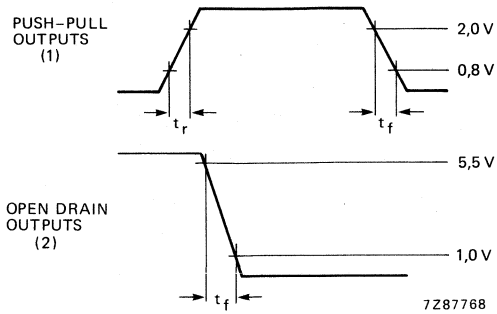


Fig. 6 After hours sync waveforms.

L = line sync pulses (4,2 to 5,1 μs)
E = equalizing pulses (2,29 μs ± 10%)
B = broad pulses (26,4 to 28 μs)



(1) These outputs will be tested with simulated TTL loads and with the load resistors adjusted such that the correct current conditions are obtained.

(2) These outputs will be tested with 3 kΩ resistors to the +6 V line for outputs $\overline{PL}$ and $\overline{CBB}$.

Fig. 7 Definition of the rise and fall times for the output stages.

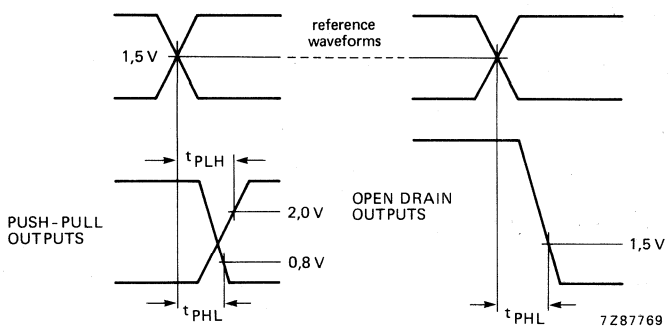


Fig. 8 Definition of the propagation delays for the output stages.

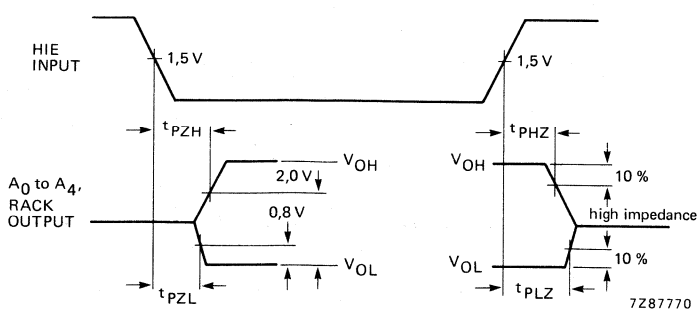


Fig. 9 Definitions of the high-impedance state propagation delay times.

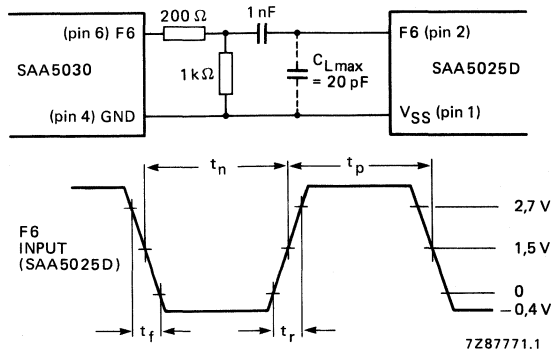


Fig. 10 Recommended 6 MHz interface circuitry between the SAA5025D and the SAA5030 (input F6). With this circuitry the F6 input will be set to a level of approximately −0,4 V in the LOW state. This is acceptable as the internal clamping diode in the F6 input of the SAA5025D provides an adequate current clamp; also shown is the F6 input waveform with the appropriate definitions.

The duty factor is defined as: $\frac{t_p}{t_p + t_n} \times 100\%$

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. **V_{SS} – ground (0 V)**

2. **F6 – 6,041957 MHz clock input**

   Obtained from video processor (SAA5030) or other source. The permissible mark/space ratio is in the range from 56:44 to 40:60 (see also Fig. 10).

3. **TR6 – 6,041957 MHz clock output**

   Dot-rate clock for Teletext character generator SAA5050 series.

4. **F1 – 1,007 MHz clock output**

   Character-rate clock for Teletext character generator SAA5050 series.

5. **$\overline{\text{AHS}}$ – after hours sync output**

   A composite sync waveform consisting of a successive sequence of line sync pulses ($\overline{\text{LSP}}$) followed by six equalizing pulses ($\overline{\text{EP}}$), six broad pulses ($\overline{\text{BP}}$) and six equalizing pulses ($\overline{\text{EP}}$), and is followed by another sequence of $\overline{\text{LSP}}$. This composite sync waveform occurs at the end and beginning of each field/picture (see also Fig. 6).

6. **DE – display enable input**

   A LOW level signal from the Teletext acquisition and control circuit (SAA5040 series) to this input switches output DEN to the LOW state.

7. **FLR – fast line reset input**

   This is the input for a positive-going pulse with a duration of 0,5 μs to 63 μs which resets the line rate counter ($\div$ 64).
   After accepting an FLR pulse, further resets are inhibited for one line period of approximately 63,5 μs.

8. **$\overline{\text{GLRD}}$ – general line reset delay output**

   A negative-going pulse with a duration of 993 ns which commences 5,96 μs from the start of each line (see also Fig. 3).

9. **$\overline{\text{GLR}}$ – general line reset output**

   A negative-going pulse with a duration of 993 ns which commences 3,97 μs from the start of each line (see also Fig. 3).

10. **$\overline{\text{GLRS}}$ – general line reset starting output**

    A negative-going pulse with starting 3,97 μs and ending 7,94 μs from the start of each line (see also Fig. 3).

11. **$\overline{\text{PL}}$ – phase lock open drain output**

    This open drain output is used to lock the oscillator in the SAA5030 to the line rate. It is a negative-going pulse with a duration of 3,96 μs which starts at 61,58 μs on one line and it ends at 1,98 μs after the start of the following line (see also Fig. 3).

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

12. $\overline{CBB}$ – colour burst blanking output

This open-drain output blanks the colour burst in the SAA5030. It is a 7,94 μs negative-going pulse which starts at the beginning of each line (t = 0; see also Fig. 3).

13. FS – field (picture) sync input

This input accepts a positive-going pulse of approximately 160 μs duration. Its leading edge occurs during the second half of line one on even fields (half picture) and correspondingly in odd fields (other half picture). It is ignored during the odd field.

14. CRS – character rounding select output

The output signal starts HIGH during the even field (lines 1 to 263), goes LOW after the 1st LOSE pulse, again HIGH after the 2nd LOSE pulse, then LOW after the 6th LOSE pulse and finally HIGH at the end of the 7th LOSE pulse. This sequence repeats every 8 lines (every row) for the entire display period (see also Fig. 5). For the odd field (lines 264 to 525) CRS starts HIGH, goes LOW after the 2nd LOSE pulse, again HIGH after the 5th LOSE pulse, then LOW after the 7th LOSE pulse and finally HIGH at the end of the 8th LOSE pulse. This sequence repeats every 8 lines (every row) for the entire display period (see also Fig. 5).

15. V_{DD} – positive supply (+ 5 V)

16. LOSE – load output shift register enable output

This is a positive-going output pulse of 39,72 μs duration commencing 13,41 μs from start of line valid during line 47 to 238 inclusive, for the even field. A step-pulse starting at the count of 3 characterrate clock pulses (F1) after the 2nd and 7th LOSE pulses and of the count of 3 character-rate clock pulses repeated every row is included. For the odd field, the LOSE pulse is preceded by a pre-pulse of 7 μs duration commencing 7,41 μs in line 20 and has a step-pulse after the 5th and 8th pulse, repeated every row (see also Fig. 5).

17. DEW – data entry window output

This output defines the period during which data may be extracted from the incoming television signal. It is HIGH during line 7 to 18 inclusive for the even fields and line 270 to 281 inclusive for the odd fields. The positive-going pulse has a duration of 762,67 μs and commences at 6,95 μs from the start of the line (see also Fig. 4).

18. DEN – display enable output

The output pulse is positive-going at 13,5 μs from the start of a line to 56,5 μs and is active during line 47 to 238 inclusive if the DE input is HIGH. If the DE input is LOW, the DEN is held in the LOW state.

19. $\overline{TLC}$ – transmitted large characters input

When this input is LOW, it enables rows of double-height characters to be displayed as required. Large characters descend into the next memory row address location. $\overline{TLC}$ is always HIGH (i.e. small) for the first line of a row, even if it contains large characters.

20. HIE – high impedance enable input

When this input is in the HIGH state it will force the RACK and memory row address output into the high-impedance state. For normal Teletext operation this input should be connected to the DEW output (pin 17).

21. $\overline{BCS}$ – big character select input

For normal size character display this input signal must be HIGH while a LOW gives double-height characters.

22. $\overline{T}$/B – top/bottom select input

When both $\overline{BCS}$ and $\overline{T}$/B are LOW the top half of a page is displayed with double-height characters. If $\overline{T}$/B is HIGH and $\overline{BCS}$ is LOW the bottom half of the page is displayed also with double-height characters.

23 to 27. A_0 to A_4 – memory row address outputs (3-state)

These binary count outputs sequencing from 00000 (count 0) to address 10111 (count 23) for the 40 x 24 format.
The binary count changes every 8 TV lines per row in the display period of line 47 to 238 inclusive for the 24 row display. The count changes between 6,5 μs and 9,0 μs during the line period.

28. RACK – read address clock output

This is the read address clock output to the SAA5045 (GALA) column address counter during the display period. It consists of 39 positive pulses at the 1,007 MHz rate starting at 13,57 μs from the start of the line period with the last negative edge occuring at 51,8 μs. This sequence is active on line 45 to 238 inclusive. RACK is delayed by two F1 clock periods for the whole of the field when input DE is LOW for the whole of line 39. On line 19 to 44 inclusive output RACK is permanently delayed by two F1 clock periods, unaffected by DE.

DEVELOPMENT DATA

Note

In the big character top mode the memory row address count is 0 to 11 and in the big character bottom mode the count is 12 to 23.
Each big character row is equal to 16 television lines.

The memory row addresses are held LOW for one line period starting 6,5 μs to 9 μs from the beginning of line 36 which is only valid in the big character bottom mode.

TELETEXT VIDEO PROCESSOR

The SAA5030 is a monolithic bipolar integrated circuit used for teletext video processing. It is one of a package of four circuits to be used in teletext tv data systems. The SAA5030 extracts data and data clock information from the television composite video signal and feeds this to the Acquisition and Control circuit SAA5040. A 6 MHz crystal controlled phase locked oscillator is incorporated which drives the Timing Chain circuit SAA5020. An adaptive sync separator is also provided which derives line and field sync pulses from the input video in order to synchronise the timing chain.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	nom.	12	V
Supply current (V_{CC} = 12 V)	I_{CC}	typ.	110	mA
Video input amplitude (sync-white)	$V_{16video(p-p)}$	nom.	2.4	V
Teletext data input amplitude	$V_{16teletext(p-p)}$	nom.	1.1	V
Sync amplitude	$V_{16sync(p-p)}$	nom.	0.7	V
Operating ambient temperature range	T_{amb}		0 to + 70	°C

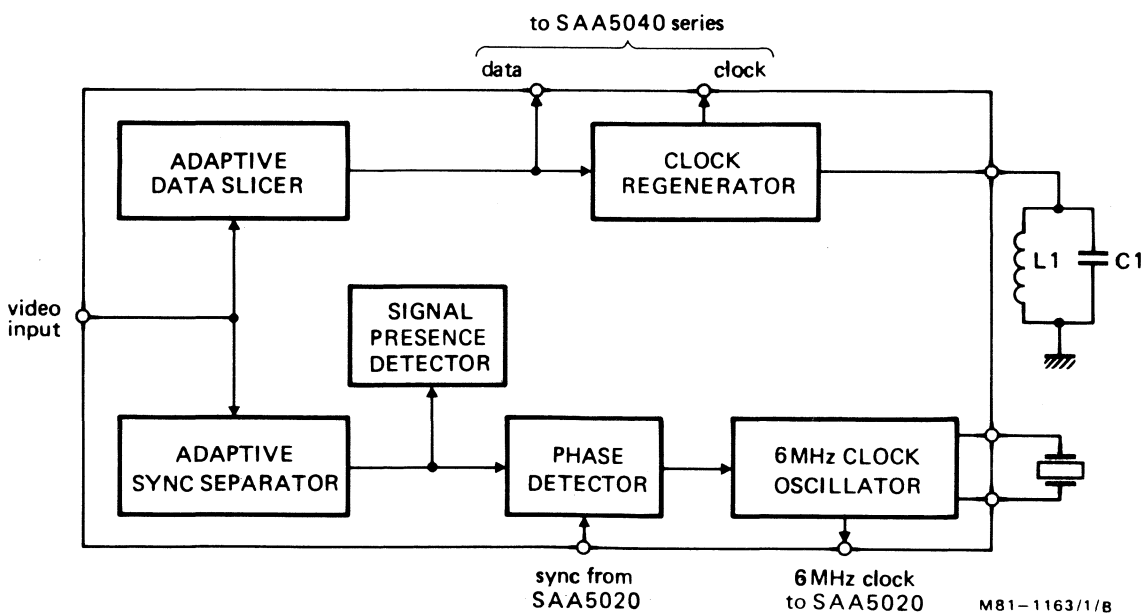


Fig.1 Block diagram

PACKAGE OUTLINE

24-lead DIL; plastic (SOT–101A with internal heat spreader).

PINNING

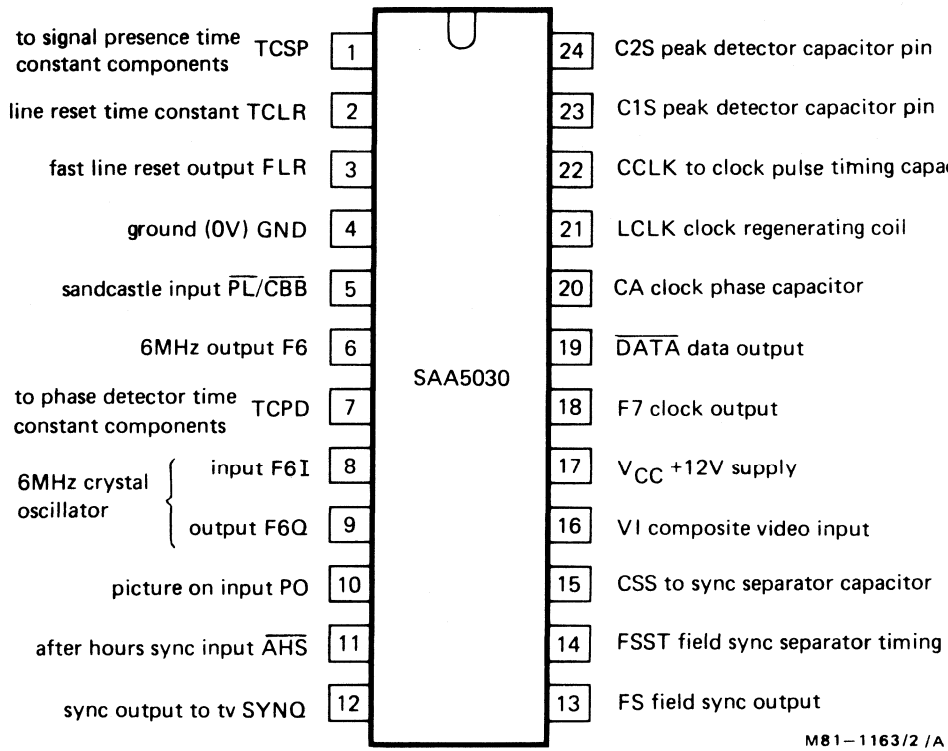


Fig.2 Pinning diagram

RATINGS Limiting values in accordance with the Absolute Maximum System. (IEC134)

Voltages

Supply voltage	V_{17-4}	V_{CC}	max.	13.2	V
Input voltages	V_{5-4}	V_I	max.	9.0	V
	V_{10-4}	V_I	max.	V_{CC}	V
	V_{11-4}	V_I	max.	7.5	V

Temperatures

Storage temperature range	T_{stg}	−20 to +125	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C ←

CHARACTERISTICS (At T_{amb} = 25 °C, V_{CC} = 12 V and with external components as shown in Fig.3 unless otherwise stated).

		min.	typ.	max.	
Supply voltage	V_{CC}	10.8	12.0	13.2	V
Supply current (V_{CC} = 12.0 V)	I_{CC}	–	110	–	mA
Video input and sync separator					
Video input amplitude (sync to white) Fig.4	$V_{16video(p-p)}$	2.0	1.4	3.0	V
Source impedance, f = 100 kHz	$\lvert Z_s \rvert$	–	–	250	Ω
Sync amplitude	$V_{16sync(p-p)}$	0.07	0.7	1.0	V
Delay through sync separator	t_d	–	0.5	–	μs
Delay between field sync datum at pin 12 and the leading edge of separated field sync at pin 13 (Note 1, Fig.4)	t_d	32	48	62	μs
Field sync output					
V_O (LOW) (I_{13} = 20 μA)	V_{OL}	–	–	0.5	V
V_O (HIGH) ($-I_{13}$ = 100 μA)	V_{OH}	2.4	–	–	V

Crystal controlled phase-locked oscillator

Measured using a crystal with the following specification e.g. catalogue number 4322 143 03241

C_1 = 27.5 fF (typ.)

C_0 = 6.8 pF (typ.)

C_L = 20 pF

Trimability (C_L increased to 30 pF) > 750 Hz

Fundamental ESR < 50 Ω

		min.	typ.	max.	
Frequency	f_{F6}	–	6.0	–	MHz
Holding range		1.5	3.0	–	kHz
Catching range		1.5	3.0	–	kHz
Control sensitivity of phase detector measured as voltage at pin 7 with respect to phase difference between separated syncs and phase lock pulse $\overline{PL}$		–	0.3	–	mV/ns
Control sensitivity of oscillator measured as change in 6 MHz phase shift from pin 8 to pin 9 with respect to voltage at pin 7		–	2	–	deg/mV
Gain of sustaining amplifier, $V_{9\text{-}8}$ measured with input voltage of 100 $mV_{p\text{-}p}$ and phase detector immobilised		2.5	–	–	V/V
Output voltage of 6 MHz signal at pin 6, measured into 20 pF load capacitance; peak-to-peak value		–	5.5	–	V
Output rise and fall times at pin 6 into 20 pF load	t_r; t_f	–	–	30	ns
Data slicer and clock regenerator					
Teletext data input amplitude, pin 16 (Note 2, Fig.4); peak-to-peak value		–	1.1	–	V
Data input amplitude at pin 16 required to enable amplitude gate flip-flop; peak-to-peak value		–	0.46	–	V
Attack rate, measured at pins 23 and 24 with a step to pin 16 (positive)		–	15	–	V/μs
(negative)		–	9	–	V/μs

Data slicer and clock regenerator (continued)		min.	typ.	max.	
Decay rate, measured at pins 23 and 24 with a step input to pin 16		48	100	144	mV/μs
Width of clock coil drive pulses from pin 21 when clock amplitude is not being controlled (Note 3)		–	40	–	ns
Clock hangover measured at pin 18 as the time the clock coil continues ringing after the end of data (Note 4)		20	–	–	Clock Periods
Clock and data output voltages at pins 18 and 19 measured with 20 pF load capacitance; peak-to-peak value		–	5.5	–	V
Output rise and fall times at pins 18 and 19 into 20 pF loads	t_r; t_f	–	–	30	ns
Sandcastle input					
Sandcastle detector thresholds, pin 5					
Phase lock pulse (PL) on		2	–	–	V
Phase lock pulse off		–	–	3	V
Blanking pulse ($\overline{CBB}$) on		4.5	–	–	V
Blanking pulse off		–	–	5.5	V
Dual polarity sync buffer					
After hours sync ($\overline{AHS}$) pulse input pin 11		–			
Threshold for $\overline{AHS}$ active			–	1.0	V ←
Threshold for $\overline{AHS}$ off		2.0	–	–	V ←
Picture On (PO) input, pin 10					
Threshold for PO active		2.0	–	–	V ←
Threshold for PO off		–	–	1.0	V ←
Sync output, pin 12					
$\overline{AHS}$ output with pin 10 < 1 V (Note 5) peak-to-peak value		–	0.7	–	V
Composite sync output with pin 10 > 2 V (Notes 5 and 6); peak-to-peak value		–	0.7	1.0	V
Output current		–	–	3	mA
Line reset and signal presence detectors					
Schmitt trigger threshold on pin 2 to inhibit line reset output at pin 3 (syncs coincident)		–	6.2	–	V
Schmitt trigger threshold on pin 2 to permit line reset output at pin 3 (syncs non-coincident)		–	7.8	–	V
Line reset output V_{OL} (I_3 = 20 μA)		–	–	0.5	V
Line reset output V_{OH} ($-I_3$ = 100 μA)		2.4	–	–	V
Signal presence Schmitt trigger threshold on pin 2 below which the circuit accepts the input signal		–	6.0	–	V
Signal presence Schmitt trigger threshold on pin 2 above which the input signal is rejected.		–	6.3	–	V

Notes

1. This is measured with the dual polarity buffer external resistor connected to give negative-going syncs. The measurement is made after adjustment of the potential divider at pin 14 for optimum delay.
2. The teletext data input contains binary elements as a two level NRZ signal shaped by a raised cosine filter. The bit rate is 6.9375 M bit/s. The use of odd parity for the 8-bit bytes ensures that there are never more than 14-bit periods between each data transition.
3. This is measured by replacing the clock coil with a small value resistor.
4. This must be measured with the clock coil tuned and using a clock-cracker signal into pin 16. The clock-cracker is a teletext waveform consisting of only one data transition in each byte.
5. With the external resistor connected to the ground rail, syncs are positive-going centred on +2.3 V. With the resistor connected to the supply rail, syncs are negative-going centred on +9.7 V.
6. When the composite sync is being delivered, the level is substantially the same as that at the video input.

APPLICATION DATA

The function is quoted against the corresponding pin number

Pin No.

1. **Signal presence time constant**

   A capacitor and a resistor connected in parallel between this pin and supply determine the delay in operation of the signal presence detector.

2. **Line reset time constant**

   A capacitor between this pin and supply integrates current pulses from the coincidence detector; the resultant level is used to determine whether to allow FLR pulses (see pin 3).

3. **Fast line reset output (FLR)**

   Positive-going sync pulses are produced at this output if the coincidence detector shows no coincidence between the syncs separated from the incoming video and the $\overline{CBB}$ waveform from the timing chain circuit SAA5020. These pulses are sent to the timing chain circuit and are used to reset its counters, so as to effect rapid lock-up of the phase locked loop.

4. **Ground** (0 V)

5. **Sandcastle input ($\overline{PL}$ and $\overline{CBB}$)**

   This input accepts a sandcastle waveform which is formed from $\overline{PL}$ and $\overline{CBB}$ from the timing chain SAA5020. $\overline{PL}$ is obtained by slicing the waveform at 2.5 V, and this, together with separated sync, are inputs to the phase detector which forms part of the phase locked loop. When the loop has locked up, the edges of $\overline{PL}$ are nominally 2 μs before and 2 μs after the leading edge of separated line syncs.
   CBB is obtained by slicing the waveform at 5 V, and is used to prevent the data slicer being offset by the colour burst.

6. **6 MHz output (F6)**

   This is the output of the crystal oscillator (see pins 8 and 9), and is taken to the timing chain circuit SAA5020 via a series capacitor.

7. **Phase detector time constant**

   The integrating components for the phase detector of the phase locked loop are connected between this pin and supply.

APPLICATION DATA (continued)

8, 9. **6 MHz crystal**

A 6 MHz crystal in series with a trimmer capacitor is connected between these pins. It forms part of an oscillator whose frequency is controlled by the voltage on pin 7, which forms part of the phase locked loop.

10. **Picture On input (PO)**

The PO signal from the acquisition and control circuits SAA5040 Series is fed to this input and is used to determine whether the input video (pin 16) or the $\overline{\text{AHS}}$ waveform (pin 11) appears at pin 12.

11. **After hours sync ($\overline{\text{AHS}}$)**

A composite sync waveform $\overline{\text{AHS}}$ is generated in the timing chain circuit SAA5020 and is used to synchronise the tv (see pin 10).

12. **Sync output to tv**

Either the input video of $\overline{\text{AHS}}$ is available at this output dependent on whether the PO signal is HIGH or LOW. In addition either signal may be positive-going or negative-going, dependent on whether the load resistor at this output is connected to ground or supply.

13. **Field sync output (FS)**

A pulse, derived from the input video by the field sync separator, which is used to reset the line counter in the timing chain circuit SAA5020.

14. **Field sync separator timing**

A capacitor and adjusting network is connected to this pin and forms the integrator of the field sync separator.

15. **Sync separator capacitor**

A capacitor connected to this pin forms part of the adaptive sync separator.

16. **Composite video input (VI)**

The composite video is fed to this input via a coupling capacitor.

17. **Supply voltage (+12 V)**

18. **Clock output**

The regenerated clock, after extraction from the teletext data, is fed out to the acquisition and control circuits SAA5040 Series via a series capacitor.

19. **Data output**

The teletext data is sliced off the video waveform, squared up and latched within the SAA5030. The latched output is fed to the acquisition and control circuits SAA5040 Series via a series capacitor.

20. **Clock decoupling**

A 1 nF capacitor between pin 20 and ground is required for clock decoupling.

21. **Clock regenerator coil**

A high-Q parallel tuned circuit is connected between this pin and an external potential divider. The coil is part of the clock regeneration circuit (see pin 22).

APPLICATION DATA (continued)

22. **Clock pulse timing capacitor**

Short pulses are derived from both edges of data with the aid of a capacitor connected to this pin. The resulting pulses are fed, as a current, into the clock coil connected to pin 21. Resulting oscillations are limited and taken to the acquisition and control circuits SAA5040 Series via pin 18.

23, 24 **Peak detector capacitors**

The teletext data is sliced with an automatic data slicer whose slicing level is the mid-point of two peak detectors working on the video signal. Storage capacitors are connected to these pins for the negative and positive peak detectors.

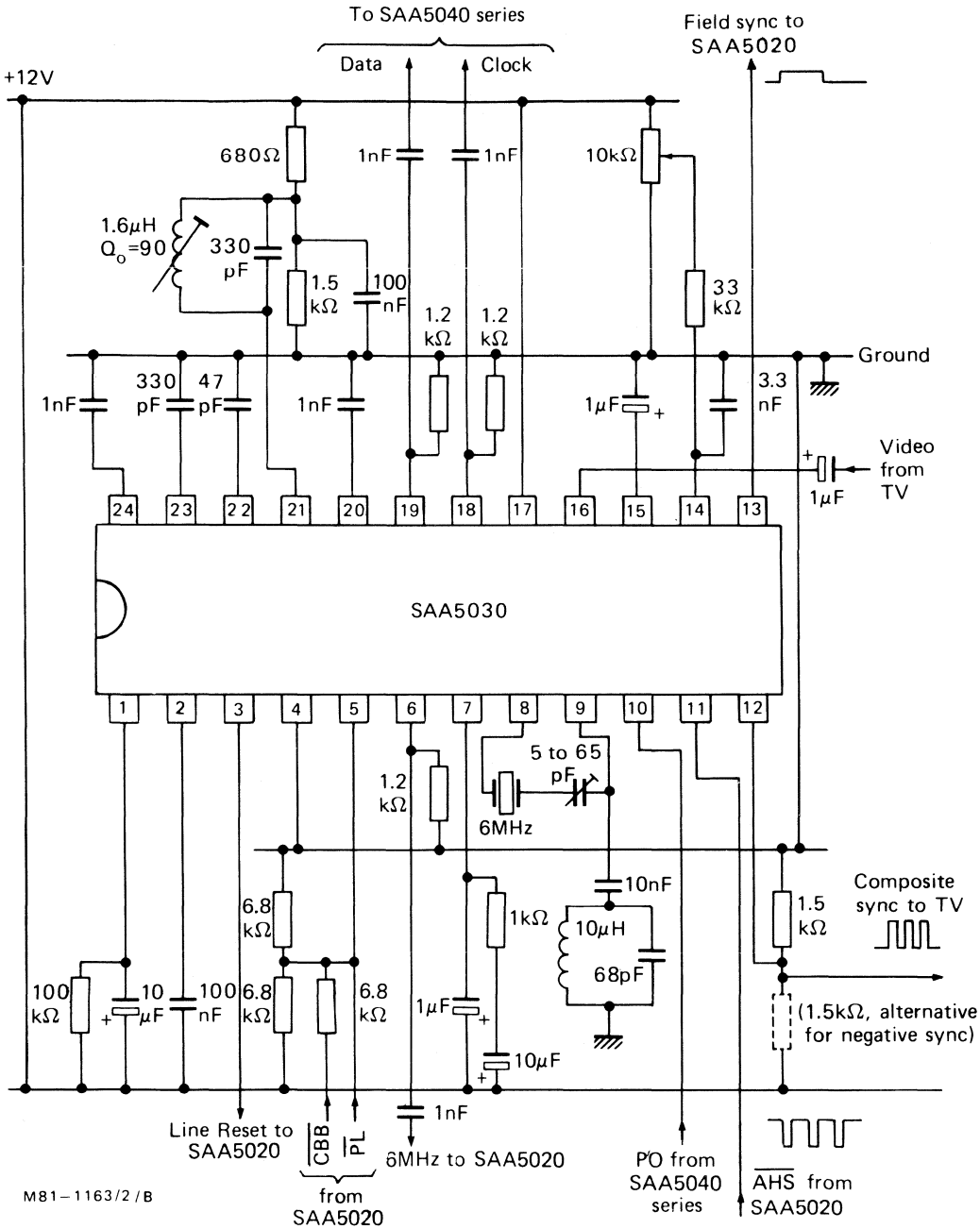


Fig.3 Peripheral circuit

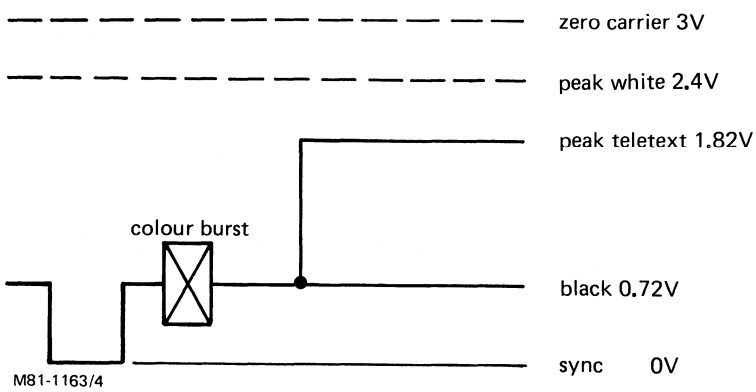


Fig.4 Part of teletext line, with burst showing nominal levels.

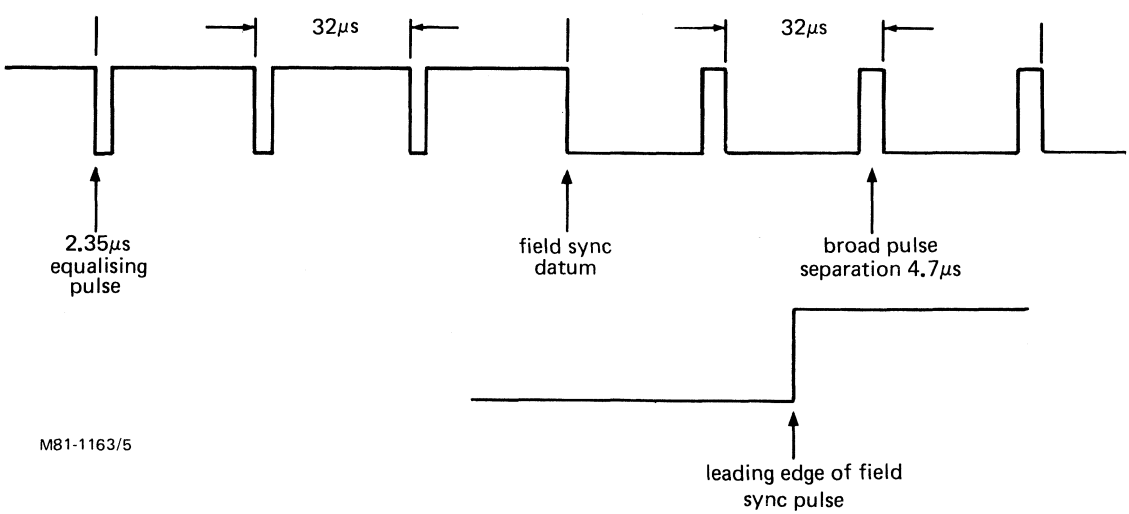


Fig.5 Detail of idealised composite sync waveform.

TELETEXT ACQUISITION AND CONTROL CIRCUIT

GENERAL

The SAA5040A, SAA5040B, SAA5040C, SAA5041, SAA5042 and form the SAA5040 series of MOS N-channel integrated circuits. They perform the control, data acquisition and data routing functions of the teletext system. The circuits differ in the on-screen display that is provided and in the decoding of the remote control commands. The functions of the circuits are detailed in Tables 1, 2 and 3; throughout the remainder of the data the SAA5040 is referred to when the complete series of the circuits is being described.

The SAA5040 is a 28-lead device which receives serial teletext data and clock signals from the remote control systems incorporating the SAA5012 or SAB3022, SAB3023 decoder circuits. The SAA5040 selects the required page information and feeds it in parallel form to the teletext page memory.

The SAA5040 works in conjunction with the SAA5020 timing chain and the SAA5050 series of character generators.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	80	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

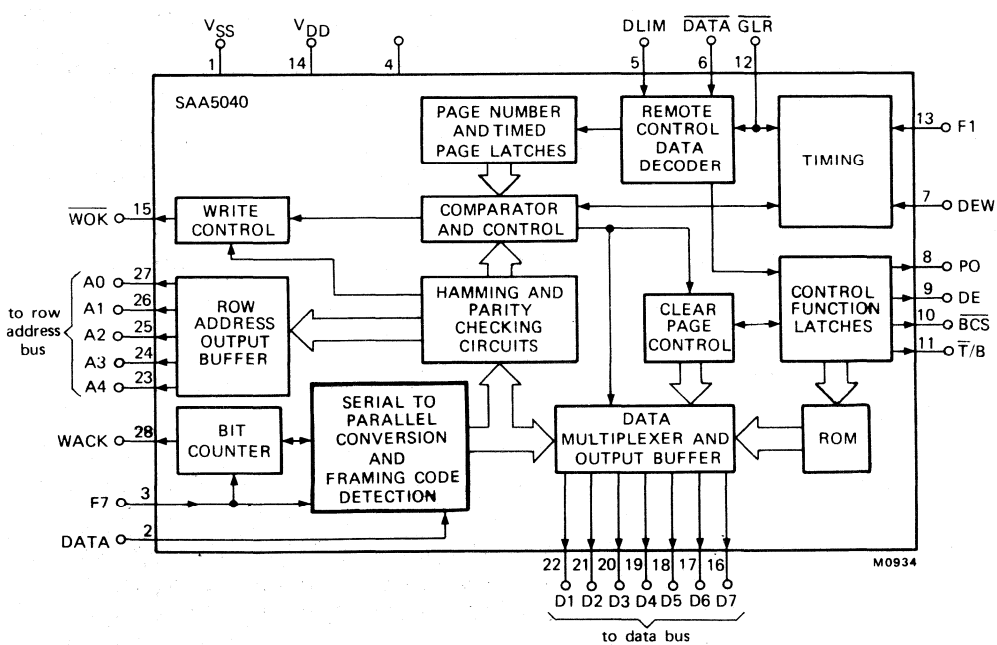


Fig.1 Block diagram.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117)

PINNING

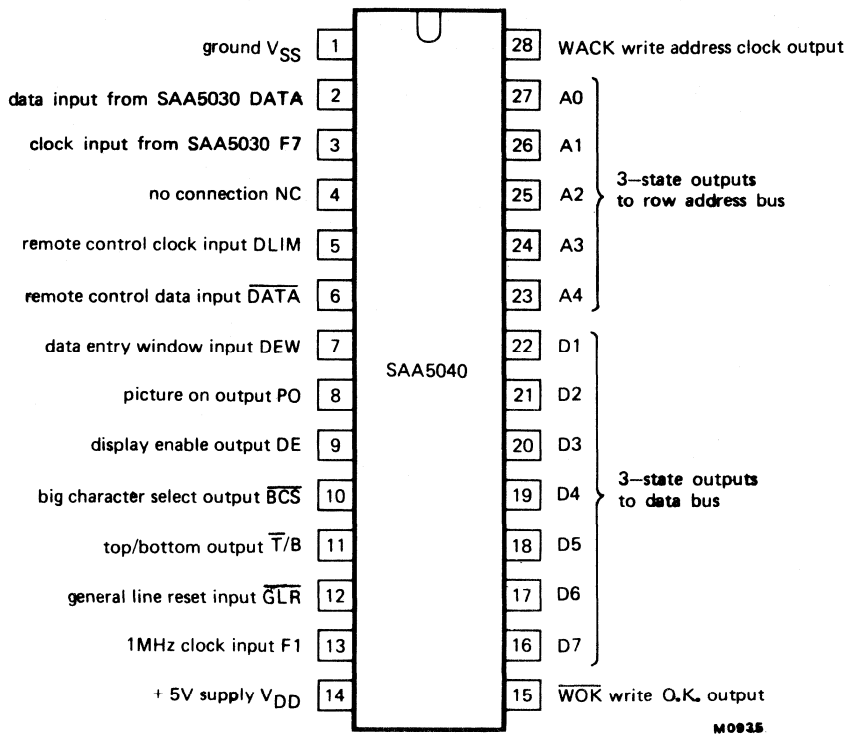


Fig.2 Pinning diagram.

DESCRIPTION

The circuit consists of two main sections.

a) Data acquisition section

The basic input to this section is the serial teletext data stream DATA from the SAA5030 video processor circuit. This data stream is clocked at a 6.9375 MHz clock rate (F7) from the SAA5030. The incoming data stream is processed and sorted so that the page of data selected by the user is written as 7-bit parallel words into the system memory. Hamming and parity checks are performed on the incoming data to reduce errors. Provision is also made to process the control bits in the page header.

b) Control section

The basic input to this section is the 7-bit serial data ($\overline{DATA}$) from the remote control decoder circuit such as the SAA5012 or SAB3012. This is clocked by the DLIM signal.
The remote control commands are decoded and the control functions are stored.
Full details of the remote control commands used in the various SAA5040 series options are given in Tables 1, 2 and 3 below. The control section also writes data into the page memory independently of the data acquisition section. This gives an on-screen display of certain user-selected functions such as page number and programme name.
The 3-state data and address outputs to the system memory are set to high impedance state if certain remote control commands are received (e.g. viewdata mode). This is to allow another circuit to access the memory using the same address and data lines. The address lines are also high impedance while the acquisition and control circuit is not writing into the memory.
Further information on the control of the complete teletext system is available.
The circuit is designed in accordance with the September 1976 Broadcast Teletext specification published by BBC/IBA/BREMA.
A typical circuit diagram of a teletext decoder is shown in Fig.7.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS devices").

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Voltages (with respect to pin 1)

		min.	max.	
Supply voltage (pin 14)	V_{DD}	−0.3	7.5	V
Input voltage (all inputs)	V_I	−0.3	7.5	V
Output voltage (pin 8)	V_{O8}	−0.3	13.2	V
Output voltage (all other outputs)	V_O	−0.3	7.5	V
Temperatures				
Storage temperature range	T_{stg}		−20 to +125	°C
Operating ambient temperature range	T_{amb}		−20 to +70	°C

CHARACTERISTICS

		min.	typ.	max.	
Supply voltage (pin 14)	V_{DD}	4.5	–	5.5	V

The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.

Supply current	I_{DD}	–	80	120	mA
Inputs					
F7 DATA (pin 2), **F7 CLOCK** (pin 3)					
Input voltage; HIGH	V_{IH}	3.5	–	5.5	V
Input voltage; LOW Note 1	V_{IL}	–	–	0.5	V
Rise time	t_r	–	–	30	ns
Fall time	t_f	–	–	30	ns
Input resistance (measured at 4 V)	R_I	2	–	18	MΩ
Input capacitance	C_I	–	–	7	pF
F1 (pin 13)					
Input voltage; HIGH	V_{IH}	2.4	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Rise time	t_r	–	–	50	ns
Fall time	t_f	–	–	30	ns
Input capacitance	C_I	–	–	7	pF
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	μA
All other inputs					
DLIM (pin 5), **$\overline{\text{DATA}}$** (pin 6), **DEW** (pin 7), **$\overline{\text{GLR}}$** (pin 12)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Input capacitance	C_I	–	–	7	pF
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	μA
Outputs					
DE (pin 9), **$\overline{\text{BCS}}$** (pin 10), **$\overline{\text{T}}$/B** (pin 11) (with internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 400 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH $-I_{OH}$ = 50 μA for pin 9 $-I_{OH}$ = 30 μA for pin 10 $-I_{OH}$ = 20 μA for pin 11	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time	t_r	–	–	10	
Output voltage fall time	t_f	–	–	1	μs
Output capacitance	C_O	–	–	7	pF
Output current with output in HIGH state (V_O = 0.5 V)	$-I_O$	50	–	500	μA

CHARACTERISTICS Continued

		min.	typ.	max.	
PO (pin 8) (with internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 140 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 50 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	10	μs
Output capacitance	C_O	–	–	7	pF
Output current with output in HIGH state (V_O = 0.5 V)	$-I_O$	50	–	500	μA
D1 to D7 (pins 16 to 22) (3-state)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	100	ns
Output leakage current in 'OFF' state (V_O = 0 to 5.5 V)	$\pm I_{ORoff}$	–	–	10	μA
Output capacitance	C_O	–	–	7	pF
$\overline{\text{WOK}}$ (pin 15) (3-state with internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 400 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time (C_L = 80 pF) (Note 3)	t_r	–	–	50	ns
Output voltage fall time (C_L = 80 pF) (Note 3)	t_f	–	–	100	ns
Output current with 3-state 'OFF' (V_O = 0.5 V)	$-I_{ORoff}$	80	–	500	μA
Output capacitance	C_O	–	–	7	pF
WACK (pin 28) (3-state)					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time (C_L = 40 pF) (Note 3)	t_r	–	–	50	ns
Output voltage fall time (C_L = 40 pF) (Note 3)	t_f	–	–	300	ns
Output leakage current in 'OFF' state (V_O = 0 to 5.5 V)	$\pm I_{ORoff}$	–	–	10	μA
Output capacitance	C_O	–	–	7	pF
A0 to A2 (pins 25 to 27) (3-state)					
Output voltage; LOW (I_{OL} = 200 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 90 pF) (Note 3)	t_r, t_f	–	–	300	ns
Output leakage current in 'OFF' state (V_O = 0 to 5.5 V)	$\pm I_{ORoff}$	–	–	10	μA
Output capacitance	C_O	–	–	7	pF

CHARACTERISTICS (Continued)

Outputs

		min.	typ.	max.	
A3 and A4 (pins 23 and 24) (3-state)					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	300	ns
Output leakage current in 'OFF' state (V_O = 0 to 5.5 V)	$+I_{ORoff}$	–	–	10	μA
Output capacitance	C_O	–	–	7	pF

TIMING CHARACTERISTICS

Teletext Data and Clock (F7 DATA + F7 CLOCK) (Note 2 and Fig.3)					
F7 Clock cycle time	TF_7	144	–	–	ns
F7 Clock duty cycle (HIGH to LOW)		30	–	70	%
F7 Clock to data set-up time	t_{SU}	–	60	–	ns
F7 Clock to data hold time	t_{HOLD}	–	40	–	ns
Control $\overline{\text{DATA}}$ and Clock ($\overline{\text{DATA}}$ + DLIM) (Note 3 and Fig.4)					
DLIM Clock HIGH time	t_{CH}	6.5	8	Note 4	μs
DLIM Clock LOW time	t_{CL}	3.5	8	60	μs
DLIM to DATA set-up time	t_{SU}	0	14	–	μs
DLIM to DATA hold time	t_{HOLD}	8	14	–	μs
Writing Teletext data into memory during DEW (Fig.5)					
WACK cycle time	T_{WACK}	1150	–	–	ns
WACK rising edge to $\overline{\text{WOK}}$ falling edge	t_{AWW}	250	–	450	ns
WACK rising edge to $\overline{\text{WOK}}$ rising edge	t_{WRW}	150	–	310	ns
$\overline{\text{WOK}}$ pulse width	t_{WPD}	300	–	–	ns
Data output set-up time	t_{DW}	330	–	–	ns
Data output hold time	t_{DH}	0	–	–	ns
Row address set-up time before first $\overline{\text{WOK}}$	t_{RAW}	190	–	–	ns
Row address valid time after last $\overline{\text{WOK}}$	t_{RWR}	0	–	–	ns

TIMING CHARACTERISTICS

Writing Header information into memory during tv line 40

(Fig.6)

This arrangement is a combined phasing of the SAA5040 and the SAA5020 and is therefore referred to F1 input. The first $\overline{WOK}$ is related to F1 No 14½ from the SAA5020

		min.	typ.	max.	
F1 Clock cycle time		1000	–	–	ns
Time from F1 to $\overline{WOK}$ falling edge	t_{WF}	300	–	500	ns
Time from F1 to $\overline{WOK}$ rising edge	t_{FW}	0	–	120	ns
Data output set-up time	t_{DW}	330	–	–	ns
Data output hold time	t_{DH}	0	–	–	ns

Notes

1. These inputs may be a.c. coupled. Minimum rating is −0.3 V but the input may be taken more negative if a.c. coupled.
2. Transition times measured between 0.5 and 3.5 volt levels.
   Delay times are measured from 1.5 V level.
3. Transition times measured between 0.8 and 2.0 volt levels.
   Delay times are measured from 1.5 V level.
4. There is no maximum DLIM cyle time provided the DLIM duty cycle is such that $t_{CLmax.}$ requirement is not exceeded.

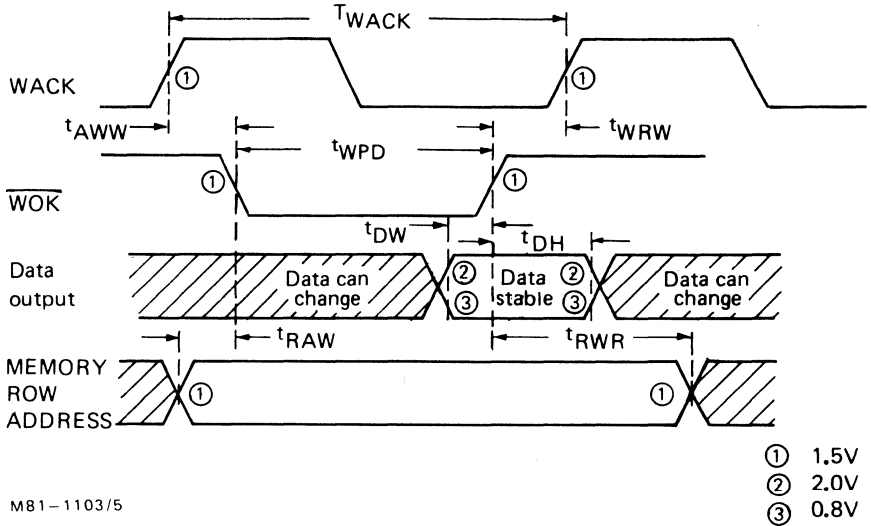


Fig.5 Writing teletext data into memory during DEW

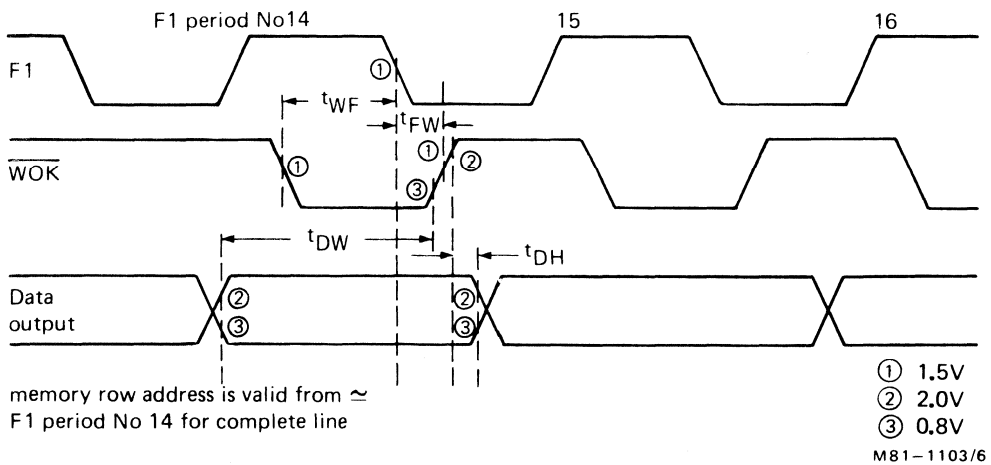


Fig.6 Writing data into memory during tv line 40

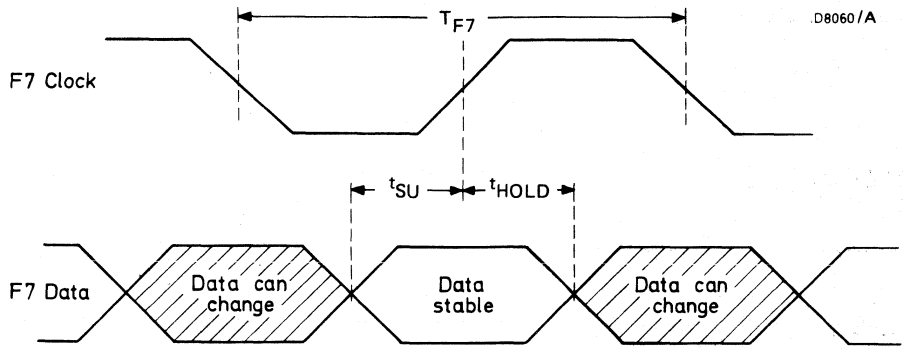


Fig.3 Teletext data timing

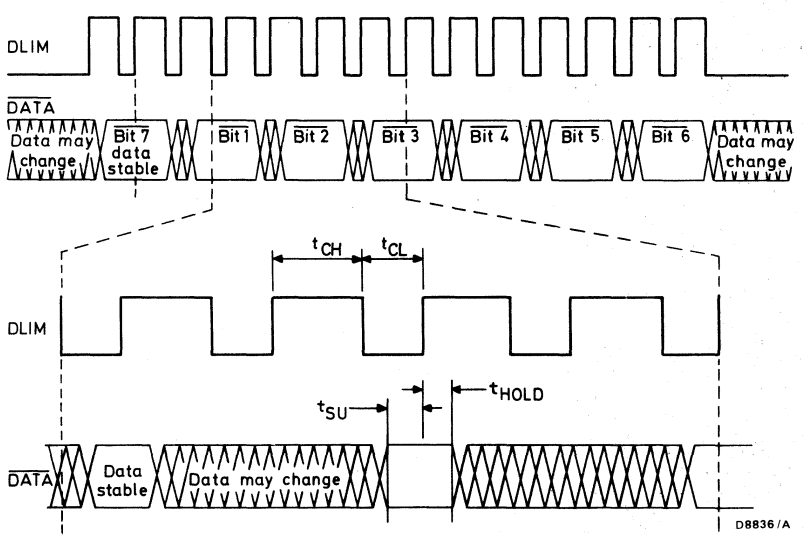


Fig.4 Remote control data input timing

APPLICATION DATA

The function is quoted against the corresponding pin number

Pin No.

1. V_{SS} Ground - 0 V
2. **DATA Data input from SAA5030**

   This input is a serial data stream of broadcast teletext data from the SAA5030 video processor, the data being at a rate of 6.9375 MHz.
   This input from the SAA5030 is a.c. coupled with internal d.c. restoration of the signal levels.
3. **F7 Clock input from SAA5030**

   This input is a 6.9375 MHz clock from the SAA5030 video processor which is used to clock the teletext data acquisition circuitry. The positive edge of this clock is nominally at the centre of each teletext data bit.
   This input from the SAA5030 is a.c. coupled with internal d.c. restoration of the signal levels.
5. **DLIM Remote control clock input**

   This input from the remote control receiver decoder is used to clock remote control data into the SAA5040. The positive-going edge of every second clock pulse is nominally in the centre of each remote control data bit.
6. **$\overline{\text{DATA}}$ Remote control data**

   This input is a 7-bit serial data stream from the remote control receiver decoder.
   This data contains the teletext and viewdata remote control user functions. The nominal data rate is 32 μs/bit. The remote control commands used in the SAA5040 series are shown in Tables 1, 2 and 3.
7. **DEW Data entry window**

   This input from the SAA5020 Timing Chain defines the period during which received teletext data may be accepted by the SAA5040. This signal is also used to enable the 5 memory address outputs (pins 23 to 27) and the 7-bit parallel data outputs (pins 16 to 22).
8. **PO Picture On**

   This output to the SAA5012, SAA5030 and SAA5050 circuits is a static level used for the selection of tv picture video 'on' or 'off'. The output is HIGH for tv picture 'ON', LOW for tv picture 'OFF'. The output has an internal pull-up to V_{DD}.
9. **DE Display enable**

   This output to the SAA5050 teletext character generator is used to enable the teletext display. The output is HIGH for display enabled, LOW for display disabled.
   The output is also forced to the LOW state during the DEW and tv line 40 periods and when a teletext page is cleared.
   The output has an internal pull-up to V_{DD}.
10. **$\overline{\text{BCS}}$ Big character select**

    This output to the SAA5020 timing chain and to the SAA5050 character generator is used to select double height character format under user control. The output is HIGH for normal height characters, LOW for double height characters. It is also forced to the HIGH state on page clear. The output has an internal pull-up to V_{DD}.
11. **$\overline{\text{T}}$/B Top/bottom**

    This output to the SAA5020 timing chain is used to select whether top or bottom half page is being viewed. The output is HIGH for bottom half page and LOW for top half page. It is also forced to the LOW state on page clear.
    The output has an internal pull-up to V_{DD}.

APPLICATION DATA

12. **$\overline{\text{GLR}}$ General line reset**

This input from the SAA5020 timing chain is used as a reset signal for internal control and display counter.

13. **F1**

This input is a 1 MHz clock signal from the SAA5020 timing chain used to clock internal remote control processing and encoding circuits.

14. **V_{DD} +5 V Supply**

This is the power supply input to the circuit.

15. **$\overline{\text{WOK}}$ Write O.K.**

This 3-state output signal to the system memory is used to control the writing of valid data into the system memory. The signal is LOW to write, and is in the high impedance state when viewdata is selected. The three-state buffer is enabled at the same time as the data outputs (see below). An internal pull-up device prevents the output from floating into the LOW state when the 3-state buffer is OFF.

16, 17, 18, **D7 to D1, Data outputs**

19, 20, 21, 22 These 3-state outputs are the seven bit parallel data outputs to the system memory. The outputs are enabled at the following times:—

a) During the data entry window (DEW) to write teletext data into the memory. The data rate is 867 kbytes per second and is derived from the teletext data clock.

b) During tv line 40 for encoded status information about user commands (e.g. programme number), to be written into the memory. This period is known as EDIL (encoded data insertion line). The data rate is 1 Mbyte per second and is derived from the 1 MHz display clock F1.

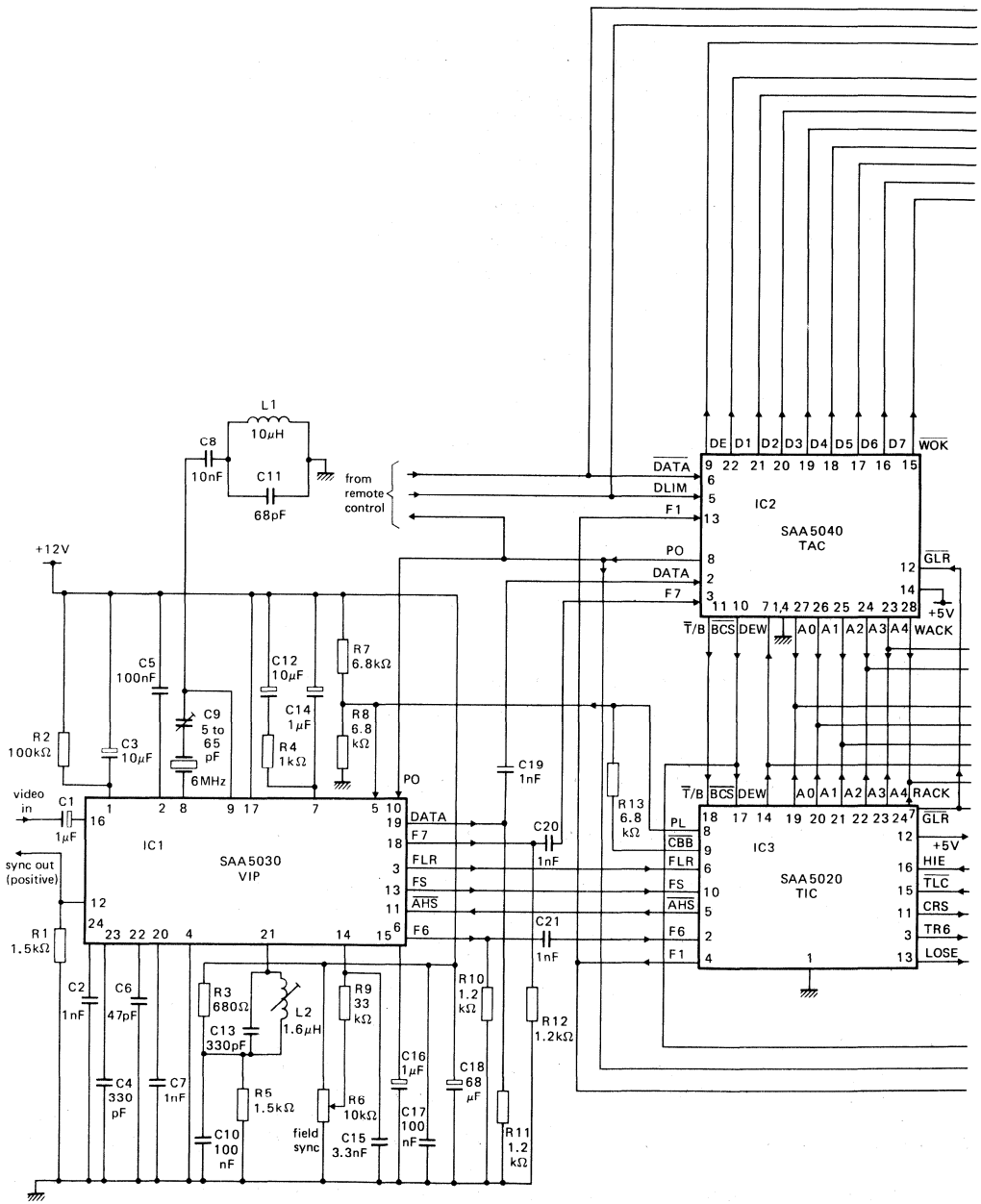
c) When the page is cleared. In this case the data output is forced to the space code (0100000) during the display period for one field. This data is held at the space code from either tv line 40 (if page clear is caused by user command), or the received teletext data line causing the clear function, until the start of the data entry window (DEW) of the next field.

23, 24, 25, **A4 to A0 Memory addresses**

26, 27 These 3-state outputs are the 5-bit row address to the page memory. This address specifies in which of 24 rows the teletext data is to be written. The outputs are enabled during the data entry period (DEW).

28. **WACK Write address clock**

This 3-state output is used to clock the memory address counter during the data entry period (DEW). The output is enabled only during this period. The positive-going edge of WACK is used to clock the address counter.


L1
10μH
C8
10nF
C11
68pF
from
remote
control
DATA
DLIM
F1
IC2
SAA5040
TAC
DE D1 D2 D3 D4 D5 D6 D7 WOK
PO
DATA
F7
GLR
+5V
T/B BCS DEW A0 A1 A2 A3 A4 WACK
+12V
C5
100nF
C12
10μF
R7
6.8kΩ
C9
5 to
65
pF
6MHz
C14
1μF
R4
1kΩ
R8
6.8
kΩ
R2
100kΩ
C3
10μF
C19
1nF
R13
6.8
kΩ
T/B BCS DEW A0 A1 A2 A3 A4 RACK
video
in
C1
1μF
IC1
SAA5030
VIP
DATA
F7
FLR
FS
AHS
F6
PO
C20
1nF
PL
CBB
FLR
FS
AHS
F6
F1
IC3
SAA5020
TIC
GLR
+5V
HIE
TLC
CRS
TR6
LOSE
sync out
(positive)
R1
1.5kΩ
C21
1nF
C2
1nF
C6
47pF
R3
680Ω
L2
1.6μH
C13
330pF
R9
33
kΩ
R10
1.2
kΩ
R12
1.2kΩ
C16
1μF
C18
68
μF
C4
330
pF
C7
1nF
R5
1.5kΩ
R6
10kΩ
C17
100
nF
C10
100
nF
field
sync
C15
3.3nF
R11
1.2
kΩ

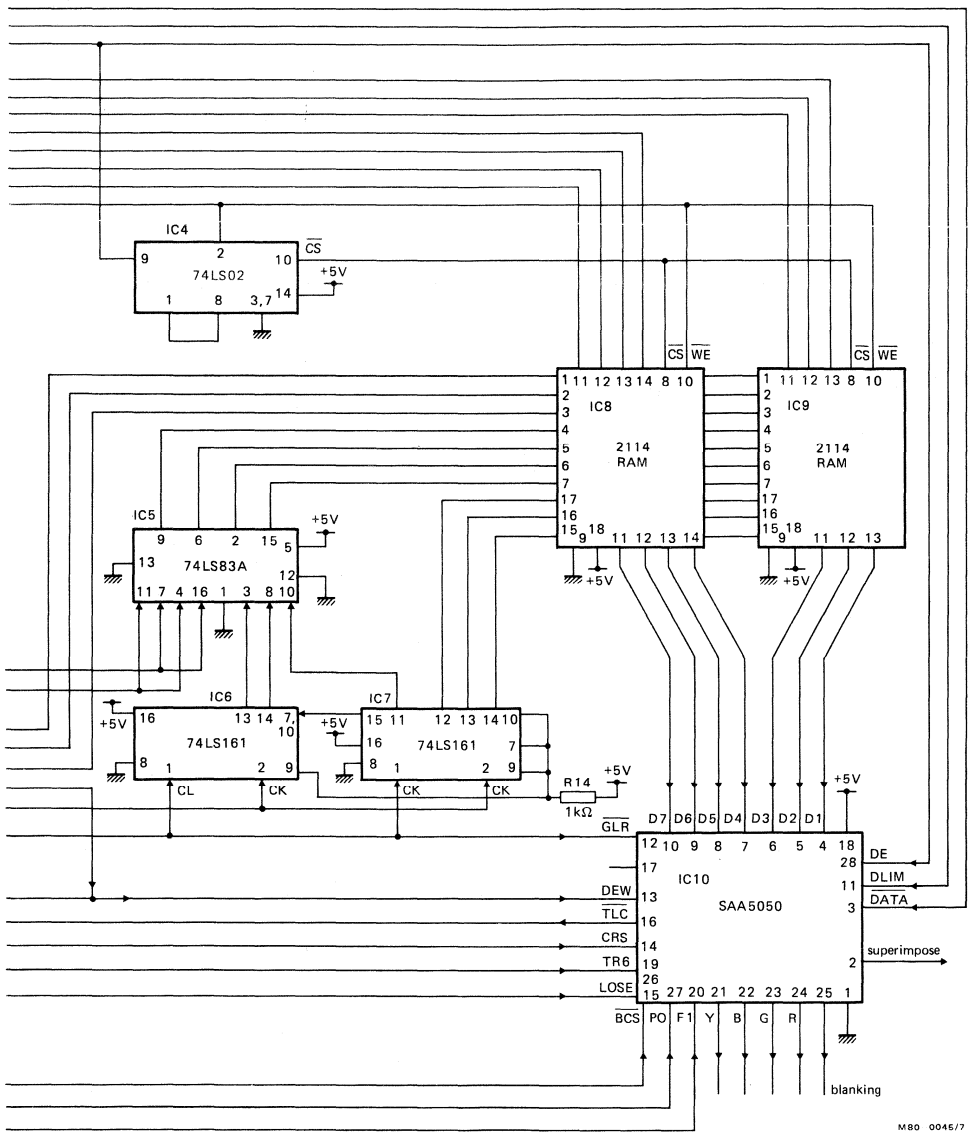


Fig.7 Typical circuit diagram of a teletext decoder.

TABLE 1 (Note 8)

Remote control commands used in the SAA5040A/SAA5040B/SAA5040C/SAA5043

CODE b_5	b_4	b_3	b_2	b_1	TELEVISION MODE ($b_7 = b_6 = 0$) (Note 7)	TELETEXT MODE ($b_7 = 1$, $b_6 = 0$) (Note 7)
0	0	0	0	0	RESET (Note 1)	
0	0	0	0	1		
0	0	0	1	0		
0	0	0	1	1	TV/ON Gives programme display.	
0	0	1	0	0	STATUS Gives programme display.	STATUS Programme/header display (Note 6)
0	0	1	0	1		HOLD Stops reception of teletext. (Note 9)
0	0	1	1	0		
0	0	1	1	1	TIME Gives time display.	DISPLAY CANCEL (Note 3)
0	1	0	0	0		
0	1	0	0	1		
0	1	0	1	0		
0	1	0	1	1		
0	1	1	0	0		TAPE Resets to small characters.
0	1	1	0	1		
0	1	1	1	0		TIMED PAGE OFF
0	1	1	1	1		TIMED PAGE ON
1	0	0	0	0	PROGRAMMES (Note 2)	NUMBERS (Notes 4 and 6) 1
1	0	0	0	1		2
1	0	0	1	0		3
1	0	0	1	1		4
1	0	1	0	0		5
1	0	1	0	1		6
1	0	1	1	0		7
1	0	1	1	1		8
1	1	0	0	0		9
1	1	0	0	1		0
1	1	0	1	0		SMALL CHARACTERS
1	1	0	1	1		LARGE CHARACTERS TOP HALF PAGE
1	1	1	0	0		LARGE CHARACTERS BOTTOM HALF PAGE
1	1	1	0	1		
1	1	1	1	0		SUPERIMPOSE (Note 6)
1	1	1	1	1		TELETEXT/ON (Note 5)

Notes for Table 1

1. Reset clears the page memory, sets page number to 100 and time code to 00.00 and resets timed page and display cancel modes.
2. Programme names are displayed for 5 s in a box at the top left of the screen in large characters. Programme commands clear the page memory except in timed page mode.

The following boxed information is displayed.

REMOTE CONTROL COMMAND b_5 b_4 b_3 b_2 b_1	SAA5040A	SAA5040B	SAA5040C	SAA5043
1 0 0 0 0	BBC1	Gives no status box	BBC1	Ch 1
1 0 0 0 1	BBC2		ITV	Ch 2
1 0 0 1 0	ITV		BBC2	Ch 3
1 0 0 1 1	4		BBC1	Ch 4
1 0 1 0 0	5		ITV	Ch 5
1 0 1 0 1	6		VTR	Ch 6
1 0 1 1 0	7		BBC1	Ch 7
1 0 1 1 1	VCR		ITV	Ch 8
1 1 0 0 0	9		BBC2	Ch 9
1 1 0 0 1	10		BBC1	Ch 0
1 1 0 1 0	11		ITV	Ch 10
1 1 0 1 1	12		VTR	Ch 11

3. Display cancel removes the text and restores the television picture. The device then reacts to any update indicator on the selected page. An updated newsflash or subtitle is displayed immediately. When an updated normal page arrives the page number only is displayed in a box at the top left of the screen. The full page of text can then be displayed when required using the teletext/on command.
4. Three number commands in sequence request a new page, and four number commands select a new time code in timed page mode. When a new page has been requested the page header turns green and the page numbers roll until the new page is captured.
5. The teletext/on command resets display cancel, hold and superimpose modes.
6. Status, timed page on, timed page off, numbers, superimpose and teletext/on commands all reset to top half page and produce a box round the header for 5 s. This allows the header to be seen if the television picture is on (e.g. newsflash or display cancel modes).
7. In viewdata mode ($b_7 = b_6 = 1$) the device is disabled and teletext cannot be received. All 3-state outputs are high impedance.
8. Table 1 shows code required for functions specified. The device requires the inverse of these codes i.e. $\overline{b_7}$ to $\overline{b_1}$. The code is transmitted serially in the following order: $\overline{b_7}$, $\overline{b_1}$, $\overline{b_2}$, $\overline{b_3}$, $\overline{b_4}$, $\overline{b_5}$, $\overline{b_6}$.
9. When hold node is selected 'HOLD' is displayed in green at the top right of the screen.
10. A 'P' is displayed before the page number at the top left of the screen (e.g. P123).

TABLE 2 (Note 9)

Remote control commands used in the SAA5041

CODE b_5 b_4 b_3 b_2 b_1	TELEVISION MODE ($b_7 = b_6 = 0$) (Note 8)	TELETEXT MODE ($b_7 = 1$, $b_6 = 0$) (Note 8)
0 0 0 0 0		
0 0 0 0 1		
0 0 0 1 0		
0 0 0 1 1		
0 0 1 0 0	TIME Gives time display.	STATUS Gives header and time display. (Note 6)
0 0 1 0 1		TIMED PAGE On/off toggle function.
0 0 1 1 0		
0 0 1 1 1		
0 1 0 0 0		
0 1 0 0 1		
0 1 0 1 0		
0 1 0 1 1		
0 1 1 0 0		
0 1 1 0 1		
0 1 1 1 0		
0 1 1 1 1		TELETEXT RESET (Note 1)
1 0 0 0 0		0
1 0 0 0 1		1
1 0 0 1 0		2
1 0 0 1 1		3
1 0 0 0 0		4
1 0 1 0 1	PROGRAMMES (Note 10)	NUMBERS 5
1 0 1 1 0		(Notes 2 and 7) 6
1 0 1 1 1		7
1 1 0 0 0		8
1 1 0 0 1		9
1 1 0 1 0		SMALL CHARACTERS
1 1 0 1 1		LARGE CHARACTERS Top/bottom toggle function
1 1 1 0 0		HOLD Stops reception of teletext - toggle function (Note 3)
1 1 1 0 1		DISPLAY CANCEL (Note 4)
1 1 1 1 0		SUPERIMPOSE
1 1 1 1 1		NORMAL DISPLAY (Note 5)

Notes for Table 2

1. The teletext reset command clears the page memory, selects Page 100, goes to small characters and resets hold, timed page and display cancel modes.

2. Three number commands in sequence request a new page, and four number commands select a new time code in timed page mode. When a new page has been requested the page header turns green and the page numbers roll until the new page is captured.

3. When hold mode is selected 'HALT' is displayed in green at the top right of the screen.

4. Display cancel removes the text and restores the television picture. The SAA5041 then reacts to any update indicator on the selected page. An updated newsflash or subtitle is displayed immediately. When an updated normal page arrives the page number only is displayed in a box at the top left of the screen. The full page of text can then be displayed when required using the normal display command.

5. The normal display command resets display cancel, hold and superimpose modes.

6. Status, timed page, numbers, hold, superimpose and normal display commands all reset to top half page and produce a box round the header for five seconds. This allows the header to be seen even if the television picture is on (e.g. newsflash or display cancel modes).

7. An 'S' is displayed before the page number at the top left of the screen (e.g. S123).

8. In viewdata mode ($b_7 = b_6 = 1$) the SAA5041 is disabled and teletext cannot be received. All 3-state outputs are high impedance.

9. Table 2 shows code required for functions specified. The SAA5041 requires the inverse of these codes i.e. b_7 to b_1. The code is transmitted serially in the following order: $\overline{b_7}$, $\overline{b_1}$, $\overline{b_2}$, $\overline{b_3}$, $\overline{b_4}$, $\overline{b_5}$, $\overline{b_6}$.

10. Clear Memory occurs except in Timed Page Mode.

TABLE 3 (Note 9)

Remote control commands used in the SAA5042

CODE b_5	b_4	b_3	b_2	b_1	TELEVISION MODE ($b_7 = b_6 = 0$) (Note 8)	TELETEXT MODE ($b_7 = 1$, $b_6 = 0$) (Note 8)
0	0	0	0	0	RESET (Note 1)	
0	0	0	0	1		
0	0	0	1	0		
0	0	0	1	1		
0	0	1	0	0		STATUS Gives header and time display. (Note 6)
0	0	1	0	1		HOLD Stops reception of teletext - toggle function (Note 3)
0	0	1	1	0		
0	0	1	1	1	TIME Gives time display	
0	1	0	0	0		
0	1	0	0	1		
0	1	0	1	0		SMALL CHARACTERS
0	1	0	1	1		
0	1	1	0	0		LARGE CHARACTERS TOP HALF PAGE
0	1	1	0	1		LARGE CHARACTERS BOTTOM HALF PAGE
0	1	1	1	0		DISPLAY CANCEL/RECALL (Note 4)
0	1	1	1	1		DISPLAY RECALL
1	0	0	0	0		0
1	0	0	0	1		1
1	0	0	1	0		2
1	0	0	1	1		3
1	0	1	0	0		4
1	0	1	0	1	PROGRAMMES (Note 10)	NUMBERS 5
1	0	1	1	0		(Notes 2 and 7) 6
1	0	1	1	1		7
1	1	0	0	0		8
1	1	0	0	1		9
1	1	0	1	0		TIMED PAGE On/Off toggle function
1	1	0	1	1		CLEAR MEMORY
1	1	1	0	0		LONG TERM STORE/SMALL CHARACTERS
1	1	1	0	1		
1	1	1	1	0		SUPERIMPOSE
1	1	1	1	1		TELETEXT/ON (Note 5)

Notes for Table 3

1. Reset clears the page memory, sets page number to 100 and time code to 00.00 and resets timed page and display cancel modes.

2. Three number commands in sequence request a new page, and four number commands select a new time code in timed page mode. When a new page has been requested the page header turns green and the page numbers roll until the new page is captured.

3. When hold mode is selected 'STOP' is displayed in green at the top right of the screen.

4. Display cancel/recall removes the text and restores the television picture. The SAA5042 then reacts to any update indicator on the selected page. An updated newsflash or subtitle is displayed immediately. When an updated normal page arrives the page number only is displayed in a box at the top left of the screen. The same command will then cause a normal page to be displayed, but will cancel a newsflash or subtitle page. Alternatively, text can be recalled by using the teletext/on command.

5. The teletext/on command resets display cancel, hold and superimpose modes.

6. Status, timed page, numbers, superimpose and teletext/on commands all reset to top half page and produce a box round the header for five seconds. This allows the header to be seen even if the television picture is on (e.g. newsflash or display cancel modes).

7. A 'P' is displayed before the page number at the top left of the screen (e.g. P123).

8. In viewdata mode ($b_7 = b_6 = 1$) the SAA5042 is disabled and teletext cannot be received. All 3-state outputs are high impedance.

9. Table 3 shows code required for functions specified. The SAA5042 requires the inverse of these codes i.e. $\overline{b}_7$ to $\overline{b}_1$. The code is transmitted serially in the following order: $\overline{b}_7$, $\overline{b}_1$, $\overline{b}_2$, $\overline{b}_3$, $\overline{b}_4$, $\overline{b}_5$, $\overline{b}_6$.

10. Clear Memory occurs except in Timed Page Mode.

GEARING AND ADDRESS LOGIC ARRAY FOR USA TELETEXT (GALA)

GENERAL DESCRIPTION

The SAA5045 is a PCF0700 CMOS process gate array designed to interface the SAA5040B Teletext Acquisition Control (TAC) IC to the SAA5030 Video Processor (VIP) data output for modified U.K. standard 525-line Teletext. It also provides an address interface between SAA5040B, SAA5025D Teletext Timing Chain for USA 525 line system (USTIC) and the page memory RAM. The memory interface includes read/write control compatible with the geared 32 + 8 transmission system at 5,727272 MHz data rate employed in the modified U.K. system.

For RATINGS and CHARACTERISTICS see data sheet: CMOS GATE ARRAYS (PCF0700).

SYSTEM CONTENT

Functionally the chip contains two main sections which operate during the acquisition and display periods.

Gearing control section

The data from the SAA5030 (VIP) and data clock, are processed to detect the presence of the gearing bit and convert the data for correct operation of the SAA5040B (TAC). Data and clock outputs to the TAC are internally compensated for processing delays, so that correct clocking-in of data is ensured.

Addressing section

Column counters are included, which operate from the WACK (TAC) and RACK (USTIC) column clock signals during acquisition and display respectively.

Five row-address input circuits (pins A0 to A4) are provided for (TAC) and (USTIC) address outputs. These are multiplexed with the column address from the internal counters for correct mapping of the RAM via ten output address pins (AA0 to AA9). During acquisition, the multiplexer is controlled by the gearing bit detection to give correct assembly of the 40 character per row page structure.

The address output buffers are 3-state devices controlled by the line reset signal (pin 8; $\overline{\text{GLRS}}$). During the horizontal flyback period the address pins are 3-state to allow alternative addressing for customized applications.

Read/write control to RAM

An internal counter prevents overwriting if more than 32 character WOK pulses are received from TAC due to poor transmission conditions. Two control outputs, one for read/write ($\overline{\text{WE}}$) and the other for chip select ($\overline{\text{CS}}$), are provided to eliminate conflicts on the input/output RAM bus.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117D).

SYSTEM CURRENT (continued)

Framing code detection

When a valid data line is received and the framing code is detected in the gearing section, then flag pulses (pair of pulses) are available at output $\overline{WE}$, before the $\overline{CS}$ output is driven LOW for normal writting into the RAM. If a framing-code-present signal is required, it can be obtained by gating $\overline{WE}$ and $\overline{CS}$ outputs such, that an output from the $\overline{WE}$, when output $\overline{CS}$ is HIGH, indicates the detection of a framing code; N.B., each framing code produces a pair of pulses.

RAM ADDRESS CONTROL

Figure 2 shows that the ten RAM address outputs are controlled by a multiplexer (MUX3), which interchanges the two groups of five address lines, when a gearing bit equal to logic "1" is received during data input. During display, MUX3 is switched by bit number 6 of the column counter. MUX1, which is switched by the gearing bit, controls stepping of the row address when fill-in rows are received. MUX2 is switched by either the gearing bit or bit 6 of the column counter to access the part of RAM storing the last eight bytes of each row of data.

The mapping of the 1024-byte RAM is shown in Fig. 1. Area "A" stores data corresponding to the left-hand side (32 bytes wide) of the display whilst area "B" stores the remainder for the right-hand side.

Access to the RAM for custom operations can be made during the time that $\overline{GLRS}$ (pin 8) is LOW, which causes all ten address buffers to be in the open state. It should be noted that $\overline{GLRS}$ LOW also resets the column counters and the gearing-bit detection system to logic "0". This normally occurs during the horizontal interval (between 5 and 8 μs) after the horizontal sync pulse falling edge.

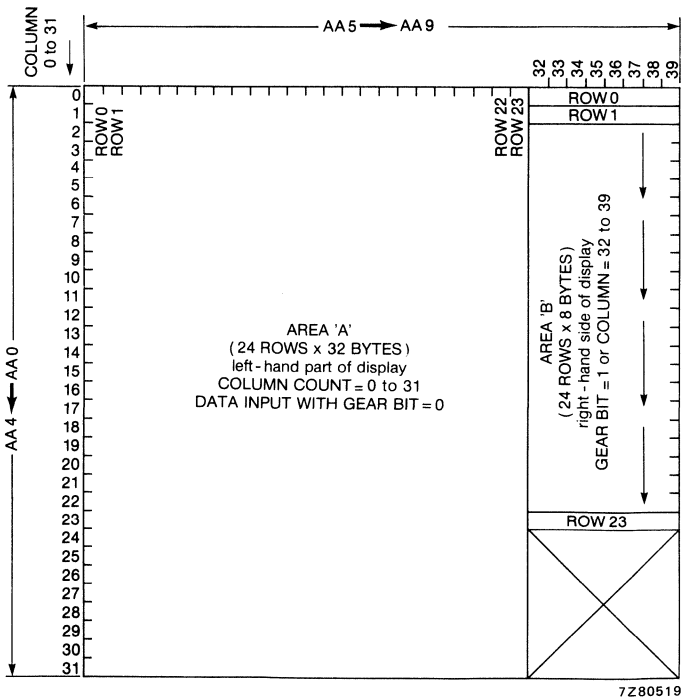


Fig. 1 Memory map for the SAA5045 address system.

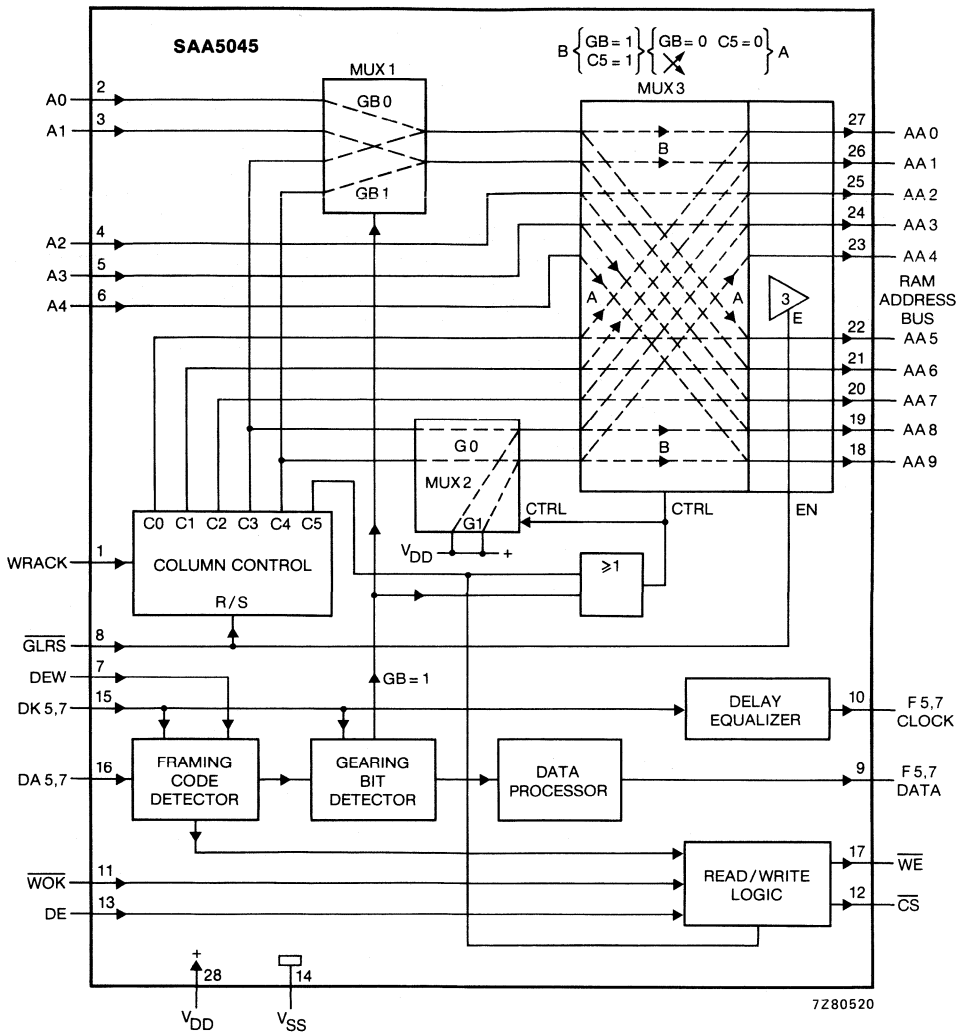


Fig. 2 Block diagram.

PIN DESCRIPTION

pin no.	symbol	name and function
1	WRACK	input clock to column counter
2	A0	row address system inputs
3	A1	
4	A2	
5	A3	
6	A4	
7	DEW	data entry window input
8	$\overline{\text{GLRS}}$	general line reset starting output
9	F5,7 DATA	5,7 MHz data output
10	F5,7 CLOCK	5,7 MHz clock output
11	$\overline{\text{WOK}}$	write enable input
12	$\overline{\text{CS}}$	chip select output
13	DE	display enable input
14	V_{SS}	ground
15	DK5,7	5,7 MHz data clock input
16	DA5,7	5,7 MHz data input
17	$\overline{\text{WE}}$	write enable output
18	AA9	memory address outputs
19	AA8	
20	AA7	
21	AA6	
22	AA5	
23	AA4	
24	AA3	
25	AA2	
26	AA1	
27	AA0	
28	V_{DD}	positive supply (+ 4,5 V to + 5,5 V)

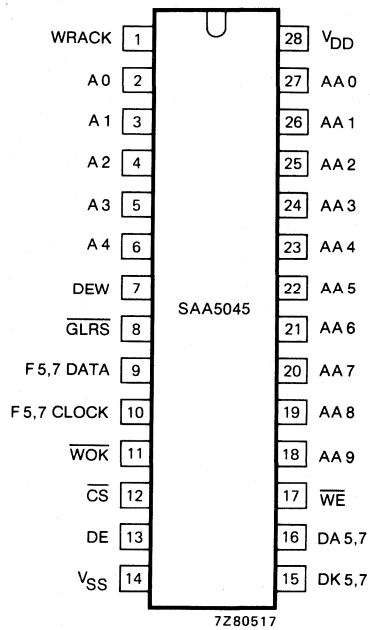


Fig. 3 Pin configuration.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. WRACK – input clock to column counter

Input clock to column counter during data input or display; WACK from SAA5040B (TAC) or RACK from SAA5025D (USTIC).

2 to 6. A0 to A4 – row address system inputs

Inputs to row address system during data input or display. Row address numbers greater than 0 to 23 disable writing to the RAM during input.

7. DEW – data entry window input

Data entry window input enables gearing bit detection and data processing part of system.

8. $\overline{\text{GLRS}}$ – general line reset starting output

Input from the SAA5025D is a negative reset pulse at line rate for column counters and gearing system. When this input is LOW, it opens 3-state address buffers.

9. F5,7 DATA – 5,7 MHz data output

Data output at 5,7 MHz rate to SAA5040B (TAC) during the data acquisition period when DEW is HIGH.

10. F5,7 CLOCK – 5,7 MHz clock output

Data clock output at 5,7 MHz rate to SAA5040B (TAC), synchronized to data at pin 9 (F5,7 DATA).

11. $\overline{\text{WOK}}$ – write enable input

Write enable input from SAA5040B (TAC) during data acquisition, when correct data is received, for RAM write/read control (via output $\overline{\text{WE}}$; pin 17).

12. $\overline{\text{CS}}$ – chip select output

Output to drive the RAM chip enable during data input and display periods controlled by the display enable output (DE) and write O.K. ($\overline{\text{WOK}}$) output of the SAA5040B (TAC), avoiding input/output bus conflict.

13. DE – display enable input

Display enable input from SAA5040B (TAC) to control $\overline{\text{CS}}$.

14. V_{SS} – ground

15. DK5,7 – 5,7 MHz data clock input

Data clock input at 5,7 MHz rate from the SAA5030 (VIP); this pin is capacitively coupled with a d.c. restoring diode and is externally connected to V_{SS}.

16. DA5,7 – 5,7 MHz data input

Data input at 5,7 MHz rate from SAA5030 (VIP); this pin is capacitively coupled with a d.c. restoring diode and is externally connected to V_{SS}.

17. $\overline{\text{WE}}$ – write enable output

Write enable output to control RAM write/read. This output is the gated and delay version of the $\overline{\text{WOK}}$ from the SAA5040B, but limited to 32 pulses which are possible before the WACK count is equal to 32.
A pair of pulses on this output precedes the $\overline{\text{WOK}}$ pulses, whilst $\overline{\text{CS}}$ is HIGH whenever a framing code is detected.

APPLICATION INFORMATION (continued)

18 to 27. AA9 to AA0 – memory address outputs

Memory address outputs; 3-state buffered outputs, open when $\overline{GLRS}$ is LOW for auxiliary access to the RAM address bus if required.

N.B.: AA9 and AA8 are simultaneously HIGH whenever a gear bit with logic "1" is received during DEW is HIGH. This enables detection of gearing bit reception, following $\overline{GLRS}$ reset on each line, which always resets AA0 to AA9 to logic "0".

28. V_{DD} – positive supply (4,5 V to 5,5 V)

Note

Input pins other than 15 and 16 have internal 15 kΩ pull-up resistors for compatibility with SAA5025D and SAA5040B output signal ranges. Pins 15 and 16 are CMOS inputs for d.c. restored drive from the SAA5030 (VIP) clock and data output signals.

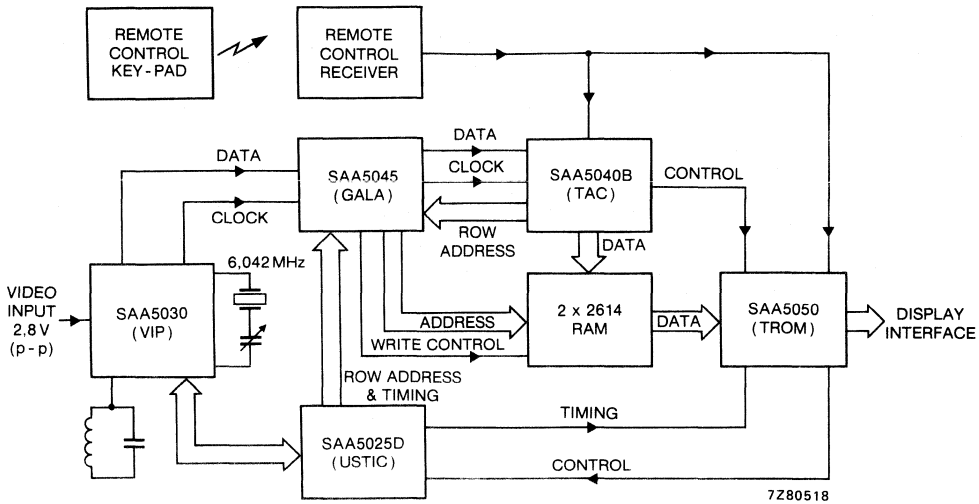


Fig. 4 Schematic diagram of the 5-chip decoder.

TELETEXT CHARACTER GENERATOR

The SAA5050 series of MOS N-channel integrated circuits provides the video drive signals to the television receiver necessary to produce the teletext/viewdata display. The variants are described in the Quick Reference Data and full details of the characters sets are given in Figs. 11 to 18.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	85	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

Variant	Character set	Variant	Character set
5050	English	5054	Belgian
5051	German	5055	US ASCII
5052	Swedish	5056	Hebrew
5053	Italian	5057	Cyrillic

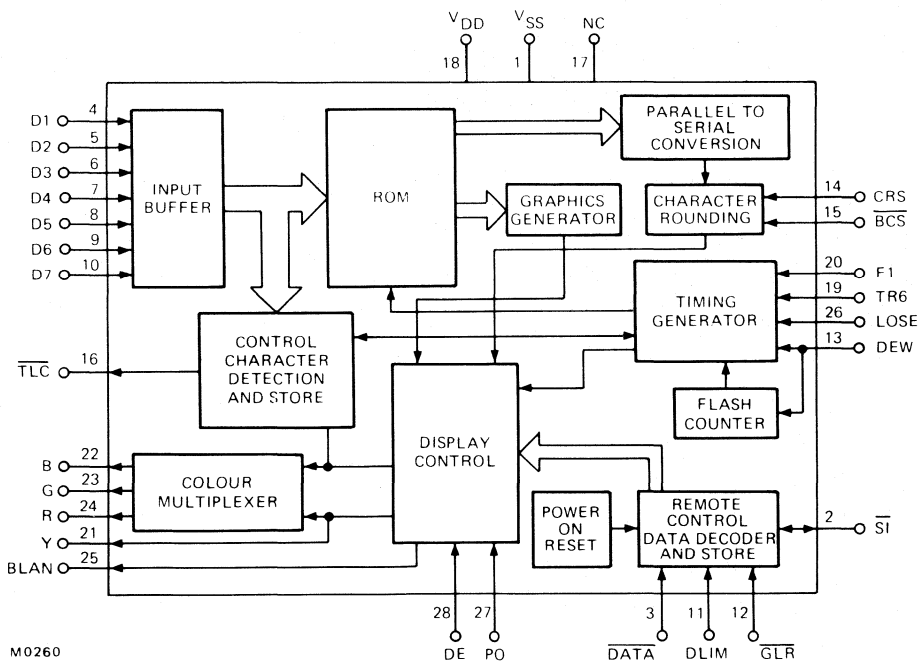


Fig.1 Block diagram

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

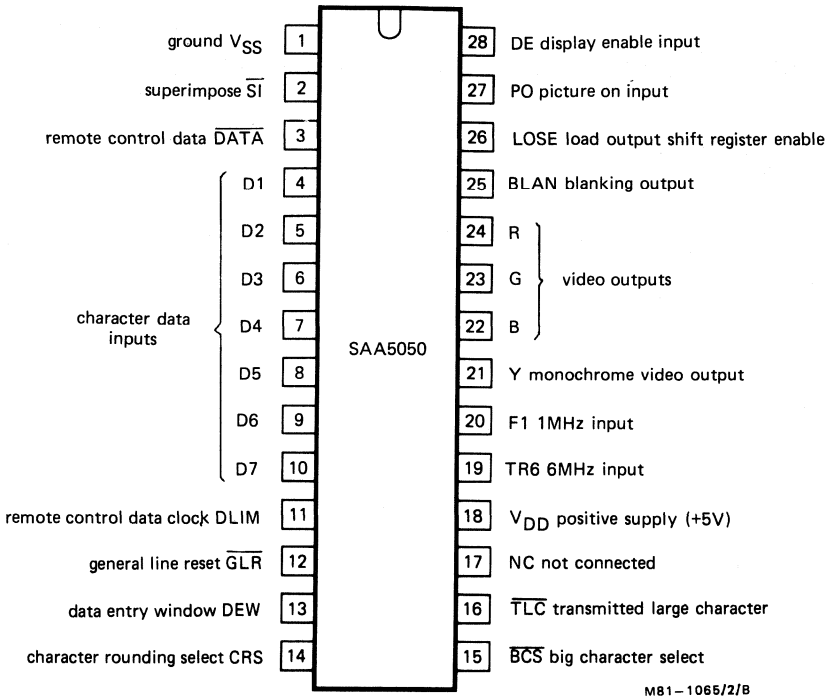


Fig.2 Pinning diagram

DESCRIPTION

The SAA5050 is a 28 pin device which incorporates a fast access character generator ROM (4.3 k bits), the logic decoding for all the teletext control characters and decoding for some of the remote control functions. The circuit generates 96 alphanumeric and 64 graphic characters. In addition there are 32 control characters which determine the nature of the display.

The SAA5050 is suitable for direct connection to the SAA5010, SAA5012, SAA5020 and SAA5040 Series integrated circuits.

The basic input to the SAA5050 is the character data from the teletext page memory. This is a 7 bit code. Each character code defines a dot matrix pattern. The character period is 1 μs and the character dot rate is 6 MHz. The timings are derived from the two external input clocks F1 (1 MHz) and TR6 (6 MHz) which are amplified and re-synchronised internally. Each character rectangle is 6 dots wide by 10 TV lines high. One dot space is left between adjacent characters, and there is one line space left between rows. Alphanumeric characters are generated on a 5 x 9 matrix, allowing space for descending characters. Each of the 64 graphic characters is decoded to form a 2 x 3 block arrangement which occupies the complete 6 x 10 dot matrix (Fig.9). Graphics characters may be either contiguous or separated (Fig.10). The alphanumeric characters are character rounded, i.e. a half dot is inserted before or after a whole dot in the presence of a diagonal in a character matrix.

The character video output signals comprise a monochrome signal and RGB signals for a colour receiver. A blanking output signal is provided to blank out the television video signal under the control of the PO and DE inputs and the box control characters (see Table 3).

The monochrome data signal can be used to inlay characters into the television video. The use of the 32 control characters provides information on the nature of the display, e.g. colour. These are also used to provide other facilities such as 'concealed display' and flashing words etc. The full character set is given in Table 1.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (See 'Handling MOS Devices').

RATINGS Limiting values in accordance with the Absolute Maximum System, (IEC134)

		min.	typ.	max.	
Voltages (with respect to pin 1)					
Supply voltage (pin 18)	V_{DD}	−0.3	–	7.5	V
Input voltages (all inputs + input/output)	V_I	−0.3	–	7.5	V
Output voltage (pin 16)	V_{O16}	−0.3	–	7.5	V
(all other outputs)	V_O	−0.3	–	14.0	V
Temperature					
Storage temperature range	T_{stg}		−20 to +125		°C
Operating ambient temperature range	T_{amb}		−20 to +70		°C

CHARACTERISTICS

		min.	typ.	max.	
Supply voltage (pin 18)	V_{DD}	4.5	–	5.5	V
The following parameters apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.					
Supply current	I_{DD}	–	85	160	mA
Inputs					
Character data D1 to D7 (pins 4 to 10)					
Input voltage; HIGH	V_{IH}	2.65	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Clock inputs F1 (pin 20) **TR6** (pin 19)					
Input voltage; HIGH	V_{IH}	2.65	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Logic inputs					
$\overline{\text{DATA}}$ (pin 3) DEW (pin 13) LOSE (pin 26) DLIM (pin 11) CRS (pin 14) PO (pin 27) $\overline{\text{GLR}}$ (pin 12) $\overline{\text{BCS}}$ (pin 15) DE (pin 28)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
All inputs					
Input leakage current (V_I = 5.5 V)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

			min.	typ.	max.	
Outputs						
Character video outputs + Blanking output (open drain) (note 3)						
B – (pin 22), G – (pin 23), R – (pin 24), Y – (pin 21), Blanking (pin 25)						
Output voltage; LOW (I_{OL} = 2 mA)		V_{OL}	–	–	0.5	V
Output voltage; LOW (I_{OL} = 4 mA)		V_{OL}	–	–	1.0	V
Output voltage; HIGH (note 5)		V_{OH}	V_{DD}	–	13.2	V
Output load capacitance		C_L	–	–	15	pF
Output fall time	note 1	t_f	–	–	30	ns
Variation of fall time between any outputs	note 1	Δt_f	0	–	20	ns
$\overline{\text{TLC}}$ (pin 16)						
Output voltage; LOW (I_{OL} = 100 μA)		V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)		V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		C_L	–	–	30	pF
Output rise time	Measured between 0.8 V and 2.0 V levels	t_r	–	–	1.0	μs
Output fall time	Measured between 0.8 V and 2.0 V levels	t_f	–	–	1.0	μs
Input/output						
$\overline{\text{SI}}$ (pin 2) (open drain)						
Input voltage; HIGH		V_{IH}	2.0	–	6.5	V
Input voltage; LOW		V_{IL}	0	–	0.8	V
Input leakage current (V_I = 5.5 V)		I_{IR}	–	–	10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 0.4 mA)		V_{OL}	0	–	0.5	V
Output voltage; LOW (I_{OL} = 1.3 mA)		V_{OL}	0	–	1.0	V
Output load capacitance		C_L	–	–	45	pF
Output voltage; HIGH state (note 2)		V_{OH}	–	–	6.5	V

Timing characteristics

For typical display of 40 characters per line. Line rate = 64 μs. Field rate = 20 ms.

Character data timing (Fig.4)

		min.	typ.	max.	
TR6 rising edge to F1 falling edge	t_D	6	–	60	ns
TR6 frequency	f_{TR6}	–	6	–	MHz
TR6 mark/space ratio		40:60	–	60:40	
F1 frequency	f_{F1}	–	1	–	MHz
F1 mark/space ratio		40:60	–	60:40	
Data set-up time	t_{CDS}	80	–	–	ns
Data hold time	t_{CDH}	100	–	–	ns
Delay time – character in/ character data at outputs Graphics	t_{CDG}	–	2.6	–	μs
Delay time – character in/ character data at outputs Alphanumerics	t_{CDA}	–	2.767	–	μs

Display period timing (Fig.5)

F1 falling edge to LOSE rising edge	t_{LDH}	0	–	250	ns
F1 falling edge to LOSE falling edge	t_{LDL}	0	–	250	ns
LOSE rising edge to 'Display on'	t_{DON}	–	2.6	–	μs
LOSE falling edge to 'Display off'	t_{DOFF}	–	2.6	–	μs
'Display period'	t_{DP}	–	40	–	μs

Line rate timing (Fig.6)

F1 rising edge to GLR falling edge	t_{DGL}	0	–	200	ns
F1 rising edge to GLR rising edge	t_{DGH}	0	–	200	ns
GLR LOW time	t_{GLP}	–	1	–	μs
Line start* to GLR falling edge	t_{GLR}	–	5	–	μs
Line start* to LOSE rising edge	t_{LSL}	–	14.5	–	μs
LOSE falling edge to Line start*	t_{LLS}	–	9.5	–	μs
Line period	t_{LNP}	–	64	–	μs
LOSE HIGH time	t_{LHP}	–	40	–	μs

Remote data input timing (Fig.8)

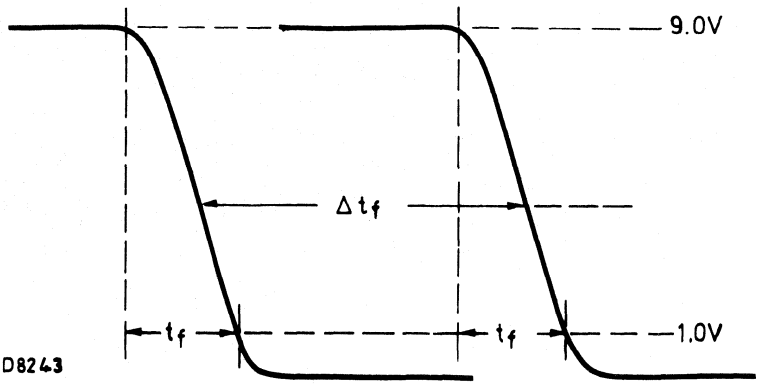
Assuming F1 period = 1 μs and GLR period = 64 μs

DLIM clock HIGH time	t_{CH}	6.5	8	(note 4)	μs
$\overline{\text{DLIM}}$ clock LOW time	t_{CL}	3.5	8	60	μs
DATA to $\overline{\text{DLIM}}$ set-up time	t_{DS}	0	14	–	μs
$\overline{\text{DLIM}}$ to $\overline{\text{DATA}}$ hold time	t_{DH}	8	14	–	μs

*Taken as falling edge of 'line sync' pulse.

Notes to characteristics

1. Fall time, t_f and Δt_f, are defined as shown and are measured using the circuit shown below:
   t_f is measured between the 9 V and 1 V levels.
   Δt_f is the maximum time difference between outputs.



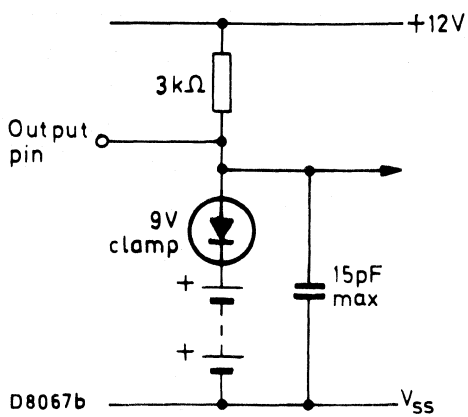


Fig.3

2. Recommended pull-up resistor for $\overline{SI}$ is 18 kΩ.
3. The R, G, B, Y and blanking outputs are protected against short circuit to supply rails.
4. There is no maximum DLIM cycle time, provided the DLIM duty cycle is such that the $t_{CL\,max}$ requirement is not exceeded.
5. With maximum pull-up voltage applied to R, G, B and BLAN outputs the leakage current will not exceed 20 μA with the outputs in the OFF state.

SPECIAL FEATURES

Flash oscillator

The circuit generates a 0.75 Hz signal with a 3:1 ON/OFF ratio to provide the flashing character facility.

Power-on-reset

When the supply voltage is switched on, the character generator will reset to tv, conceal, and not superimpose modes.

Character rounding

The character rounding function is different for the small and double height characters. In both cases the ROM is accessed twice during the character period of 1 μs. The dot information of two rows is then compared to detect the presence of any diagonal in the character matrix and to determine the positioning of the character rounding half dots.
For small characters rounding is always referenced in the same direction (i.e. row before in even fields and row after in odd fields as determined by the CRS signal).
For double height characters rounding is always referenced alternately up and down changing every line using an internally generated signal. (The CRS signal is '0' for the odd field and '1' for the even field of an interlaced tv picture).

Graphics decoder

The 64 graphics characters are decoded directly from the character data inputs and they appear on a 2 x 3 matrix. Figure 9 gives details of the graphics decoding.

APPLICATION DATA

The function is quoted against the corresponding pin numbers

Pin No.

1. V_{SS} **Ground** - 0 V

2. $\overline{\text{SI}}$ **Superimpose**

   This is a dual purpose input/output pin. The output is an open drain transistor (capable of sinking current to V_{SS}), which is in the conducting state when superimpose mode is selected. This allows contrast reduction of the tv picture in superimpose mode if required. If the pin is held LOW, the internal 'tv mode' flip-flop is held in the 'text' state. This is for VDU applications when the remote control is not used.

3. $\overline{\text{DATA}}$ **Remote control data**

   This input accepts a 7-bit serial data stream from the remote control decoder. This data contains the teletext and viewdata remote control functions. The nominal data rate is 32 μs/bit. The command codes used in the SAA5050 are shown in Table 2.

4,5,6 7,8,9, 10 **D1 to D7 Character data**

These inputs accept a 7-bit parallel data code from the page memory. This data selects the alphanumeric characters, the graphics characters and the control characters. The alphanumeric addresses are ROM column addresses, the graphics and control data are decoded internally.

11. **DLIM**

    This input receives a clock signal from the remote control decoder and this signal is used to clock remote control data into the SAA5050. The positive-going edge of every second clock pulse is nominally in the centre of each remote control data bit (Fig.8).

12 **GLR General line reset**

This input signal from the SAA5020 Timing Chain is required for internal synchronisation of remote control data signals.

13. **DEW Data entry window**

    This input signal from the SAA5020 Timing Chain is required to reset the internal ROM row address counter prior to the display period. It is also used internally to derive the 'flash' period.

APPLICATION DATA (continued)

14. **CRS Character rounding select**

This input signal from the SAA5020 Timing Chain is required for correct character rounding of displayed characters. (Normal height characters only).

15. **$\overline{\text{BCS}}$ Big character select**

This input from the SAA5040 Teletext Acquisition and Control device allows selection of large characters by remote control.

16. **$\overline{\text{TLC}}$ Transmitted large characters**

This output to the SAA5020 Timing Chain enables double height characters to be displayed as a result of control characters stored in the page memory.

18. **V_{DD} + 5 V supply**

This is the power supply input to the circuit.

19. **TR6**

This input is a 6 MHz signal from the SAA5020 Timing Chain used as a character dot rate clock.

20. **F1**

This input is a 1 MHz equal mark/space ratio signal from the SAA5020 Timing Chain. It is used to latch the 7-bit parallel character data into the input latches. It is also used to synchronise an internal divide-by 6 counter. The F1 signal is internally synchronised with TR6.

21. **Y Output**

This is a video output signal which is active in the HIGH state containing character dot information for tv display.
The output is an open drain transistor capable of sinking current to V_{SS}

22,23, 24. **B,G,R outputs**

These are the Blue, Green and Red Character video outputs to the tv display circuits. They are active HIGH and contain both character and background colour information.
The outputs are open drain transistors capable of sinking current to V_{SS}.

25. **BLAN Blanking**

This active HIGH output signal provides tv picture video blanking. It is active for the duration of a box when Picture On and Display Enable are HIGH. It is also activated permanently for normal teletext display when no tv picture is required (PO LOW). The output is an open drain transistor capable of sinking current to V_{SS}. Full details given in Table 3.

26. **LOSE Load output shift register enable**

This input signal from the SAA5020 Timing Chain resets the internal control character flip-flops prior to the start of each display line.
This signal also defines the character display period.

27. **PO Picture On**

This input signal from the SAA5040 Teletext Acquisition and Control device is used to control the character video and blanking outputs. When PO is HIGH, only text in boxes is displayed unless in superimpose mode. The input is HIGH for tv picture video on, LOW for picture off. See Table 3.

28. **DE Display enable**

This input signal from the SAA5040 Teletext Acquisition and Control device is used to enable the teletext display. The input is HIGH for teletext display enabled. LOW for display cancelled. See Table 3.

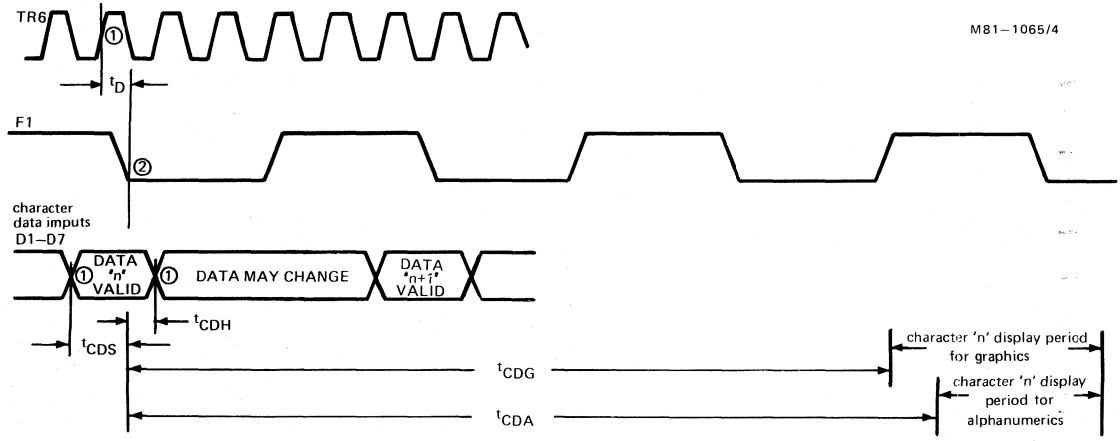


Fig.4 Character data timing (for typical 40 character display)

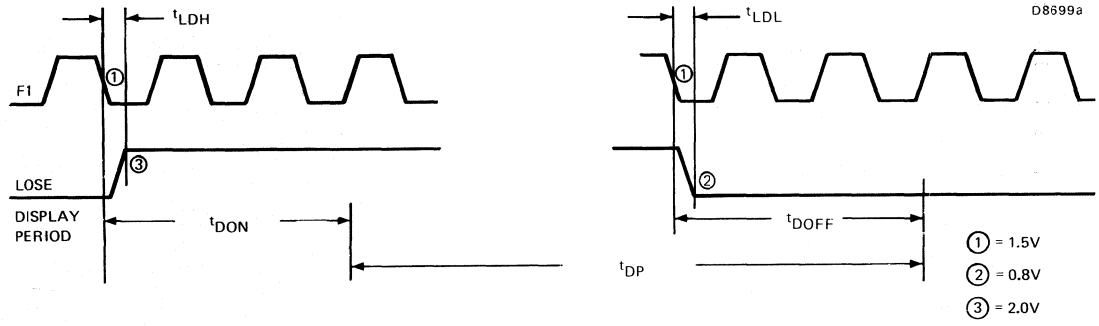


Fig.5 Display period timing (for typical 40 character display)

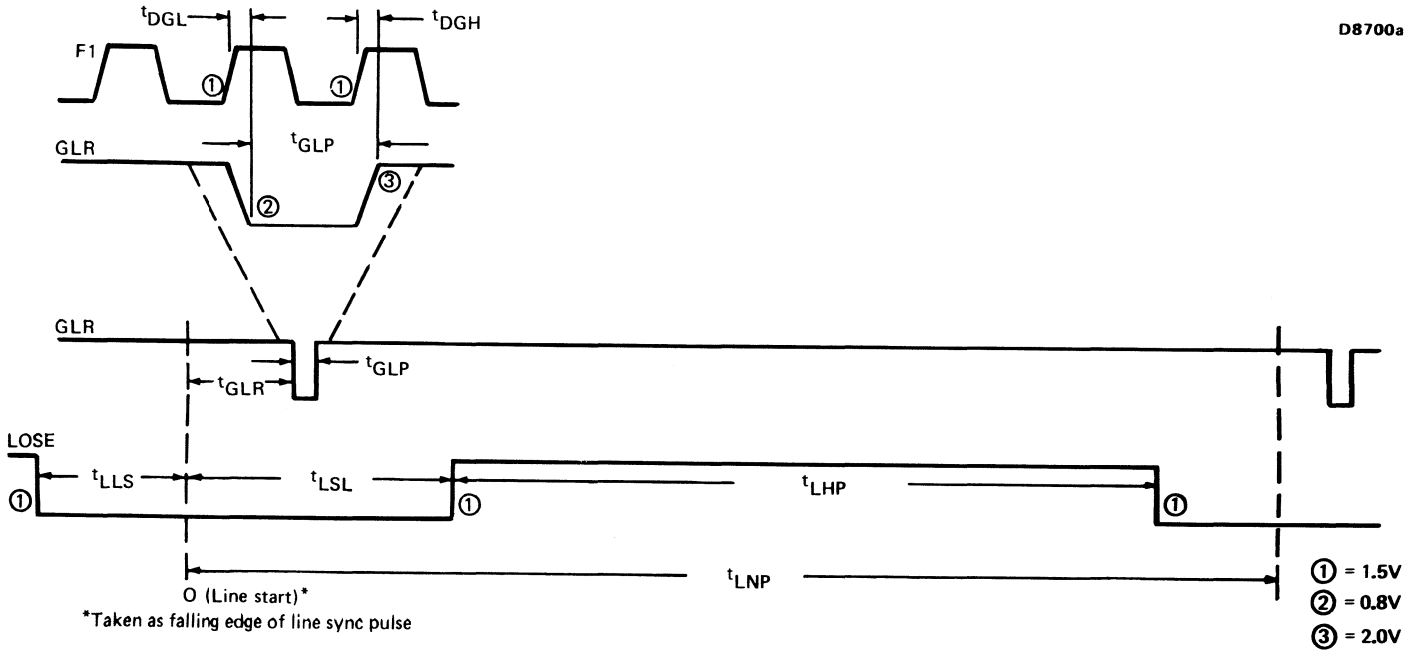


Fig.6 Line rate clocks (for line period of 64 μs)

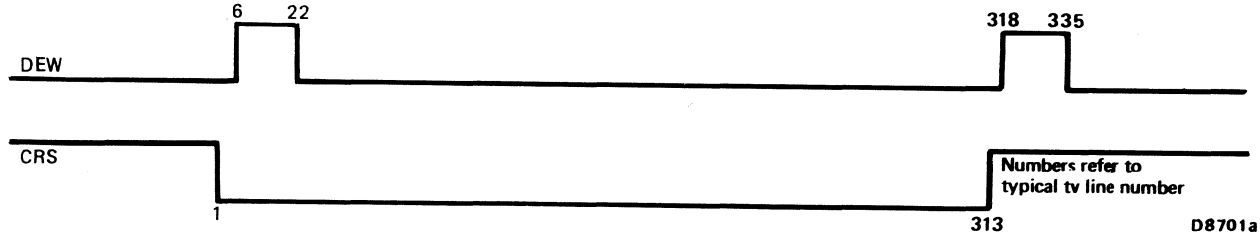


Fig.7 Field rate clocks (for field period of 20 ms, 312½ lines per field)

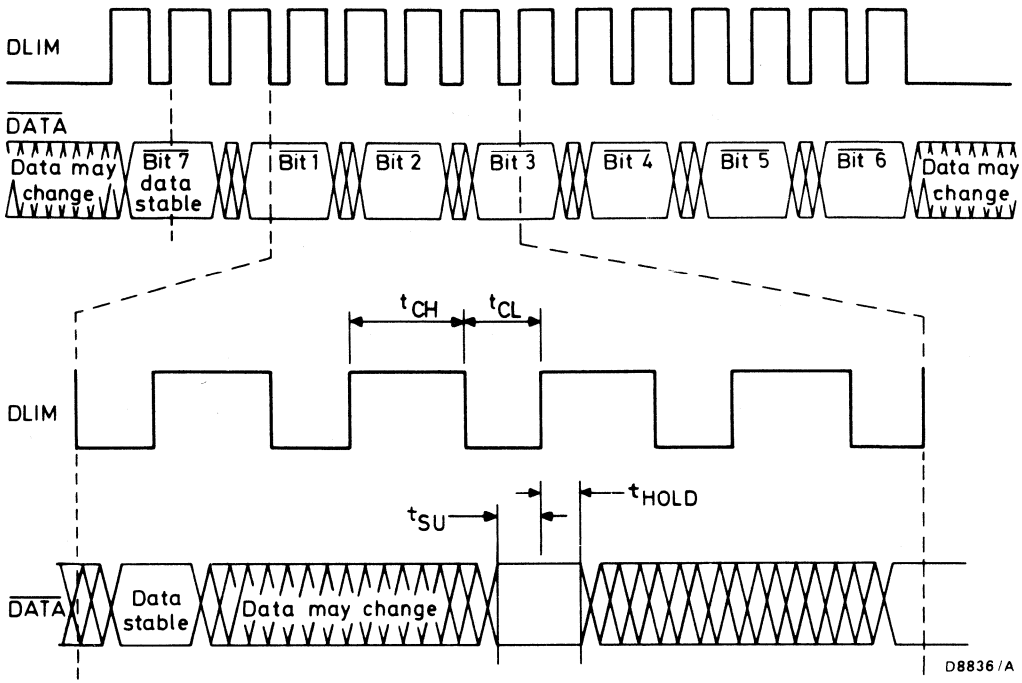
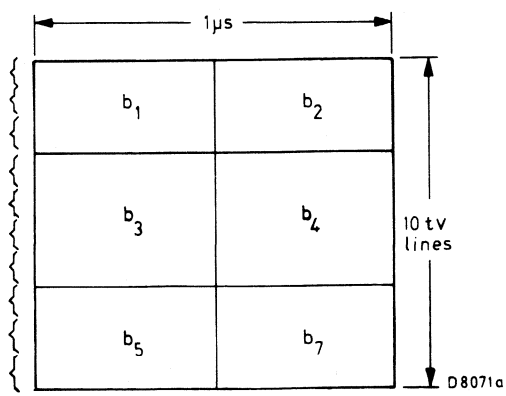


Fig.8 Remote control input timing



Each cell is illuminated if particular 'bit' (b_1, b_2, b_3, b_4, b_5, or b_7) is a '1'.
For graphics characters b_6 is always a '1' – See Table 1.

Fig.9 Graphics Character

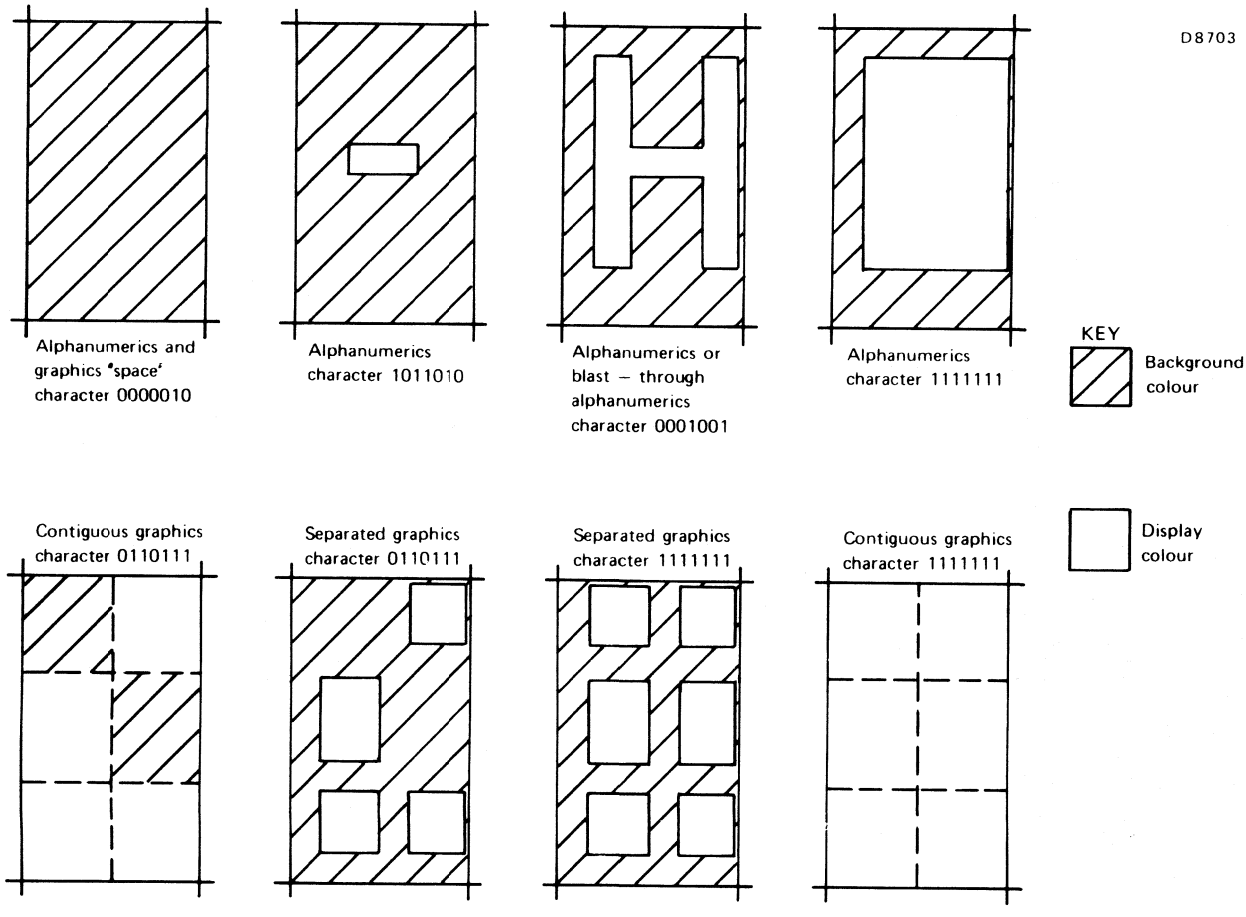


Fig.10 Character format

TABLE 1

Character data input decoding

D8068a

Bits b_4 b_3 b_2 b_1	Row	Col 0	Col 1	Col 2	Col 2a	Col 3	Col 3a	Col 4	Col 5	Col 6	Col 6a	Col 7	Col 7a
0 0 0 0	0	NUL*	DLE*	☐	☐	0	▗	@	P	-	▗	p	▄
0 0 0 1	1	Alpha^{n} Red	Graphics Red	!	▖	1	▖▗	A	Q	a	▖	q	▖▄
0 0 1 0	2	Alpha^{n} Green	Graphics Green	"	▝	2	▝▗	B	R	b	▝	r	▝▄
0 0 1 1	3	Alpha^{n} Yellow	Graphics Yellow	£	▀	3	▀▗	C	S	c	▀	s	▀▄
0 1 0 0	4	Alpha^{n} Blue	Graphics Blue	$	▌	4	▌▗	D	T	d	▌	t	▌▄
0 1 0 1	5	Alpha^{n} Magenta	Graphics Magenta	%	▌▖	5	▌▖▗	E	U	e	▌▖	u	▌▖▄
0 1 1 0	6	Alpha^{n} Cyan	Graphics Cyan	&	▌▝	6	▌▝▗	F	V	f	▌▝	v	▌▝▄
0 1 1 1	7	Alpha^{n} White**	Graphics White	'	▀▖	7	▀▖▗	G	W	g	▀▖	w	▀▖▄
1 0 0 0	8	Flash	Conceal Display	(	▀▝	8	▀▝▗	H	X	h	▀▝	x	▀▝▄
1 0 0 1	9	Steady**	Contiguous Graphics**	)	▌▝▖	9	▌▝▖▗	I	Y	i	▌▝▖	y	▌▝▖▄
1 0 1 0	10	End Box**	Separated Graphics	*	▌▀	:	▌▀▗	J	Z	j	▌▀	z	▌▀▄
1 0 1 1	11	Start Box	ESC*	+	▀▖	;	▀▖▗	K	←	k	▀▖	¼	▀▖▄
1 1 0 0	12	Normal Height**	Black Background**	,	▄	<	▄▗	L	½	l	▄	‖	▄▄
1 1 0 1	13	Double Height	New Background	-	▄▖	=	▄▖▗	M	→	m	▄▖	¾	▄▖▄
1 1 1 0	14	SO*	Hold Graphics	.	▄▝	>	▄▝▗	N	↑	n	▄▝	÷	▄▝▄
1 1 1 1	15	S1*	Release Graphics**	/	▄▀	?	▄▀▗	O	#	o	▄▀	■	▄▄

Control characters shown in columns 0 and 1 are normally displayed as spaces.
The SAA5050 character set is shown as example. Details of character sets are given in Figs. 11 to 18.

* These control characters are reserved for compatability with other data codes.

** These control characters are presumed before each row begins.

Codes may be refered to by their column and row e.g. 2/5 refers to %

☐ Character rectangle

Black represents display colour.

White represents background.

TABLE 2

Remote control command codes used in the SAA5050

CODE b_7	b_6	b_5	b_4	b_3	b_2	b_1	COMMAND	FUNCTION
0	X	X	X	X	X	X	'tv' mode	Allows text on top row of display only.
1	X	X	X	X	X	X	'Text' mode	Allows text throughout display period.
1	0	1	1	1	1	0	Superimpose	Sets Superimpose mode.
1	0	1	1	1	1	1	teletext	Resets Superimpose mode.
0	X	X	X	X	X	X	'tv' mode	Resets Superimpose mode.
1	1	X	X	X	X	X	viewdata mode	Resets Superimpose mode;
1	X	0	0	1	1	0	Reveal	Reveals for time-out (notes 3, 4).
1	X	0	1	0	1	1	Reveal set	Sets Reveal mode (note 3).
Any command apart from reveal set.								Resets Reveal mode (note 3)

X = Don't care.

Notes

1. When the power is applied the SAA5050 is set into the 'tv' mode and reset out of Superimpose and Reveal modes.
2. 'Text' mode is selected when $\overline{SI}$ (pin 2) is held LOW
3. Reveal mode allows display of text previously concealed by 'conceal display' control characters.
4. This code is sent from the SAA5010 or the SAA5012 Series as a repeated command. Thus Reveal mode is set for as long as the Reveal key is depressed. The SAA5050 reverts to normal 'not Reveal' mode 160 ms after the last Reveal command.
5. The Superimpose output is LOW only if Superimpose mode is set and the DE (display enable) input is HIGH.
6. The above table shows code required for functions specified.
   The SAA5010 or the SAA5012 Series transmits and the SAA5050 requires the inverse of these codes i.e. $\overline{b_7}$ to $\overline{b_1}$. The code is transmitted serially in the following order: $\overline{b_7}$ $\overline{b_1}$ $\overline{b_2}$ $\overline{b_3}$ $\overline{b_4}$ $\overline{b_5}$ $\overline{b_6}$.
   For full details of remote control data coding see the SAA5010 or the SAA5012 data sheets.

TABLE 3

Conditions affecting display (see note 3)

	Inputs		Control data		Outputs	
	Picture On (PO)	Display Enable (DE)	Superimpose Mode	Box	Text Display Enabled (i.e. R,G,B,Y outputs)	Blanking
(a)	1	0	1 or 0	1 or 0	0	0
(b)	0	1	1 or 0	1 or 0	1	1
(c)	0	0	1 or 0	1 or 0	0 (note 2)	1
(d)	1	1	0	0	0	0
(e)	1	1	1	0	1	0
(f)	1	1	1	1	1	1
(g)	1	1	0	1	1	1

Notes

1. For tv mode (Picture On = '1', Superimpose mode not allowed) rows (a), (d) and (g) of Table 3 refer to display row 0 only. For all other rows text display is disabled and Blanking = '0'.
2. The R, G, B outputs may contain character and background colour information. The only exception is that background colours are inhibited when Blanking = '0'.
3. Valid during display period only (see Fig.5) otherwise no character or background information is displayed as blanking is determined by the Picture On. (No blanking if PO = '1').

Fig. 11 SAA5050 character set (English).

Fig.12 SAA5051 character set (German).

Fig. 13 SAA5052 character set (Swedish).

Fig.14 SAA5053 character set (Italian).

Fig. 15 SAA5054 character set (Belgian)

Fig.16 SAA5055 character set (US ASCII).

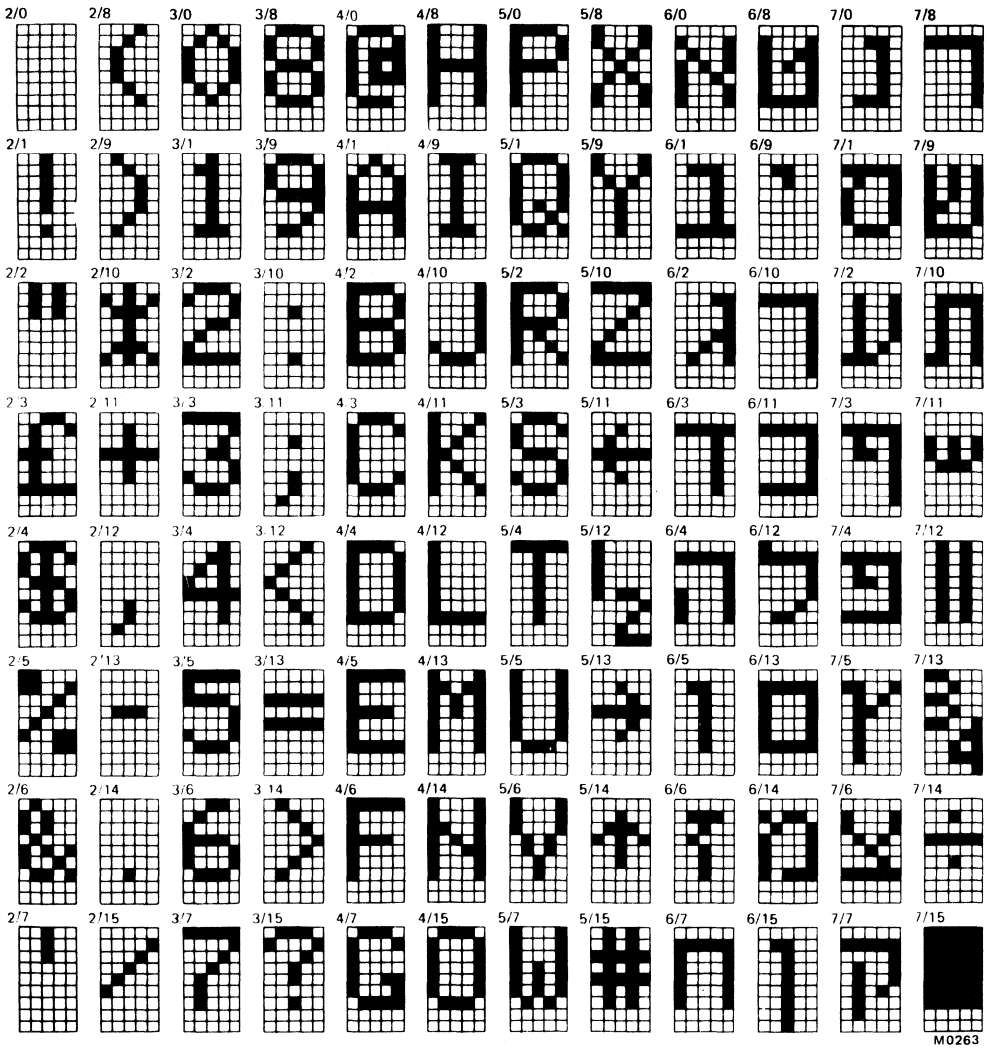


Fig.17 SAA5056 character set (Hebrew).

Fig.18 SAA5057 character set (Cyrillic).

MICROCOMPUTER/MICROPROCESSOR PERIPHERAL IC FOR VIEWDATA (LUCY)

The SAA5070 is a complex microcomputer/microprocessor peripheral integrated circuit in N-channel MOS technology intended for use in wired data communication systems, notably viewdata.

Features

- Microcomputer/microprocessor interface. • Modem – both 1200/75 and 1200/1200 baud.
- Line "UART" and tape recorder "UART", both with software parity control (or 8-bit without parity).
- Tape recorder modem (modified 'Kansas City' standard 1300 baud).
- Autodialler for British Post Office and Continental requirements.
- IBUS receivers and transmitters. • Timer circuits (60 s and 1.5 s time-outs).
- General input/output ports.
- Provision for connection of any external modem through V24 interface.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	75	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

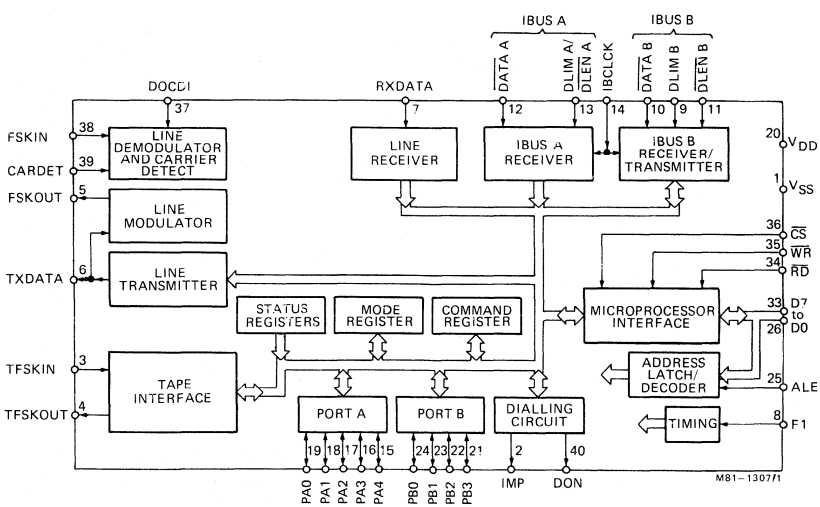
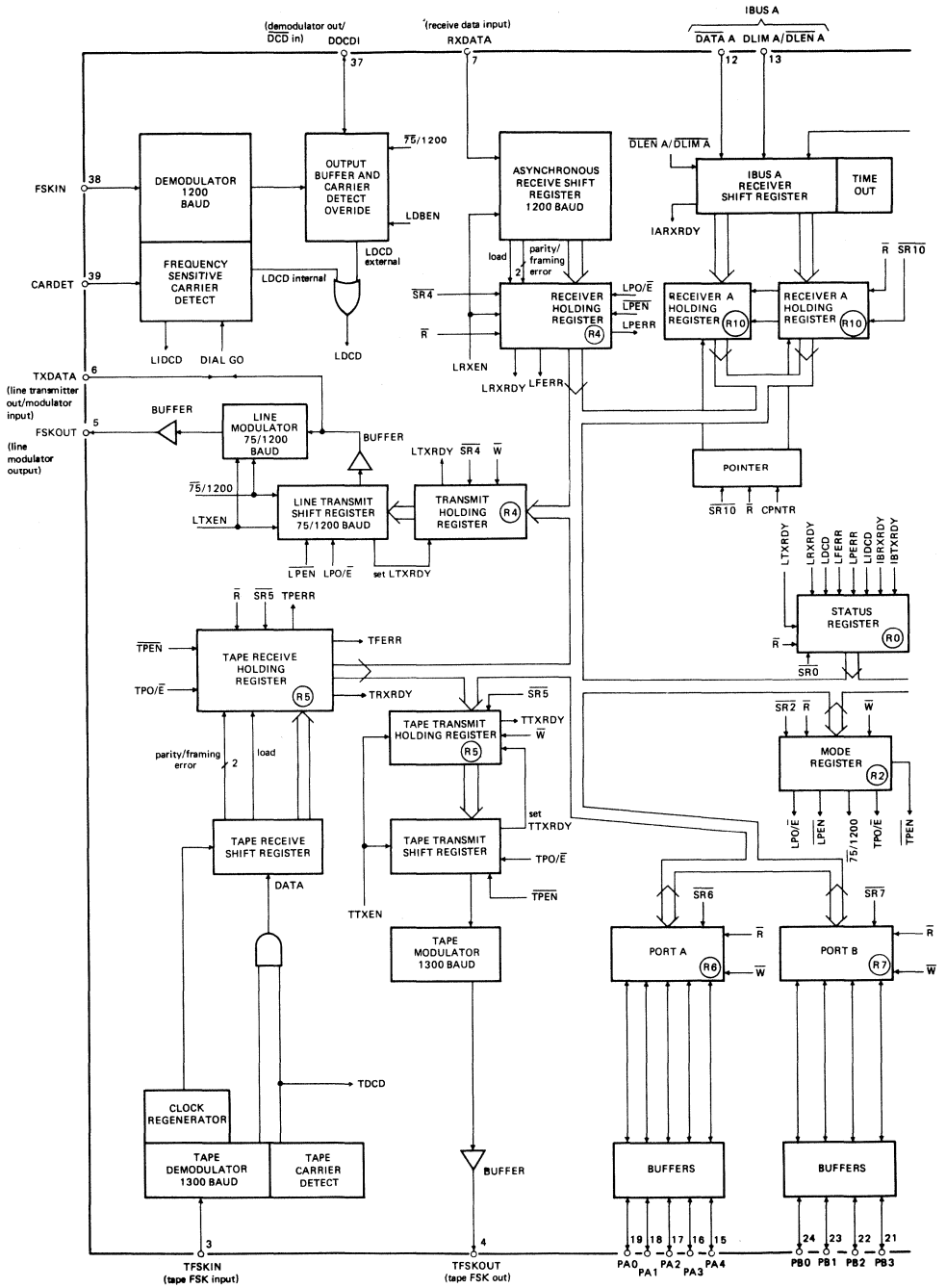


Fig.1a Simplified block diagram

PACKAGE OUTLINE

40-lead DIL; plastic (SOT−129).


IBUS A
DATA A
DLIM A/DLEN A
(demodulator out/ DCD in)
DOCDI
(receive data input)
RXDATA
37
7
12
13
FSKIN
38
DEMODULATOR 1200 BAUD
OUTPUT BUFFER AND CARRIER DETECT OVERIDE
75/1200
LDBEN
ASYNCHRONOUS RECEIVE SHIFT REGISTER 1200 BAUD
DLEN A/DLIM A
IBUS A RECEIVER SHIFT REGISTER
TIME OUT
IARXRDY
CARDET
39
FREQUENCY SENSITIVE CARRIER DETECT
LDCD external
LDCD internal
load
parity/ framing error
2
R
SR10
SR4
R
RECEIVER HOLDING REGISTER
R4
LPO/E
LPEN
LPERR
RECEIVER A HOLDING REGISTER
R10
LIDCD
DIAL GO
LDCD
LRXEN
LRXRDY
LFERR
TXDATA
6
(line transmitter out/modulator input)
FSKOUT
5
(line modulator output)
BUFFER
LINE MODULATOR 75/1200 BAUD
LTXRDY
SR4
W
POINTER
75/1200
LTXEN
LINE TRANSMIT SHIFT REGISTER 75/1200 BAUD
TRANSMIT HOLDING REGISTER
R4
LPEN
LPO/E
set LTXRDY
SR10
R
CPNTR
LTXRDY
LRXRDY
LDCD
LFERR
LPERR
LIDCD
IBRXRDY
IBTXRDY
STATUS REGISTER
R0
SR0
R
SR5
TPERR
TPEN
TAPE RECEIVE HOLDING REGISTER
R5
TFERR
TPO/E
TRXRDY
SR5
TAPE TRANSMIT HOLDING REGISTER
R5
TTXRDY
W
SR2
R
W
MODE REGISTER
R2
parity/framing error
2
load
set TTXRDY
LPO/E
LPEN
75/1200
TPO/E
TPEN
TAPE RECEIVE SHIFT REGISTER
TAPE TRANSMIT SHIFT REGISTER
TPO/E
TPEN
DATA
TTXEN
SR6
SR7
PORT A
R6
R
W
PORT B
R7
R
W
TAPE MODULATOR 1300 BAUD
TDCD
CLOCK REGENERATOR
TAPE DEMODULATOR 1300 BAUD
TAPE CARRIER DETECT
BUFFER
BUFFERS
BUFFERS
3
4
19
18
17
16
15
24
23
22
21
TFSKIN
(tape FSK input)
TFSKOUT
(tape FSK out)
PA0
PA1
PA2
PA3
PA4
PB0
PB1
PB2
PB3

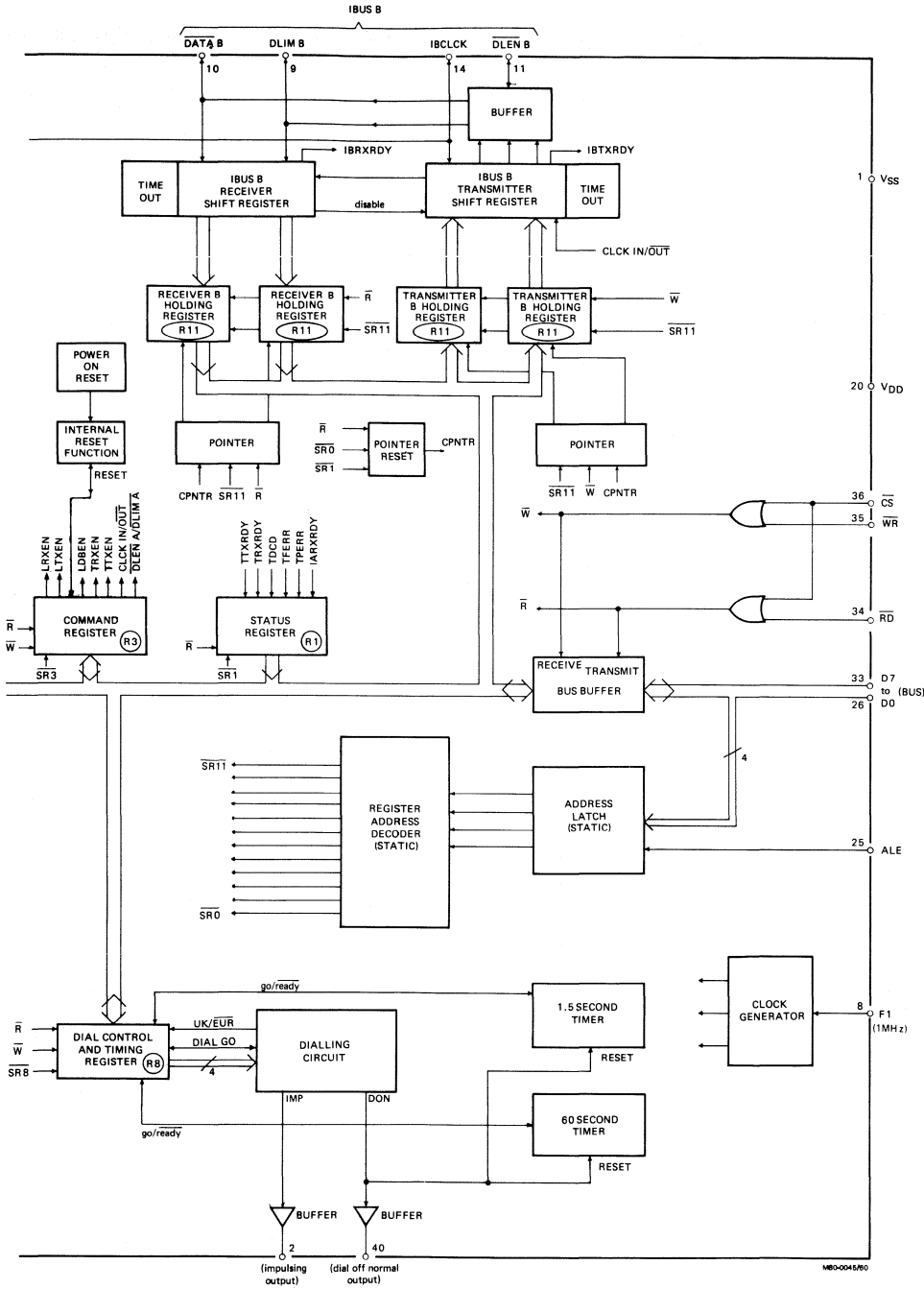


Fig. 1b. Detailed block diagram

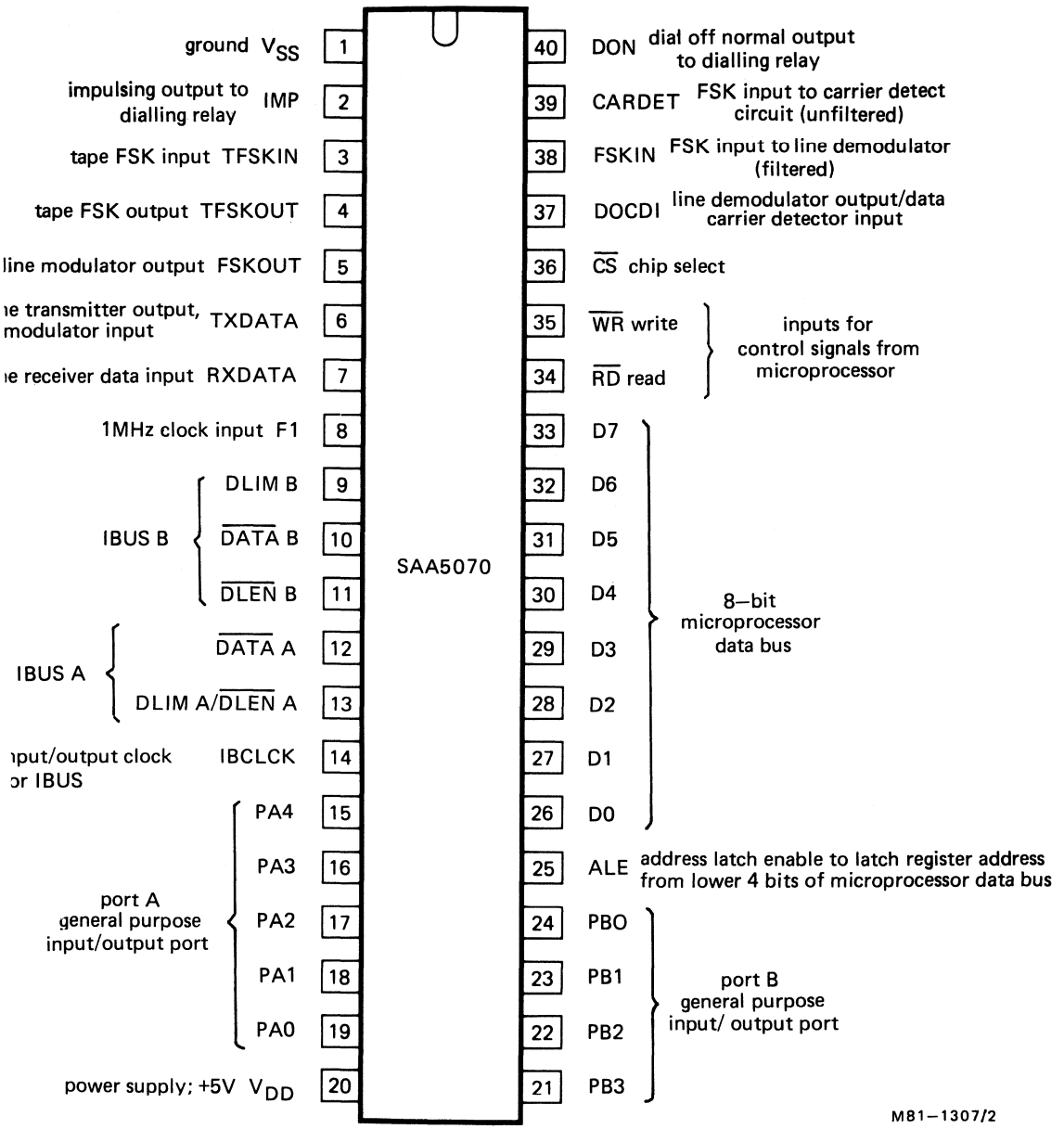


Fig.2 Pinning diagram

DESCRIPTION

The SAA5070 is a 40 pin integrated circuit in N-channel MOS with a 1 MHz clock supplying all the operating frequencies. It performs most of the hardware functions of a viewdata terminal including an autodialling circuit, a 1200 baud demodulator and asynchronous receiver, and a 75/1200 baud modulator and asynchronous transmitter.

The device also includes a tape interface circuit suitable for the recording of character codes of pages of text on a standard audio cassette recorder, and an IBUS receiver and receiver/transmitter on separate ports enabling the software recoding of IBUS transmissions. The 75 baud modulator and asynchronous transmitter can be switched to operate at 1200 baud for private telecommunications systems.

There are also two general purpose input/output ports. Port A could, for example, be used as an interface to a non volatile RAM which can store telephone numbers for autodialling and user passwords and Port B could be used for display control.

The SAA5070 has been partitioned for flexibility of use, e.g. an external modem can be used, if required, in conjunction with the internal asynchronous receiver and transmitter, or the internal modem can be used independently of the internal receiver and transmitter. Also the tape interface can work independently of, and simultaneously with, the line receiver.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. (See 'HANDLING MOS DEVICES').

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Voltages (with respect to pin 1)		min.	typ.	max.	
Supply voltage (pin 20)	V_{DD}	−0.3	–	7.5	V
Input voltage:					
PORT A (pins 15 to 10) and PB0 (pin 24)	V_I	−0.3	–	14.0	V
Input voltage (all other pins)	V_I	−0.3	–	7.5	V
Temperatures					
Storage temperature range	T_{stg}			−20 to +125	°C
Operating ambient temperature range	T_{amb}			−20 to +70	°C

CHARACTERISTICS

Supply voltage (pin 20)	V_{DD}	4.5	–	5.5	V

The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.

Supply current	I_{DD}	–	75	150	mA
Inputs					
All inputs (except F1 clock)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

Data specific to certain inputs

			min.	typ.	max.	
F1 (1 MHz) Clock						
Input voltage; LOW		V_{IL}	−0.3	–	0.6	V
Input voltage; HIGH		V_{IH}	2.2	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V)		I_{IR}	–	–	10	μA
Input capacitance		C_I	–	–	7	pF
Mark/space ratio (measured at 1.5 V level)			40:60	–	60:40	
$\overline{\text{DATA}}$ A, DLIM A/$\overline{\text{DLEN}}$ A (IBUS A)						
Data set up time	Fig.14	t_{DS}	3	–	–	μs
Data hold time		t_{DH}	3	–	–	μs
DLIM clock; HIGH		t_{CH}	4	–	–	μs
DLIM clock; LOW		t_{CL}	4	–	62	μs
Time between commands		t_{BC}	140	–	∞	μs
DLIM frequency		f_{DLIM}	16	–	160	kHz
ALE (Address Latch Enable) (Figs. 3 and 4)						
Pulse width (HIGH)		t_{ALEH}	400	–	–	ns
Cycle time		T_{ALE}	–	2500	–	ns
$\overline{\text{RD}}$, $\overline{\text{WR}}$ and $\overline{\text{CS}}$ (Figs. 3 and 4)						
Control pulse width		t_{WL}	–	700	–	ns
Address hold time		t_{LA}	80	–	–	ns
Address set-up time		t_{AL}	120	–	–	ns
Read cycle timings (Fig.3)						
ALE to read pulse delay time		t_{ALR}	80	–	–	ns
Read pulse (falling edge) to data bus delay time		t_{RD}	–	–	500	ns
Data hold time		t_{DR}	0	–	200	ns
Write cycle timings (Fig.4)						
ALE to write pulse delay time		t_{ALW}	80	–	–	ns
Address set-up time to $\overline{\text{WR}}$		t_{AW}	230	–	–	ns
Data set up time before $\overline{\text{WR}}$		t_{DW}	500	–	–	ns
Data hold time after $\overline{\text{WR}}$		t_{WD}	120	–	–	ns

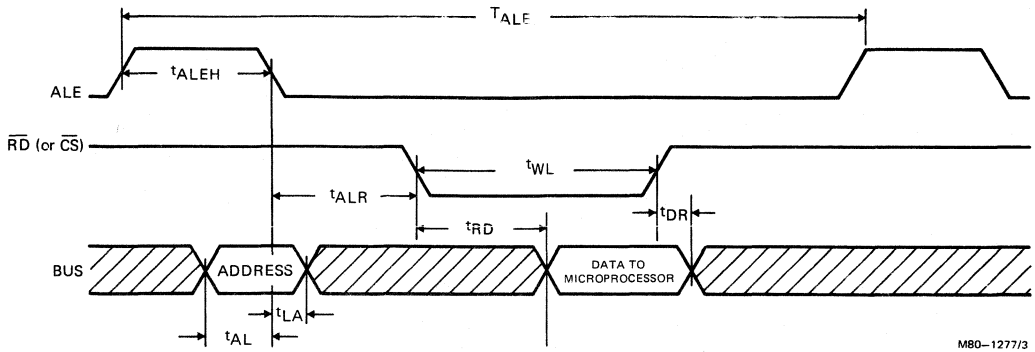


Fig.3 Read cycle timing

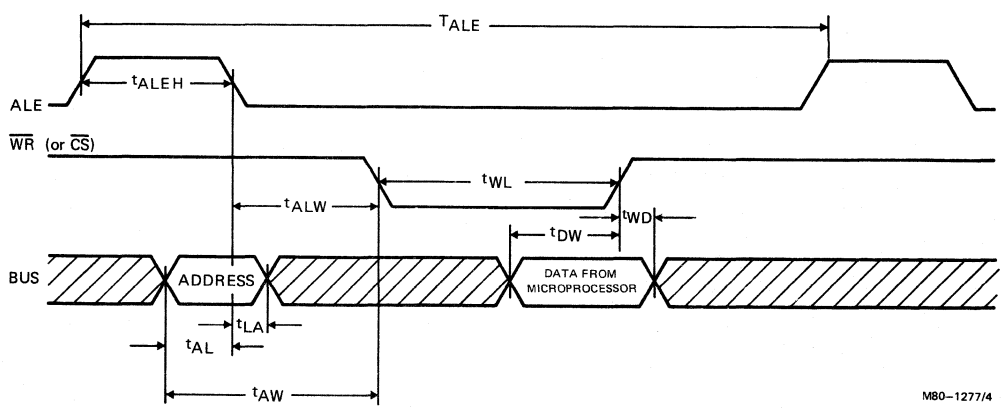


Fig.4 Write cycle timing

Inputs/Outputs

These are protected against connection to V_{SS} or V_{DD}

$\overline{\text{DATA}}$ B, DLIM B, $\overline{\text{DLEN}}$ B, IBCLCK (IBUS B)			min.	typ.	max.	
Input voltage; LOW	Fig.14	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V) (3 state buffers off)		I_{IR}	–	–	10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)		V_{OH}	2.4	–	–	V
Output rise and fall times (C_L = 300 pF)		t_r, t_f	–	–	1	μs
other timings as IBUS A						
$\overline{\text{DOCDI}}$ (open drain output)						
Input voltage; LOW		V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	5.5	V
Input leakage current; (V_I = 0 to 5.5 V) (output transistor off)		I_{IR}	–	0.4	10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	0.4	–	V
TXDATA						
(Internal resistive pull-up, permitting wired - AND connection)						
Input voltage; LOW		V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	5.5	V
Input current; LOW (V_I = 0.4 V)		$-I_{IL}$	–	–	500	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 50 μA)		V_{OH}	2.4	–	–	V
Load capacitance		C_L	–	–	40	pF
Output rise time (C_L = 40 pF)		t_r	–	3	–	μs
PA0 to PA4 (PORT A) (open drain output)						
Input voltage; LOW		V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	13.2	V
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	V
Off state leakage current (V_I = 0 to 13.2 V)		I_{OR}	–	–	10	μA
Load capacitance		C_L	–	–	40	pF
Fall time		t_f	–	–	1	μs

Inputs/Outputs (continued)		min.	typ.	max.	
PBO (PORT B) (open drain output) as PORT A except					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH	V_{OH}	–	–	13.2	V
Load capacitance	C_L	–	–	100	pF
PB1 to PB3 (PORT B)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input capacitance	C_I	–	–	7	pF
Load capacitance	C_L	–	–	100	pF
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Off state leakage current (V_I = 0 to 5.5 V)	I_{OR}	–	–	10	μA
D0 to D7 (8-bit Data bus)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V
Input leakage current (V_I = 0 to 5.5 V) (3-state buffers off)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output rise and fall times (C_L = 150 pF)	t_r, t_f	–	–	150	ns
Outputs					
These are protected against connection to V_{SS} or V_{DD}.					
FSKOUT and TFSKOUT					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V
Rise and fall times (C_L = 100 pF)	t_r, t_f	–	–	500	ns
DON and IMP					
Output voltage; LOW (I_{OL} = 50 μA)	V_{OL}	–	–	0.2	V
Output current; HIGH (V_{OH} = 0.8 V clamped)*	I_{OH}	200	–	2000	μA
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V

Autodialling timings are given in Fig.6

*These outputs are normally intended to drive the base-emitter junction of a bipolar transistor and so in normal use the V_{OH} may be clamped to V_{be}.

RESET FUNCTION

It is possible to reset the SAA5070 to its nominal state either automatically on power-on by means of an internal power-on reset circuit, or by setting D5 in command register (R3) to '1', which returns to '0' on completion of the reset sequence. The device resets to viewdata mode, i.e. 75 baud transmit rate, even parity, etc, as shown by the all zero's state in registers R0 to R3, R6, R7 and R8 except for LTXRDY, IBTXRDY, and TTXRDY (in the status registers R0 and R1) which will come up as '1' after the transmitters have been reset, showing that they are ready to accept new data.

APPLICATION DATA

Chip organisation

Each section of the SAA5070 may be accessed by the microprocessor via a register (of up to 8-bits) connected to an internal data bus. There are 15 registers on chip accessed by 11 addresses. Some of the registers are two-level, i.e. two bytes of data are transferred by two successive read (or write) sequences to the same address, also some read only registers have the same address as a write only register.
An appendix lists the registers, their contents, and their use.

Section descriptions

The description of each section includes associated registers, flags, and pins, as well as the method of operation. On the following block diagrams external pins are shown boxed and internal flags are shown underlined.

Microprocessor Interface

D0 to D7 — I/O — 8-bit input/output port

Associated pins:	ALE	input	address latch enable from microprocessor
	$\overline{WR}$	input	write pulse from microprocessor
	$\overline{RD}$	input	read pulse from microprocessor
	$\overline{CS}$	input	chip select

Operation

The control microprocessor communicates with the SAA5070 via an 8-bit data I/O port D0 to D7. An internal read or write pulse is produced by gating $\overline{RD}$ and $\overline{WR}$ with $\overline{CS}$. A single register is enabled onto the internal bus by gating the read or write lines with the address decoder outputs. The register address is taken from the 4 least significant data bits latched on the falling edge of ALE. (See timing diagrams Figs. 3, 4). The address (D3 most significant, D0 least significant) relates directly to the register numbers shown in the register map, detailed in the appendix, and referred to in other section descriptions.

Four registers not specifically related to any one section are included. These are the status registers R0 and R1, the mode register R2, and the command register R3. These registers are used to determine the current status of the device, to dictate the mode of operation or to initiate a specific operation. The status registers are read only, the mode and command registers are read/write. When writing to these registers, it is recommended that the unallocated bits are set to '0'. On reading the registers the state of the unallocated bits should be assumed to be random. The exact functions of the flags contained in these registers are described in the section description to which they relate.

Autodial section (see Fig.5)

Associated Register: — R8 — D0 to D3 write only
D4 to D7 read/write

Associated flags in other registers: None

Associated pins:	DON	output	to drive dialling relays
	IMP	output	

Operation

The autodial section includes a clock divider, a digit impulse counter, a sequence controller and an impulse generator (see block diagram Fig.5). A sequence to generate the impulses for one digit is initiated by setting D5 (DIAL GO) to '1', D3 to D0 to the binary code of the required digit, and D7 to the required mode. This initiates the sequence controller which loads the binary code into the digit impulse counter. The counter then generates the correct number of impulses at the rate of 10 per second, together with a DON pulse which overlaps the impulses by about 7 ms at the start and end (see Figs.6, 7); the interdigit pause period is also added by the sequence controller. D5 is reset to '0' at the end of a dialling sequence and may be read by the microprocessor to determine when the dial circuit is free to accept the next digit.

D7 (UK/$\overline{\text{EUR}}$) determines the mark/space ratio of the IMP pulses

UK = 2 off to 1 on
$\overline{\text{EUR}}$ = 1.5 off to 1 on
} both one pulse per 100 ms

There is a timer in the dial circuit which can be used to time out 1.5 seconds or 60 seconds by setting D4 or D6 respectively. These bits are read/write and are reset after the relevant time out period. In addition the 60 second timer can be reset by writing a '0' to D6. The 60 second timer may be used typically by the microprocessor to release the telephone line if connection has not been made within 60 seconds. The DON pulse resets the counter so that the time out is taken from the end of the last digit dialled. Once a dialling sequence for one digit has been initiated, R8 should be used only in read mode until D5 has been reset internally to '0' indicating the end of the dial sequence for that digit.

When D5 (DIAL GO) is set to '1' the carrier detect circuit (see the next section and Fig.8) is disabled.

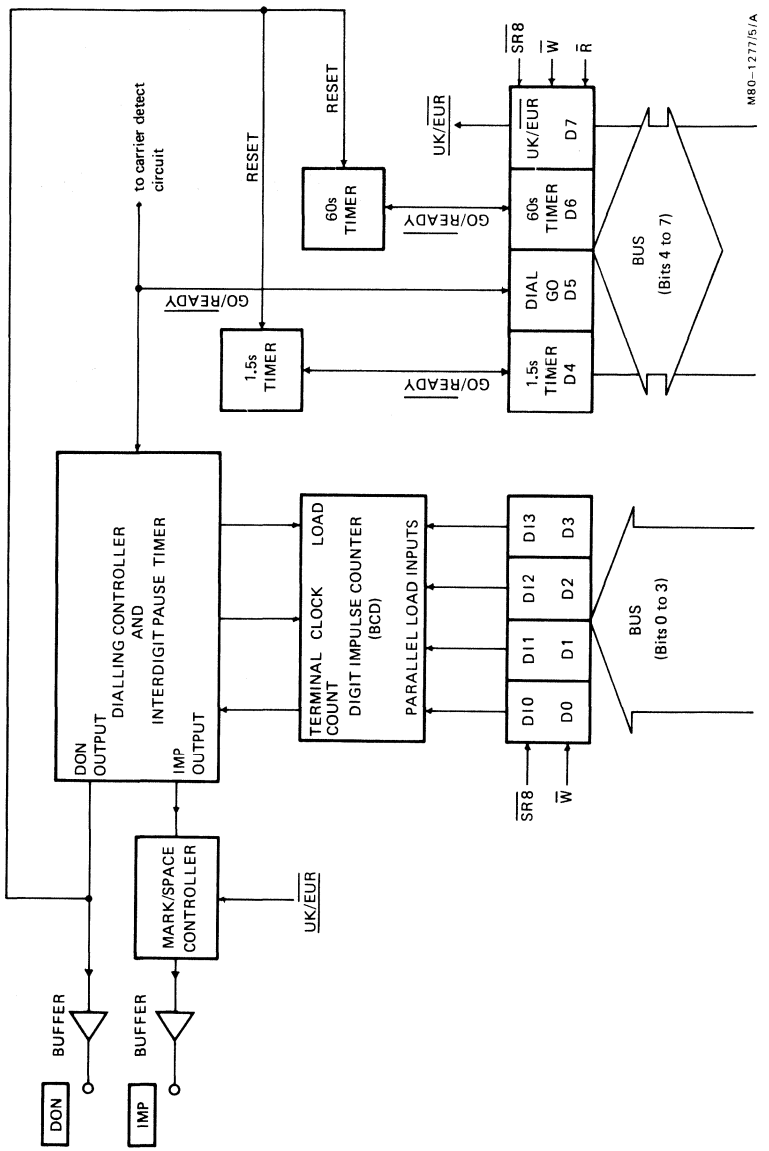


Fig.5 Autodial block diagram

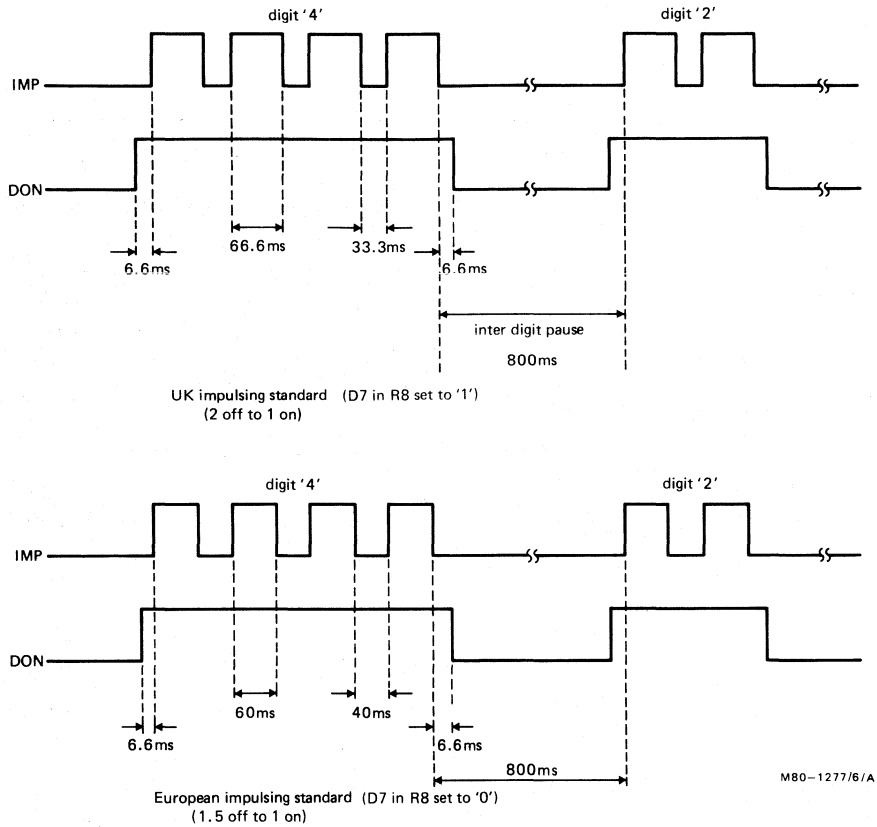


Fig.6 Autodialling timing

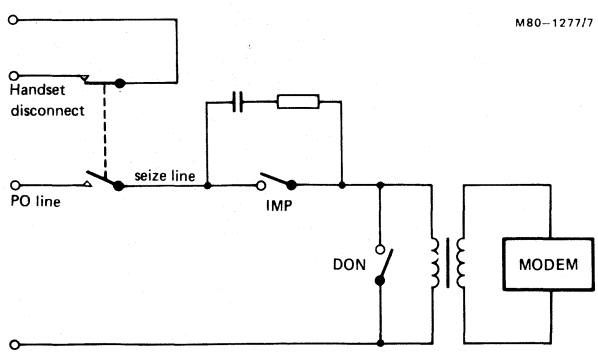


Fig.7 Simplified relay diagram

Line Demodulator and Carrier Detect (see Fig.8)

Associated Register:– None

Associated flags in other registers:

LIDCD	–	D2	–	R0 (Status)	–	instantaneous carrier detect flag
LDCD	–	D5	–	R0 (Status)	–	carrier detect flag
$\overline{75}$/1200	–	D5	–	R2 (Mode)	–	transmit frequency baud rate (used in demodulator carrier detect circuit)
LDBEN	–	D4	–	R3 (Command)	–	line demodulator output buffer and carrier detect enable
DIAL GO	–	D5	–	R8 (Dial control)	–	used to disable carrier detect circuit during dialling sequence

Associated pins:	FSKIN	– input	–	filtered, squared F.S.K. signal
	CARDET	– input	–	unfiltered (squared) F.S.K. signal.
	DOCDI	– input/output	–	demodulator output, external LDCD in

Operation

The input to the demodulator is the previously filtered and squared up F.S.K. signal from the telephone line. Its output is a pseudo analogue signal which must be externally filtered and squared to produce the demodulated data. The carrier detect circuit functions in the following modes:

a) Viewdata mode (1200 baud receive, 75 baud transmit). Initially, a narrow frequency band 'window' around 1300 Hz is accepted as carrier, this must be applied to the CARDET input. If a frequency in this range is present, the 'instantaneous carrier detected' flag will be HIGH (LIDCD), after about 2 seconds the 'line carrier detected' flag will be set HIGH (LDCD). When this occurs, the frequency window is widened to include 2100 Hz and the circuit no longer takes its input from the CARDET pin, but from the FSKIN pin.
If carrier is then removed LIDCD immediately goes LOW, and after about 1 second LDCD is reset, the frequency window again becomes narrow and around 1300 Hz and the CARDET input again becomes active. Reappearance of carrier in the 1300 Hz range will cause a repeat of the above.

b) 1200 baud each way mode
Only the instantaneous carrier detect is active in this mode. LDCD is forced LOW and the CARDET input inhibited (only FSKIN should be used in this mode).

c) External carrier detect input
If an external modem is used its (active LOW) carrier detect output is connected to DOCDI. Provided that the demodulator is not enabled, LDCD will be set if DOCDI is LOW and reset if it is HIGH.

Demodulator enable

LDCD is produced by the carrier detect circuit, which is enabled by LDBEN and disabled by DIAL GO, In the viewdata mode the demodulator is enabled by LDCD.
In the 1200 baud each way mode the demodulator is enabled directly by LDBEN.

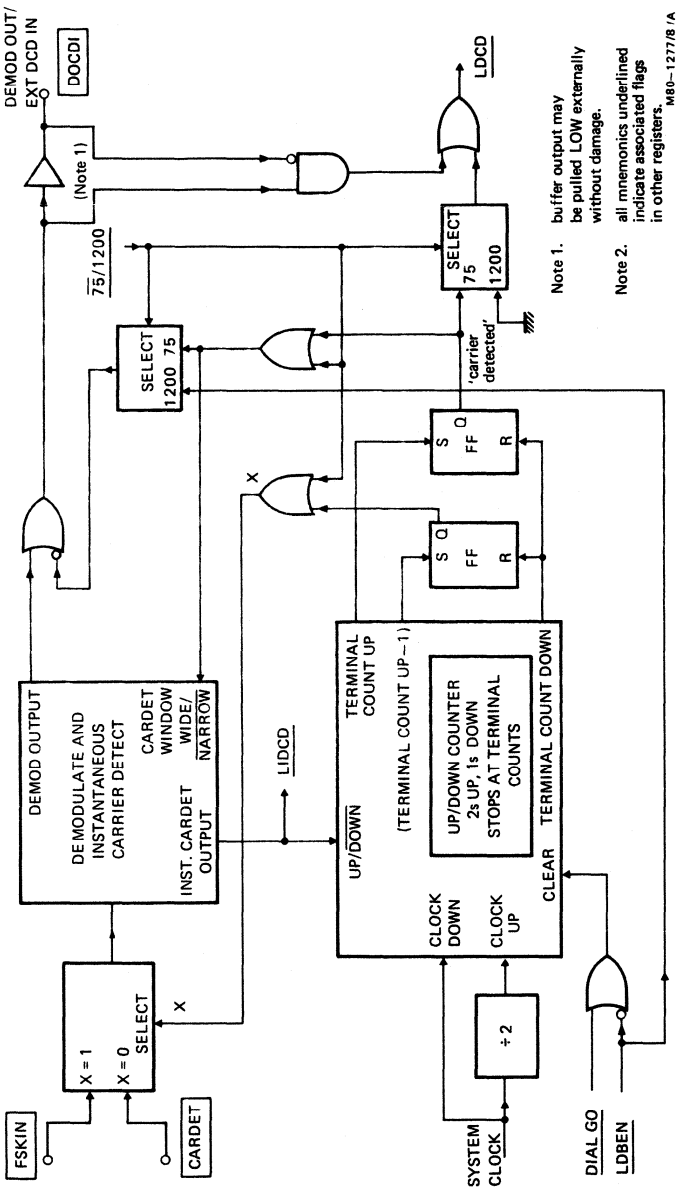


Fig.8 Line demodulator and carrier detect block diagram

Line Receiver (see Fig.9)

Associated Register: — R4 read only

Associated flags in other registers:

LRXRDY	—	D6	—	R0 (status)	—	valid data available in receive holding register
LFERR	—	D4	—	R0 (status)	—	line framing error (derived from STOP bit of message).
LPERR	—	D3	—	R0 (status)	—	line parity error.
LPO/$\overline{E}$	—	D7	—	R2 (mode)	—	odd or even parity detection mode select
$\overline{LPEN}$	—	D6	—	R2 (mode)	—	8 bit data or 7 bit plus parity mode select
LRXEN	—	D7	—	R3 (command)	—	line receiver enable.

Associated pins: RXDATA — input — received data input

Operation

The receiver may be configured to work with either 7 data bits and 1 parity, or with 8 data bits and no parity. Odd or even parity can be detected on chip, the LPERR flag being set when an error is detected. The required mode of operation should be selected by setting $\overline{LPEN}$ and LPO/$\overline{E}$ to the required states by writing to mode register (R2) before enabling the receiver by setting LRXEN to '1' in command register (R3). The data format is 10 bits per data word. The data word is made up of a start bit (LOW), 8 data bits, the 8th being an optional parity bit, and a stop bit (HIGH). The receive data will remain HIGH after the stop bit until the next data word. When the receiver has been enabled a negative transition is looked for on the RXDATA input indicating a possible start bit. After half a bit rate period the data is sampled again and if it is still LOW it is interpreted as a start bit, initiating a sequence which clocks the data into a shift register. When the full ten bit message has been received, the 8 data bits are parallel loaded into the receiver holding register (R4), the LRXRDY flag is set to '1'. The complement of the stop bit is loaded into the LFERR latch and the result of the parity check is loaded into LPERR latch. If line parity is not enabled i.e. $\overline{LPEN}$ = '1', then LPERR is held at '0'. The LRXRDY flag is reset to '0' after the microprocessor has read the receiver holding register (R4). The receiver has a 52 times baud rate factor to allow for maximum isochronous distortion.

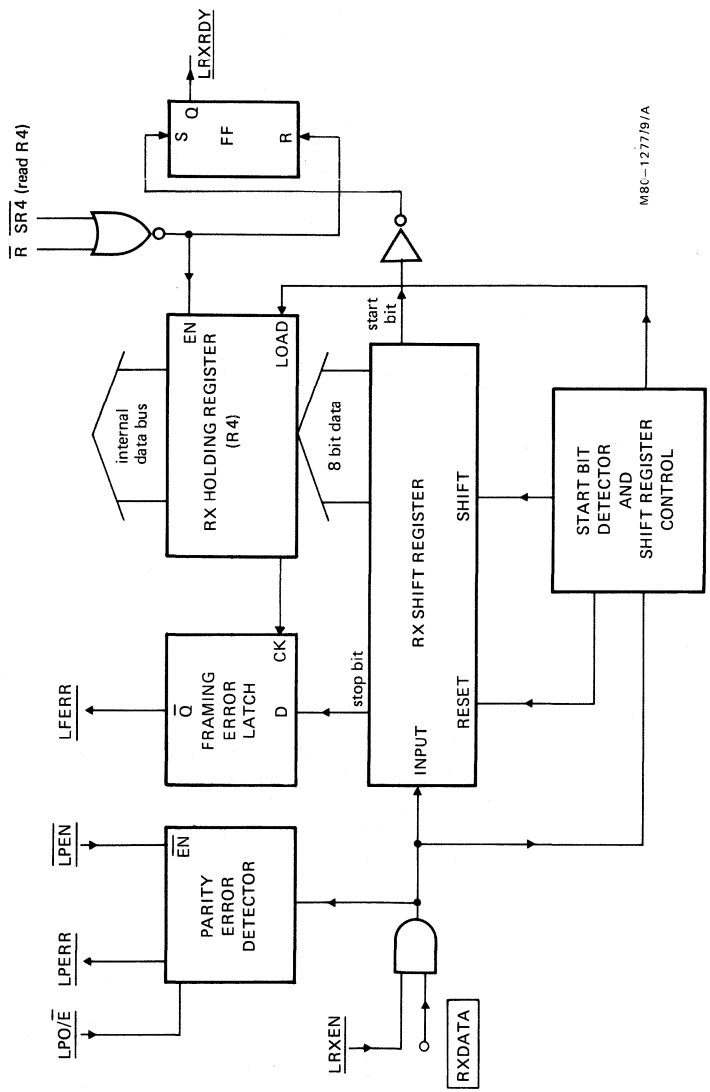


Fig.9 Line receiver block diagram

Line Transmitter (see Fig.10)

Associated Register: — R4 write only

Associated flags in other registers:

LTXRDY	—	D7	—	R0 (status)	—	transmit holding register ready to accept new data
LPO/$\overline{E}$	—	D7	—	R2 (mode)	—	odd or even parity mode select
$\overline{LPEN}$	—	D6	—	R2 (mode)	—	8 bit data or 7 bit data with parity mode select
$\overline{75}$/1200	—	D5	—	R2 (mode)	—	select transmit baud rate
LTXEN	—	D6	—	R3 (command)	—	line transmitter/modulator output enable

Associated pins: TXDATA — I/O — transmitter output (and also modulator input)

Operation

The data format of the transmitter is the same as that of the line receiver i.e. 10-bits, a start bit (LOW) followed by 8-data bits, the 8th bit being an optional parity (selected by $\overline{LPEN}$), odd or even parity being selectable (by LPO/$\overline{E}$) ending with a STOP bit (HIGH) the output remaining HIGH until the next data word is written.

The transmitter and modulator may be used together or separately. The transmitter output is brought to the TXDATA pin (if LTXEN = 1) which is connected internally to the modulator input. The TXDATA pin has an internal resistive pull up permitting wire - AND connection. If the modulator is used with an off chip data source (e.g. UART) then data should not be written to the internal transmit holding register (R4). The STOP bit (HIGH) will then be continuously output when LTXEN = 1 (required to enable modulator output) allowing the external UART to control the TXDATA (pin 6).

To operate the transmitter the required mode should be set-up initially by writing to the mode register (R2) the required states of $\overline{75}$/1200, $\overline{LPEN}$, LPO/$\overline{E}$. The transmitter can then be enabled by setting LTXEN to '1' in the command register (R3). The 8-bit data word can then be written to the transmit holding register (R4). If parity is enabled then the 8th bit is ignored and the value of the parity bit calculated from the first 7-data bits and LPO/$\overline{E}$. The LTXRDY flag is set to zero when the holding register is written into. If the transmit output shift register is not currently in use the contents of the holding register are transferred to the output shift register and LTXRDY returns to '1'. This means that new data may now be written to the holding register but will not be transferred to the output shift register until the 10-bits of the current message have been clocked out. The start, stop, and parity bit (if selected) are written into the output shift register with the data word automatically.

Two transmit baud rates are selectable, 75 baud for viewdata transmissions or 1200 baud for private data communication systems.

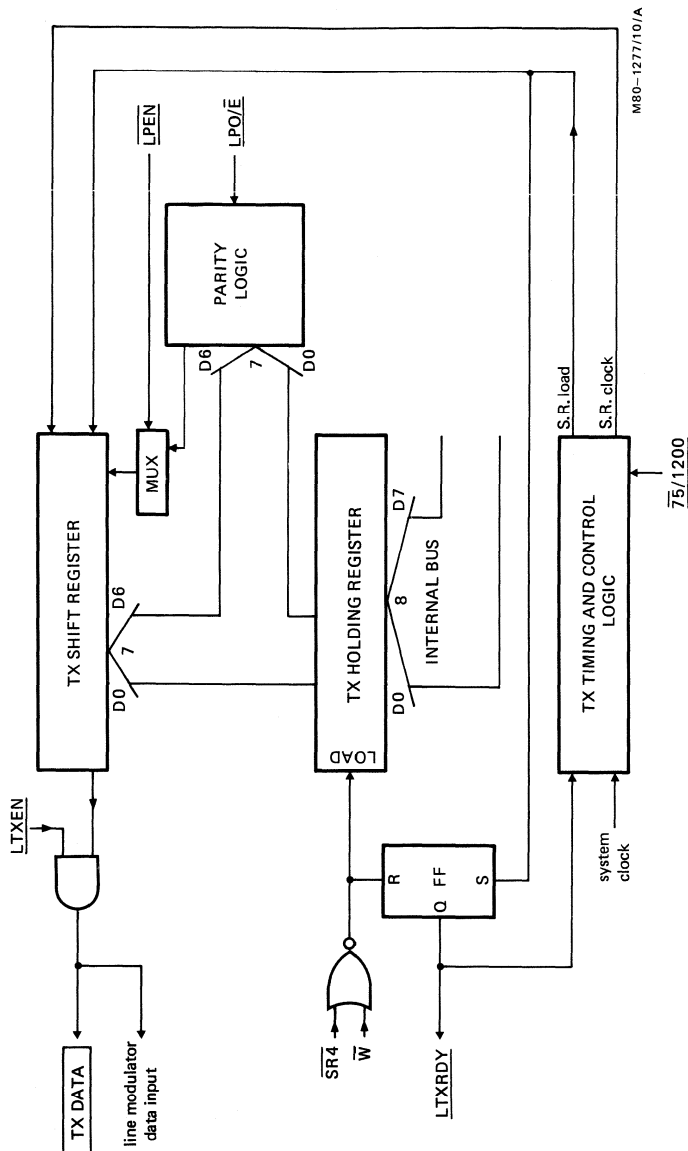


Fig.10 Line transmitter block diagram

Line Modulator (see Fig.11)

Associated Register: — None

Associated flags in other registers:

$\overline{75}$/1200	—	D5	—	R2 (mode)	—	transmit baud rate select.
LTXEN	—	D6	—	R3 (command)	—	line transmitter/modulator output enable.

Associated Pins:	TXDATA	—	I/O	—	modulator input (also (on chip) transmitter output).
	FSKOUT	—	output	—	line modulator output

Operation

The modulator generates a pseudo analogue signal from a serial shift register which is parallel loaded with patterns from an internal ROM. The frequency of the sine wave is determined by the selected baud rate $\overline{75}$/1200, and the value of the data on TXDATA (pin 6).

data	'1'	'0'
1200 baud	1300 Hz	2100 Hz
75 baud	390 Hz	450 Hz

One sine wave cycle is comprised of a 92-bit pattern which after minimal external low pass filtering provides a suitable F.S.K. signal out (see Fig.11)

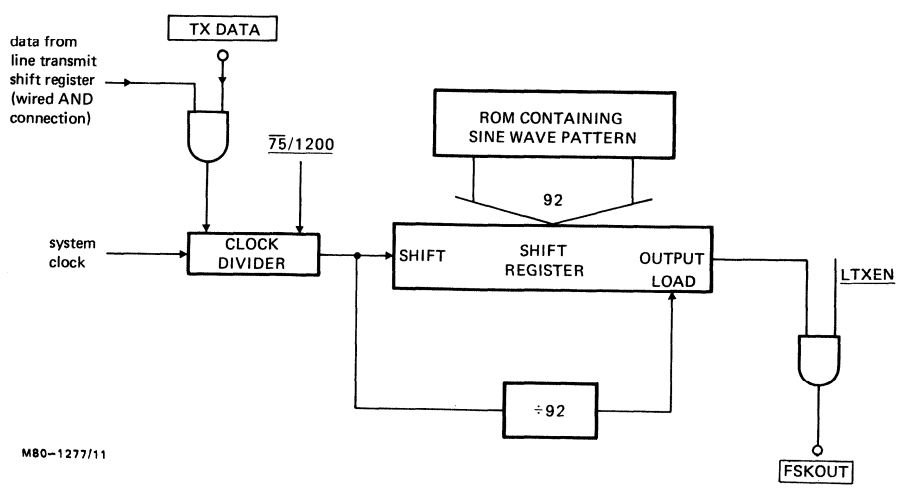


Fig.11 Line modulator block diagram

Tape section (see Fig.12)

Associated registers: — R5 — Consists of two registers with the same address:
transmit holding register write only
receive holding register read only

Associated flags in other registers:

TTXRDY	—	D7	—	R1 (status)	—	transmit holding register ready to accept new data
TRXRDY	—	D6	—	R1 (status)	—	valid data available in receive holding register
TDCD	—	D5	—	R1 (status)	—	tape data carrier detect flag
TFERR	—	D4	—	R1 (status)	—	tape framing error (derived from STOP bit of message)
TPERR	—	D3	—	R1 (status)	—	tape parity error
TPO/$\overline{E}$	—	D3	—	R2 (mode)	—	odd or even parity mode select.
$\overline{TPEN}$	—	D2	—	R2 (mode)	—	8-bit data or 7-bit plus parity mode select
TRXEN	—	D3	—	R3 (command)	—	tape receiver enable
TTXEN	—	D2	—	R3 (command)	—	tape transmitter enable

Associated pins:	TFSKIN	— input	—	F.S.K. input to tape sections
	TFSKOUT	— output	—	F.S.K. modulated data out

Operation of tape section (see Fig.12)

The tape data modulation system is a modified form of the 'Kansas City' standard. A logic '1' is represented by one cycle of 1300 Hz, and a logic '0' by two cycles of 2600 Hz, the data rate being 1300 baud. The data format is the same as that for viewdata, i.e. 10-bit words consisting of a START bit (LOW), followed by 8-data bits, the 8th being an optional parity bit, ending with a STOP bit (HIGH) which is continuous until the next data word.

To operate the tape section the required parity mode should first be set up by writing the required states of TPEN and TPO/$\overline{E}$ to the mode register (R2). The TTXEN command enables the output of the transmit shift register into the modulator, and should be set before data is written to the transmit holding register. (With TTXEN = '0' the modulator outputs a continuous 1300 Hz signal '1'). When a data word is written to the transmit holding register the TTXRDY flag is reset to '0'. If the transmit shift register is not currently active the contents of the holding register, along with valid parity bit (if enabled) and the START and STOP bits are transferred to the transmit shift register, at the same time TTXRDY is set to '1'. The holding register is then free to accept new data but this will not be transferred to the shift register until the current data has been clocked out. Data should be written to the tape transmit holding register, therefore, only when TTXRDY = '1'.

The modulator produces 1300 Hz and 2600 Hz signals which occur synchronously with the data from the transmitter. Hence a '1' is one complete 1300 Hz cycle, and a '0' two complete 2600 Hz cycles. The modulator output, TFSKOUT, requires minimal external low pass filtering to produce data suitable for audio cassette tape recorders.

To overcome the tendency of cassette recorders to attenuate high frequencies, the 1300 Hz signal contains 2 μs wide attenuating pulses every 12 μs. This reduces the 1300 Hz signal by approximately 3 dB relative to the 2600 Hz signal after external filtering.

The data rate of 1300 baud is slightly faster than the 1200 baud line receive rate, allowing incoming data from the line to be transferred simultaneously (via the microprocessor) to tape.

The TFSKIN input accepts the previously filtered and squared data from the tape recorder. The demodulator uses the fact that the modulated data is in phase with clock to regenerate the clock from the data. This permits a wide tolerance on replay speeds. A carrier detect circuit is included which sets the TDCD flag to '1' if carrier (1300 Hz or 2600 Hz) is valid for 100 ms. If carrier is lost for 100 ms the TDCD flag is reset to '0'. This flag may be read by the microprocessor to determine when to enable the tape receiver by setting TRXEN to '1'.

If TRXEN is set, then on detection of a start bit (LOW) data is shifted into the tape receive shift register by the clock which has been extracted from the data. After ten clocks, the contents of the shift register are transferred to the receive holding register. At the same time the complement of the STOP bit is loaded into the TFERR latch, the results of the parity calculation loaded into the TPERR latch, and TRXRDY is set to '1'. The TRXRDY flag is read by the microprocessor to identify when valid data is in the holding register and is reset to '0' when the holding register (R5) is read.

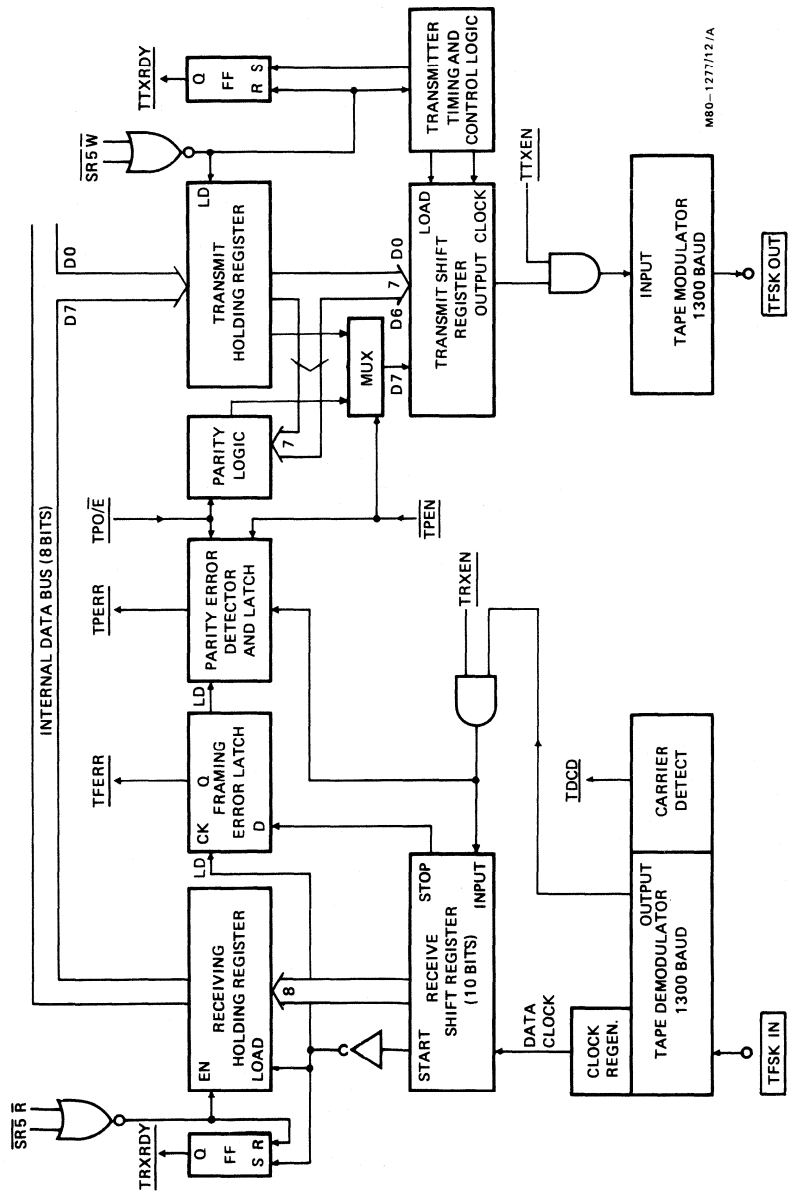


Fig.12 Tape section block diagram

IBUS A receiver and IBUS B receiver/transmitter (see Fig.13)

Associated registers:

Receiver A (2 bytes)	–	R10	– read only
Receiver B (2 bytes)	–	R11	– read only
Transmitter B (2 bytes)	–	R11	– write only

Associated flags in other registers:

IBRXRDY	–	D1	–	R0 (status)	–	valid data available in receiver B holding register
IBTXRDY	–	D0	–	R0 (status)	–	transmitter B holding register ready to accept new data
IARXRDY	–	D1	–	R1 (status)	–	valid data available in receiver A holding register
CLCK IN/$\overline{\text{OUT}}$	–	D1	–	R3 (command)	–	input/output control for 62.5 kHz pin
$\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A	–	D0	–	R3 (command)	–	3-line/2-line control for IBUS A receiver.

Associated pins:

$\overline{\text{DATA}}$ A	– input	–	receiver A data input
DLIM A/$\overline{\text{DLEN}}$ A	– input	–	receiver A data clock or bus enable signal
$\overline{\text{DATA}}$ B	– I/O	–	receiver B data input/transmitter B data output
DLIM B	– I/O	–	receiver B data clock input/transmitter B data clock output
$\overline{\text{DLEN}}$ B	– I/O	–	receiver B bus enable input/transmitter B bus enable output
IBCLCK	– I/O	–	62.5 kHz clock input/output

Operation

All three IBUS circuits (receiver A, receiver B, and transmitter B) are capable of handling variable length codes from 1 to 12 bits. (In fact 15 bits can be transmitted 12 being data the rest being trailing zero's, and 15 bits may be received but only the last 12 being retained). Each of the three circuits have two 8-bit registers which are accessed by two successive read or write operations to the same address. There is a pointer for each pair of registers which selects the first or second byte. The pointers act in a bistable fashion with each access and are reset to point to the first byte with power on, D5 set in R3, or by reading either of the status registers R0 and R1. The two bytes of data in each holding register contain 12 bits of message, and 4-bits which specify the word length of message. For the transmitter the word length is used to generate the correct number of data clocks, for the receivers it may be used to identify the source of the message, or to establish that the message was a valid length.

The contents of each receiver register pair is organised as:

1st byte	D7	D6	D5	D4	D3	D2	D1	D0
RXA – R10A RXB – R11A	L – 4	L – 5	L – 6	L – 7	L – 8	L – 9	L – 10	L – 11

2nd byte	D7	D6	D5	D4	D3	D2	D1	D0
RXA – R10B RXB – R11B	Word length MSB	Word length	Word length	Word length LSB	L	L – 1	L – 2	L – 3

Where L, L – 1 etc. means last data bit received, last minus one etc.

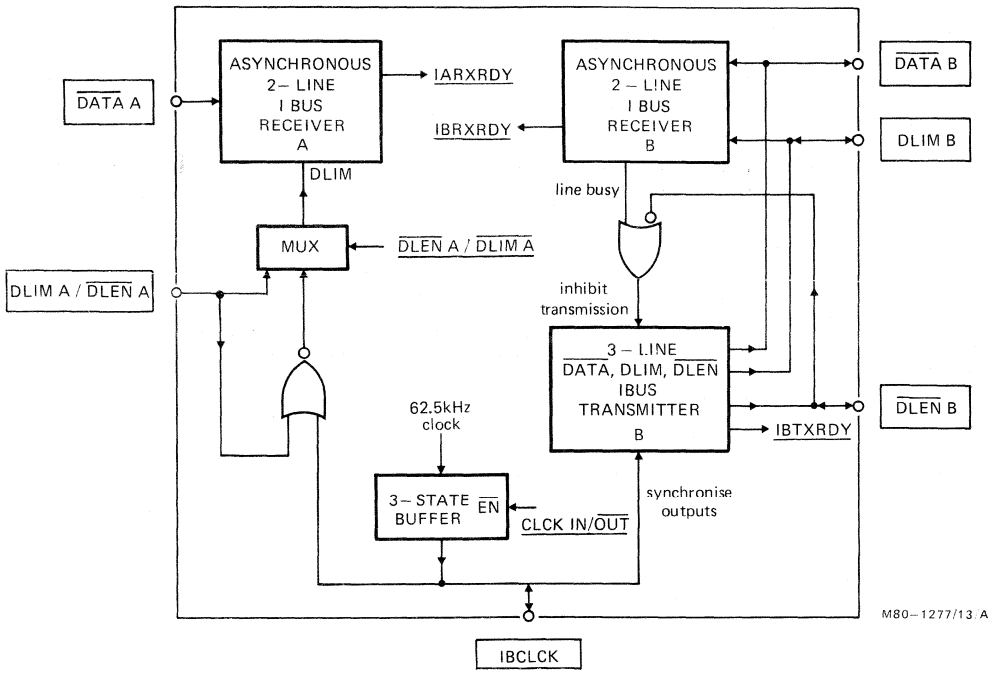


Fig. 13 IBUS block diagram

For the transmitter the register pair is organised as:

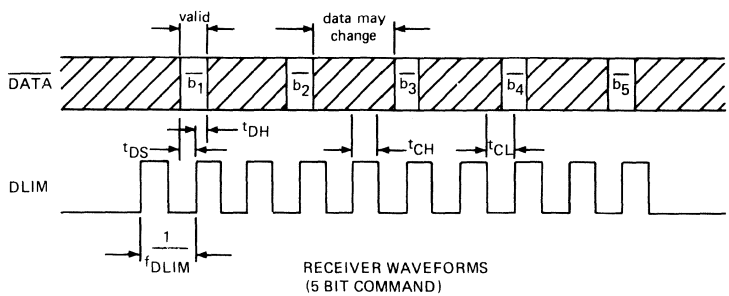
	D7	D6	D5	D4	D3	D2	D1	D0
1st byte								
TXB – R11A	8	7	6	5	4	3	2	1

	D7	D6	D5	D4	D3	D2	D1	D0
2nd byte								
TXB – R11B	Word length MSB	Word length	Word length	Word length LSB	12	11	10	9

Where 1, 2, etc. means first data bit transmitted, second data bit transmitted, etc.

IARXRDY or IBRXRDY (D1 in status registers R1 and R0) are set when a message has been received by RXA or RXB respectively. These flags also inhibit the receive holding registers from being overwritten by subsequent messages until the holding registers have been read. Reading a holding register pair will reset the relevant IARXRDY or IBRXRDY flags.

Transmitter B is initiated by writing two bytes to the transmit holding register (R11). This sets IBTXRDY to '0'. The DLIM line is sampled to detect the line busy state, and when the line is free a time out starts. If further DLIM's are detected before the end of the time out period the time out is reset and the sequence will begin again. When the time out has been completed the contents of the holding register are transferred to the output shift register and word length counter. The data and correct number of data clocks are then transmitted, at the completion of which IBTXRDY is returned to a '1'. New data should not be written to the transmit holding register (R11) while IBTXRDY = '0'. If the line is busy when a transmission is requested, the transmission will not start until 300 – 330 μs after the line becomes free (last DLIM).
Receiver B is inhibited from receiving data transmitted by transmitter B.
Receiver A may operated either as a two line receiver with $\overline{\text{DATA}}$ and DLIM, or as a three line $\overline{\text{DATA}}$, $\overline{\text{DLEN}}$ and CLK receiver. DLIM A/$\overline{\text{DLEN}}$ A use the same pin, the function of which is selected by the $\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A command D0, register R3 (command).
The 62.5 kHz clock (pin IBCLCK) may be used either as an input for receiver A (as described above), or to synchronise transmitter B outputs, or as an output synchronous with transmitter B. The function is selected by CLCK IN/$\overline{\text{OUT}}$ command D1 in R3



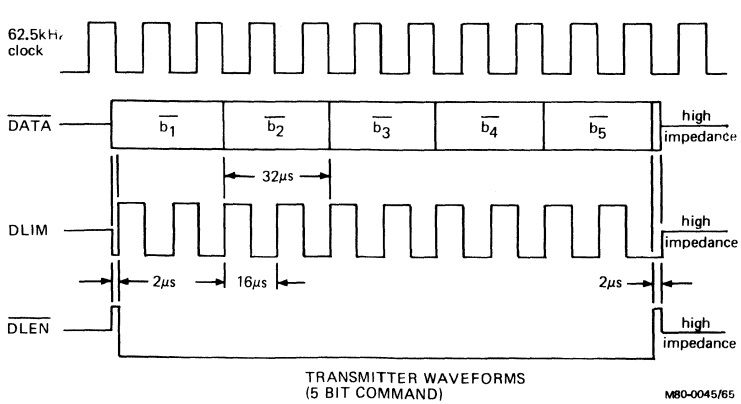


Fig. 14 IBUS waveforms

PORT A

Associated register: R6 – bits 0 to 4 – read/write

Associated pins: PA0 to PA4

Operation

This is a 5-bit general purpose input/output port. The outputs are latched and are open drain up to nominal 12 V.

The latches may be accessed by the microprocessor via BUS D0 to D7 by a read or write sequence to register R6. If any pin of the port is used as an input then its output latch must first be written with a '1'. This allows the external circuit to control the pin. The state of the pins may be read by the microprocessor by reading R6. If the supply to the open drain outputs is turned on before the V_{DD} supply to the IC, then the PORT must first be cleared by writing 1's to the output latch before operation.

PORT A might typically be used in viewdata mode as an interface to a non-volatile memory in which telephone and password numbers may be stored.

PORT B

Associated register: R7 – bits 0 to 3 – read/write

Associated pins: PB0 to PB3

Operation

This is a 4-bit general purpose input/output port. It behaves in exactly the same way as PORT A except that access is by addressing R7, and that outputs PB1 to PB3 are open drain to nominal 5 V. PB0 is open drain to nominal 12 V, and might typically be used in combined teletext/viewdata applications to control the Picture On function.

APPENDIX
Register map

	D7	D6	D5	D4	D3	D2	D1	D0	
R0	LTXRDY R	LRXRDY R	LDCD R	LFERR R	LPERR R	LIDCD R	IBRXRDY R	IBTXRDY R	STATUS REGISTER 0
R1	TTXRDY R	TRXRDY R	TDCD R	TFERR R	TPERR R		IARXRDY R		STATUS REGISTER 1
R2	LPO/$\overline{E}$ R/W	$\overline{\text{LPEN}}$ R/W	$\overline{75}$/1200 R/W		TPO/$\overline{E}$ R/W	$\overline{\text{TPEN}}$ R/W			MODE REGISTER
R3	LRXEN R/W	LTXEN R/W	RESET R/W	LDBEN R/W	TRXEN R/W	TTXEN R/W	CLCK IN/$\overline{\text{OUT}}$ R/W	$\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A R/W	COMMAND REGISTER
R4 R	PARITY OR B8 (R)	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	LINE RECEIVE HOLDING REGISTER
R4 W	PARITY OR B8 (W)	B7 W	B6 W	B5 W	B4 W	B3 W	B2 W	B1 W	LINE TRANSMIT HOLDING REGISTER
R5 R	PARITY OR B8 (R)	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	TAPE RECEIVE HOLDING REGISTER
R5 W	PARITY OR B8 (W)	B7 W	B6 W	B5 W	B4 W	B3 W	B2 W	B1 W	TAPE TRANSMIT HOLDING REGISTER
R6				PA4 R/W	PA3 R/W	PA2 R/W	PA1 R/W	PA0 R/W	PORT A
R7					PB3 R/W	PB2 R/W	PB1 R/W	PB0 R/W	PORT B
R8	UK/$\overline{\text{EUR}}$ R/W	60s TIMER R/W	DIAL GO R/W	1.5s TIMER R/W	DI 3 W	DI 2 W	DI 1 W	DI 0 W	DIAL CONTROL AND TIMING REGISTER
R10 A R10 B	B8 R — WL3 R	B7 R — WL2 R	B6 R — WL1 R	B5 R — WL0 R	B4 R — B12 R	B3 R — B11 R	B2 R — B10 R	B1 R — B9 R	IBUS A REGISTERS

APPENDIX

Register map (continued)

	D7	D6	D5	D4	D3	D2	D1	D0	
R11 A	B8 R/W	B7 R/W	B6 R/W	B5 R/W	B4 R/W	B3 R/W	B2 R/W	B1 R/W	IBUS B REGISTERS
	—	—	—	—	—	—	—	—	
R11 B	WL3 R/W	WL2 R/W	WL1 R/W	WL0 R/W	B12 R/W	B11 R/W	B10 R/W	B9 R/W	

NOTE R9 is unused.

For details of bit movement in R10 and R11 see discussion of IBUS operation. A mnemonic list for use with this register map and Fig.1b is given on the next page.

MNEMONIC LIST

ALE	address latch enable from microprocessor
CLCK IN/$\overline{\text{OUT}}$	input/output control for 62.5 kHz clock pin
CPNTR	pointer signal for two byte registers
$\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A	three line/two line control for IBUS A receiver
DON	dial off normal relay control for dialling
IMP	impulsing relay control for dialling
IARXRDY	IBUS A receiver ready — data available
IBRXRDY	IBUS B receiver ready — data available
IBTXRDY	IBUS B transmitter ready — previous transmission complete
LDBEN	line demodulator output buffer enable
LDCD	line data carrier detected
LFERR	line receiver framing error — received stop bit not HIGH
LIDCD	line instantaneous data carrier detect
$\overline{\text{LPEN}}$	line parity enable command
LPERR	line receiver parity error flag
LPO/$\overline{\text{E}}$	line parity odd/even command
LRXEN	line receiver enable
LRXRDY	line receiver ready — data available
LTXEN	line transmitter and modulator enable
LTXRDY	line transmitter ready — transmit holding register empty
$\overline{\text{SR}}$n	select register 'n'
TDCD	tape data carrier detected
TFERR	tape receiver framing error — received stop bit not HIGH
$\overline{\text{TPEN}}$	tape parity enable command
TPERR	tape receiver parity error flag
TPO/$\overline{\text{E}}$	tape parity odd/even command
TRXEN	tape receiver enable
TRXRDY	tape receiver ready — data available
TTXEN	tape transmitter enable
TTXRDY	tape transmitter ready — transmit holding register empty
UK/$\overline{\text{EUR}}$	impulsing ratio control for UK and European standards
$\overline{75}$/1200	baud rate selection command for line modulator and line transmit shift register

TELETEXT VIDEO PROCESSOR

GENERAL DESCRIPTION

The SAA5230 is a bipolar integrated circuit intended as a successor to the SAA5030. It extracts Teletext Data from the video signal, regenerates Teletext Clock and synchronizes the text display to the television syncs. The integrated circuit is intended to work in conjunction with CCT (Computer Controlled Teletext), EUROM or other compatible devices.

Features

- Adaptive data slicer
- Data clock regenerator
- Adaptive sync separator, horizontal phase detector and 6 MHz VCO forming display phase locked loop (PLL)

QUICK REFERENCE DATA

Supply voltage (pin 16)	V_{CC}	typ.	12	V
Supply current (pin 16)	I_{CC}	typ.	70	mA
Video input amplitude (pin 27) (peak-to-peak value)				
pin 2 LOW	$V_{27\text{-}13(p\text{-}p)}$	typ.	1	V
pin 2 HIGH	$V_{27\text{-}13(p\text{-}p)}$	typ.	2,5	V
Storage temperature range	T_{stg}		−20 to + 125	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

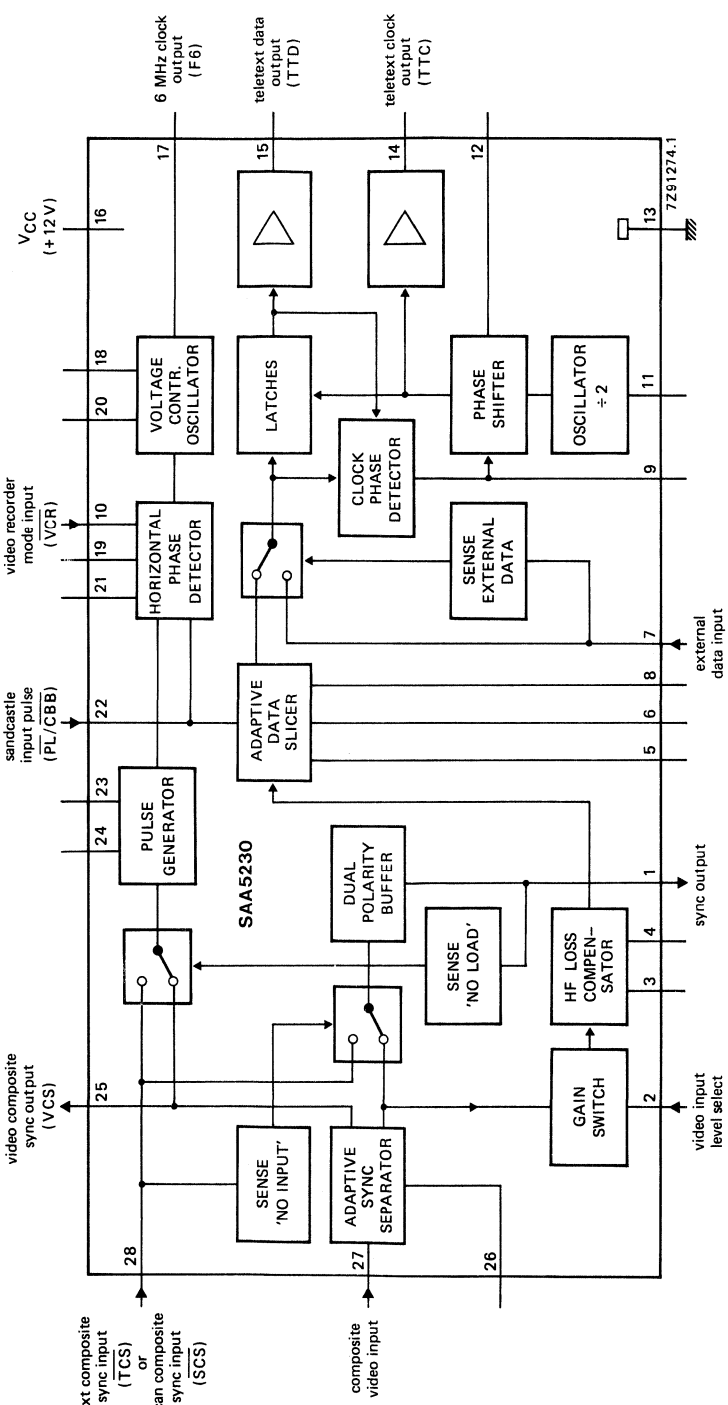


Fig. 1 Block diagram.

PINNING

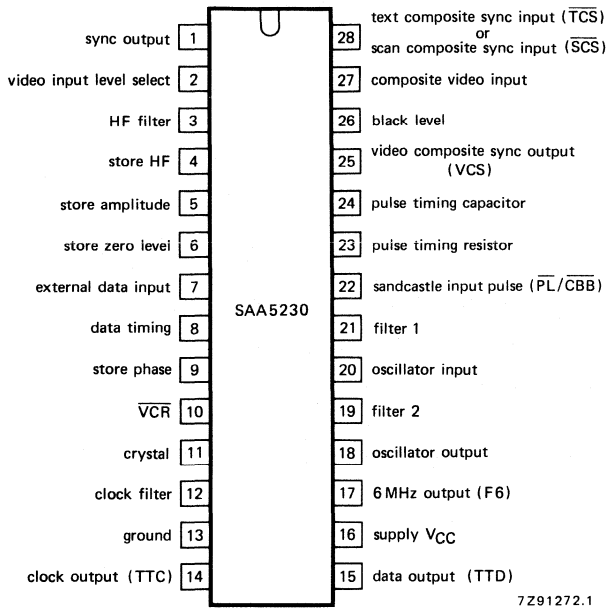


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 16)	V_{CC}	max. 13,2	V
Storage temperature range	T_{stg}	−20 to + 125	°C
Operating ambient temperature	T_{amb}	0 to + 70	°C ←

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C with external components as shown in Fig. 3a or Fig. 3b unless otherwise stated.

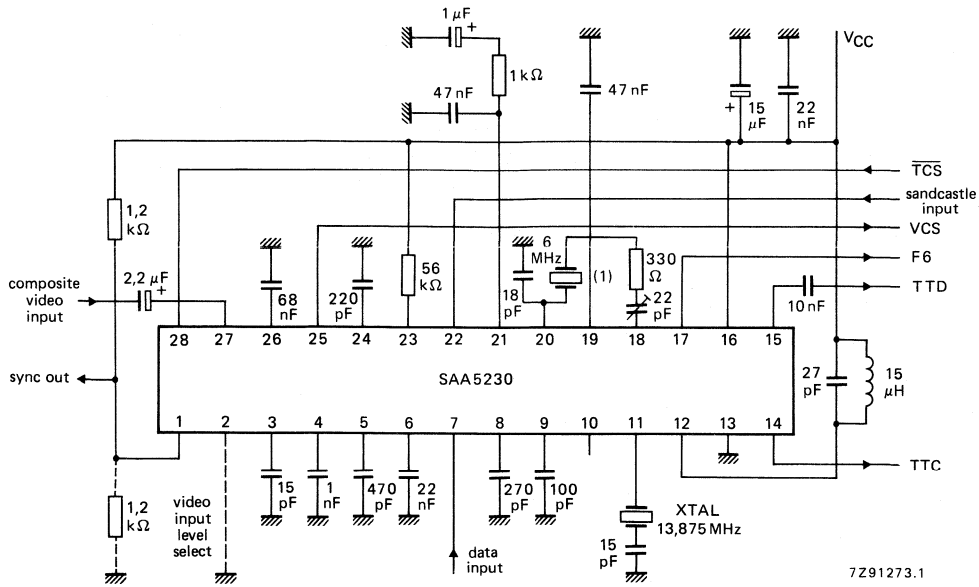
parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{CC}	10,8	12,0	13,2	V
Supply current	I_{CC}	–	70	–	mA
Video input and sync separator					
Video input amplitude (sync to white) (peak-to-peak value)					
video input select level LOW (pin 2)	$V_{27\text{-}13(p\text{-}p)}$	0,7	1	1,4	V
video input select level HIGH (pin 2)	$V_{27\text{-}13(p\text{-}p)}$	1,75	2,5	3,5	V
Source impedance	$\lvert Z_s \rvert$	–	–	250	Ω
Sync amplitude (peak-to-peak value)	$V_{27\text{-}13(p\text{-}p)}$	0,1	–	1	V
Video input level select					
Input voltage LOW	$V_{2\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{2\text{-}13}$	2,0	–	5,5	V
Input current LOW	I_2	0	–	−150	μA
Input current HIGH	I_2	0	–	1	mA
Text composite sync input ($\overline{TCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{28\text{-}13}$	2,0	–	7,0	V
Scan composite sync input ($\overline{SCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	1,5	V
Input voltage HIGH	$V_{28\text{-}13}$	3,5	–	7,0	V
Select video sync from pin 1					
Input current (pin 28)					
at V_I = 0 to 7 V	I_{28}	−40	−70	−100	μA
at V_I = 10 V to V_{CC}	I_{28}	−5	–	+ 5	μA
Video composite sync output (VCS)					
Output voltage LOW	$V_{25\text{-}13}$	0	–	0,4	V
Output voltage HIGH	$V_{25\text{-}13}$	2,4	–	5,5	V
D.C. output current LOW	I_{25}	–	–	0,5	mA
D.C. output current HIGH	I_{25}	–	–	−1,5	mA
Sync separator delay time	t_d	–	0,35	–	μs

parameter	symbol	min.	typ.	max.	unit
Dual polarity buffer output					
$\overline{TCS}$ amplitude (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	–	0,45	–	V
Video sync amplitude (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	–	–	1	V
Output current	I_1	–3	–	+ 3	mA
D.C. output voltage					
R_L to ground (0 V)	$V_{1\text{-}13}$	–	1,4	–	V
R_L to V_{CC} (12 V)	$V_{1\text{-}13}$	–	10,1	–	V
Sandcastle input pulse ($\overline{PL}$/$\overline{CBB}$)					
Phase lock pulse (PL)					
PL on (LOW)	$V_{22\text{-}13}$	0	–	3	V
PL off (HIGH)	$V_{22\text{-}13}$	3,9	–	5,5	V
Blanking pulse (CBB)					
CBB on (LOW)	$V_{22\text{-}13}$	0	–	0,5	V
CBB off (HIGH)	$V_{22\text{-}13}$	1,0	–	5,5	V
Input current	I_{22}	–10	–	+ 10	μA
Phase locked loop (PLL)					
Phase detector timing					
Pulse duration using composite video	t_p	–	2	–	μs
using scan composite sync	t_p	–	3	–	μs
time PL must be LOW to make VCO run-free	t_L	100	–	–	μs
6 MHz clock output (F6)					
A.C. output voltage (peak-to-peak value)	$V_{17\text{-}13(p\text{-}p)}$	1	2	3	V
A.C. and d.c. output voltage range	$V_{17\text{-}13(max)}$	4	–	8,5	V
Rise and fall time	t_r; t_f	20	–	40	ns
Load capacitance	$C_{17\text{-}13}$	–	–	40	pF
Video recorder mode input ($\overline{VCR}$)					
VCR-mode on (LOW)	$V_{10\text{-}13}$	0	–	0,8	V
VCR-mode off (HIGH)	$V_{10\text{-}13}$	2,0	–	V_{CC}	V
Input current	I_{10}	–10	–	+ 10	μA

CHARACTERISTICS (continued)

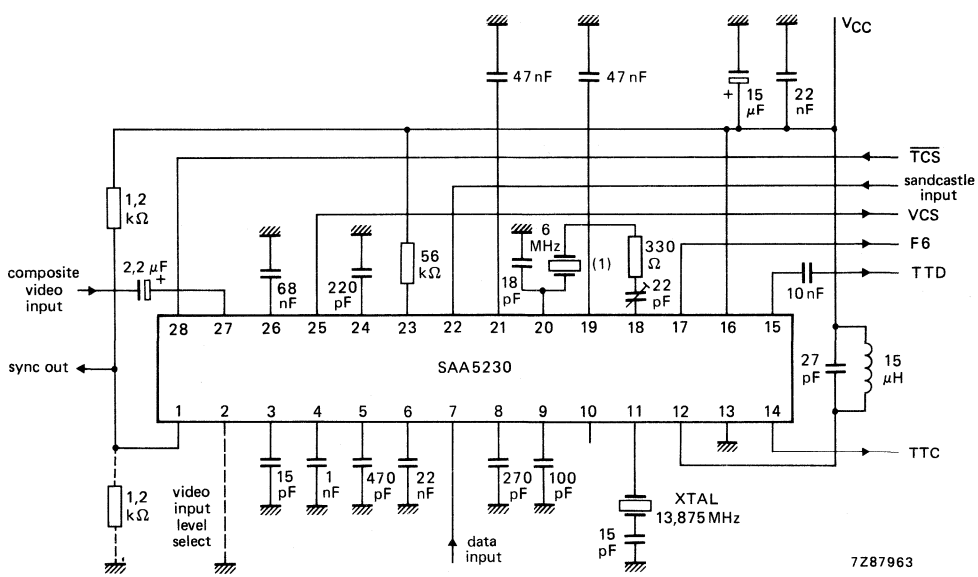
parameter	symbol	min.	typ.	max.	unit
Data slicer					
Data amplitude of video input (pin 27)					
video input level select LOW (pin 2)	$V_{27\text{-}13}$	0,30	0,46	0,70	V
video input level select HIGH (pin 2)	$V_{27\text{-}13}$	0,75	1,15	1,75	V
Teletext clock output					
A.C. output voltage (peak-to-peak value)	$V_{14\text{-}13(p\text{-}p)}$	2,5	3,5	4,5	V
D.C. output voltage (centre)	$V_{14\text{-}13}$	–	4	–	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	$t_r; t_f$	20	30	45	ns
Delay of falling edge relative to other edges of TTD	t_d	−20	0	+ 20	ns
Teletext data output					
A.C. output voltage (peak-to-peak value)	$V_{15\text{-}13(p\text{-}p)}$	2,5	3,5	4,5	V
D.C. output voltage (centre)	$V_{15\text{-}13}$	–	4	–	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	$t_r; t_f$	20	30	45	ns

APPLICATION INFORMATION



(1) Ceramic resonator e.g. Kyocera KBR 6,0 M. Adjust the free-running frequency to 6010 kHz ± 5 kHz.

Fig. 3a Application circuit using ceramic resonator in PLL.



(1) Quartz crystal e.g. catalogue number 4322 143 04101. Adjust the free-running frequency to 6000,2 kHz ± 0,2 kHz.

Fig. 3b Application circuit using quartz crystal in PLL.

APPLICATION INFORMATION (continued)

Component specifications

Specifications of some external components in Fig. 3a and Fig. 3b.

Ceramic resonator (preferred type KBR 6,0 M, Kyocera; Fig. 3a)

Load resonance frequency (f) 6 MHz; adjustment tolerance ± 0,5%
Load capacitance (C_L) 20 pF
Temperature range (T) −20 to + 70 °C; frequency tolerance ± 0,3% max.
Resonance resistance (R_r) 6 Ω typ.
Motional capacitance (C_1) 9 pF typ.
Static parallel capacitance (C_o) 60 pF typ.
Ageing (10 years) f ± 0,3% max.

Quartz crystal

Load resonance frequency (f) 13,875 MHz; adjustment tolerance ± $40 \cdot 10^{-6}$
Load capacitance (C_L) 20 pF
Temperature range (T) −20 to + 70 °C; frequency tolerance ± $30 \cdot 10^{-6}$ max.
Resonance resistance (R_r) 10 Ω typ. 60 Ω max.
Motional capacitance (C_1) 19 fF typ.
Static parallel capacitance (C_o) 5 pF typ.

Fixed inductance

Inductance (L) 15 μH ± 20%
Quality factor (Q) 20 min.

Quartz crystal (preferred type catalogue number 4322 143 04101; Fig. 3b)

Load resonance frequency (f) 6 MHz; adjustment tolerance ± $40 \cdot 10^{-6}$
Load capacitance (C_L) 20 pF
Temperature range (T) −20 to + 70 °C; frequency tolerance ± $30 \cdot 10^{-6}$ max.
Resonance resistance (R_r) 60 Ω
Motional capacitance (C_1) 28 fF typ.
Static parallel capacitance (C_o) 7 pF typ.

The function is quoted against the corresponding pin number.

1. **Synch output to TV**

   Output with dual polarity buffer, a load resistor to 0 V or + 12 V selects positive-going or negative-going syncs.

2. **Video input level select**

   When this pin is LOW a 1 V video input level is selected. When the pin is not connected it floats HIGH selecting a 2,5 V video input level.

3. **HF filter**

   The video signal for the h.f.-loss compensator is filtered by a 15 pF capacitor connected to this pin.

4. **Store h.f.**

   The h.f. amplitude is stored by a 1 nF capacitor connected to this pin.

5. **Store amplitude**

   The amplitude for the adaptive data slicer is stored by a 470 pF capacitor connected to this pin.

6. **Store zero level**

   The zero level for the adaptive data slicer is stored by a 22 nF capacitor connected to this pin.

7. **External data input**

   Current input for sliced teletext data from external device.
   Active HIGH level (current), low impedance input.

8. **Data timing**

   A 270 pF capacitor is connected to this pin for timing of the adaptive data slicer.

9. **Store phase**

   The output signal from the clock phase detector is stored by a 100 pF capacitor connected to this pin.

10. **Video tape recorder mode ($\overline{\text{VCR}}$)**

    Signal input to command PLL into short time constant mode. Not used in application circuit Fig. 3a or Fig. 3b.

11. **Crystal**

    A 13,875 MHz crystal, 2 x data rate, connected in series with a 15 pF capacitor is applied via this pin to the oscillator and divide-by-two to provide the 6,9375 MHz clock signal.

12. **Clock filter**

    A filter for the 6,9375 MHz clock signal is connected to this pin.

13. **Ground (0 V)**

14. **Teletext clock output (TTC)**

    Clock output for CCT (Computer Controlled Teletext).

APPLICATION INFORMATION (continued)

15. **Teletext data output (TTD)**

Data output for CCT.

16. **Supply voltage V_{CC} (+ 12 V typ.)**

17. **Clock output (F6)**

6 MHz clock output for timing and sandcastle generation in CCT.

18. **Oscillator output (6 MHz)**

A series resonant circuit is connected between this pin and pin 20 to control the nominal frequency of the VCO.

19. **Filter 2**

A filter with a short time constant is connected to this pin for the horizontal phase detector. It is used in the video recorder mode and while the loop is locking up.

20. **Oscillator input (6 MHz)**

See pin 18.

21. **Filter 1**

A filter with a long time constant is connected to this pin for the horizontal phase detector.

22. **Sandcastle input pulse ($\overline{PL}/\overline{CBB}$)**

This input accepts a sandcastle waveform, which is formed from PL and CBB from the CCT. Signal timing is shown in Fig. 4.

23. **Pulse timing resistor**

The current for the pulse generator is defined by a 56 kΩ resistor connected to this pin.

24. **Pulse timing capacitor**

The timing of the pulse generator is determined by a 220 pF capacitor connected to this pin.

25. **Video composite sync output (VCS)**

This output signal is for CCT.

26. **Black level**

The black level for the adaptive sync separator is stored by a 68 nF capacitor connected to this pin.

27. **Composite video input (CVS)**

The composite video signal is input via a 2,2 μF clamping capacitor to the adaptive sync separator.

28. **Text composite sync input ($\overline{\text{TCS}}$)/Scan composite sync input ($\overline{\text{SCS}}$)**

$\overline{\text{TCS}}$ is input from CCT or $\overline{\text{SCS}}$ from external sync circuit. $\overline{\text{SCS}}$ is expected when there is no load resistor at pin 1. If pin 28 is not connected the sync output on pin 1 will be the composite video input at pin 27, internally buffered.

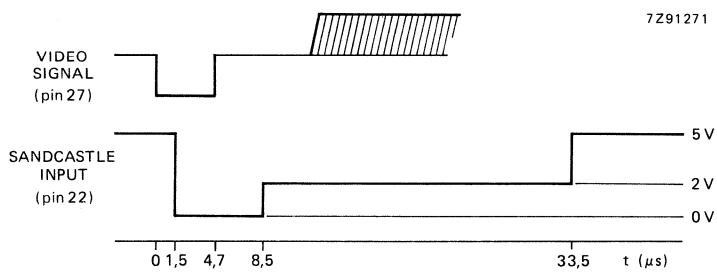


Fig. 4 Sandcastle waveform and timing.

DATALINE SLICER

The SAA5235 is a bipolar integrated circuit for dataline receivers. It extracts the dataline signal from the video signal and regenerates the dataline clock. It also provides signals for the dataline decoder.

Features

- Adaptive dataline slicer
- Dataline clock regenerator
- Buffered clock and data outputs
- Buffered composite sync output
- Gain switch for the video input signal

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 16)	V_{CC}	10,8	12	13,2	V
Supply current at V_{CC} = 12 V	I_{CC}	–	70	–	mA
Composite video amplitude					
pin 2 LOW	$V_{27(p\text{-}p)}$	–	1	–	V
pin 2 floating	$V_{27(p\text{-}p)}$	–	2,5	–	V
Storage temperature range	T_{stg}	−20	–	+ 125	°C
Operating ambient temperature	T_{amb}	0	–	+ 70	°C

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT-117).

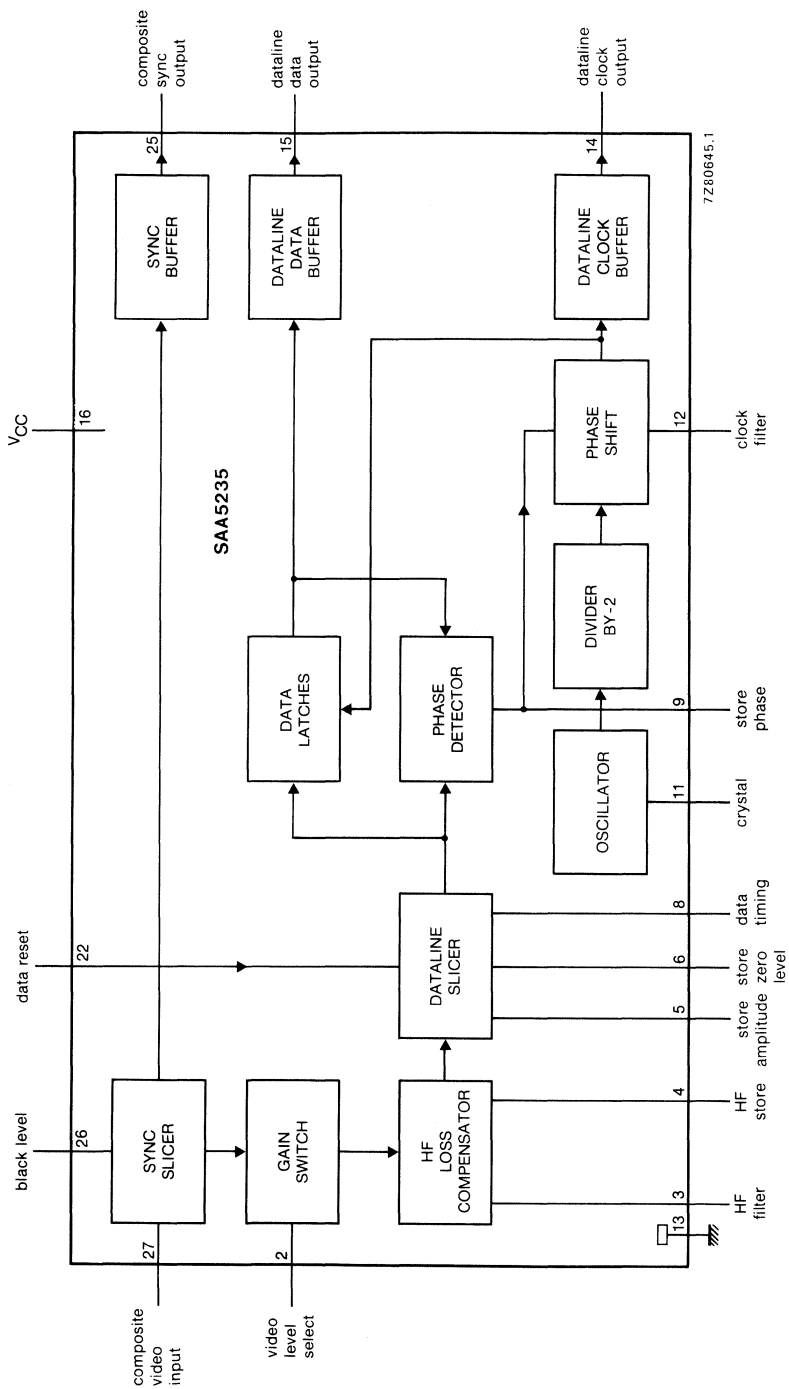


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 16)	V_{CC}	–	–	13,2	V
Storage temperature range	T_{stg}	−20	–	125	°C
Operating ambient temperature	T_{amb}	0	–	70	°C

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; with external components as shown in Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 16)	V_{CC}	10,8	12,0	13,2	V
Supply current	I_{CC}	–	70	–	mA
Video input and sync separator					
Composite video input (CV)					
Level select input (pin 2) LOW	$V_{27\text{-}13(p\text{-}p)}$	0,7	1	1,4	V
Level select input (pin 2) HIGH	$V_{27\text{-}13(p\text{-}p)}$	1,75	2,5	3,5	V
Source impedance	$\lvert Z_s \rvert$	–	–	250	Ω
Sync amplitude	$V_{27\text{-}13(p\text{-}p)}$	0,1	–	1	V
Video level select					
Input voltage					
LOW	$V_{2\text{-}13}$	0	–	0,8	V
HIGH	$V_{2\text{-}13}$	2,0	–	5,5	V
Input current					
LOW	I_2	0	–	−150	μA
HIGH	I_2	0	–	1	mA
Video composite sync output (VCS)					
Output voltage					
LOW	$V_{25\text{-}13}$	0	–	0,4	V
HIGH	$V_{25\text{-}13}$	2,4	–	5,5	V
Sync separator delay time	t_d	–	0,35	–	μs
Data reset input (DAR)					
Input voltage					
LOW (DAR on)	$V_{22\text{-}13}$	0	–	0,5	V
HIGH (DAR off)	$V_{22\text{-}13}$	1,0	–	5,5	V
Input current	I_{22}	−10	–	10	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Dataline slicer					
Dataline amplitude (pin 27)					
Video select voltage (pin 2) LOW	$V_{27\text{-}13(p\text{-}p)}$	0,3	0,46	0,7	V
Video select (pin 2) FLOATING	$V_{27\text{-}13(p\text{-}p)}$	0,75	1,15	1,75	V
Dataline clock output (DLCL)					
A.C. output voltage	$V_{14\text{-}13(p\text{-}p)}$	2,5	3,5	4,5	V
Output voltage (d.c.) centre	$V_{14\text{-}13}$	–	4,0	–	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r, t_f	20	30	45	ns
Delay of falling edge relative to edges of DLD	t_d	–20	–	20	ns
Dataline data output (DLD)					
A.C. output voltage	$V_{15\text{-}13(p\text{-}p)}$	2,5	3,5	4,5	V
Output voltage (d.c.) centre	$V_{15\text{-}13}$	–	4,0	–	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r, t_f	20	30	45	ns

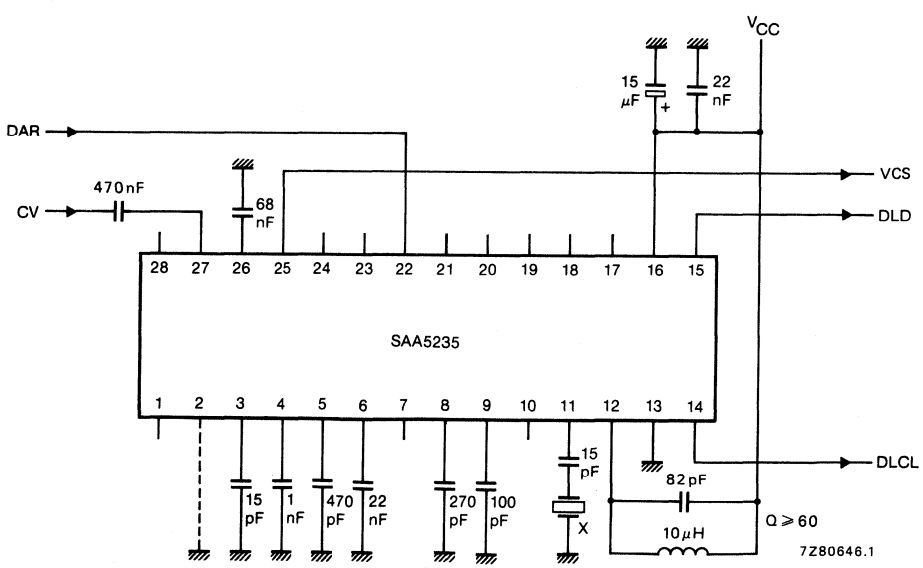


Fig. 2 Application circuit; crystal X; f = 10,000 MHz.

APPLICATION DATA

Composite video input CV (pin 27)

The composite video has to be fed into this input via a clamp capacitor. The input amplitude depends on the position of the gain switch at pin 2.

Video gain switch (pin 2)

Low level selects 1 V video input amplitude at pin 27. With no connection pin 2 floats HIGH, selecting 2,5 V video amplitude.

Black level (pin 26)

A capacitor connected to this pin stores the black level for the adaptive sync separator.

Video composite sync output VCS (pin 25)

This pin provides a video composite sync signal for the data-line decoder.

H.F. loss compensator (pins 3 and 4)

The h.f. loss compensator needs two capacitors for operation. The capacitor at pin 3 filters the video signal for the h.f. loss compensator. The h.f. amplitude information is stored in the capacitor connected to pin 4.

Dataline slicer (pins 5, 6 and 8)

A capacitor at pin 5 stores the amplitude information for the dataline slicer. The zero-level information is stored in a capacitor connected to pin 6. The capacitor at pin 8 is necessary for timing of the dataline slicer.

Phase detector (pin 9)

The phase information which is detected from the phase detector is stored in a capacitor connected to pin 9.

Oscillator (pin 11)

The one-pin oscillator needs a 10,000 MHz crystal (2 x dataline frequency) connected to pin 11.

Phase shifter (pin 12)

A clock filter for the dataline clock of 5,000 MHz is connected to the phase shifter at pin 12.

Outputs

The dataline clock output DLCL (pin 14) and the dataline data output DLD (pin 15) provide signals for the dataline decoder.

Data reset DAR (pin 22)

The dataline slicer needs a reset signal each line, for signal timing see Fig. 3.

APPLICATION DATA (continued)

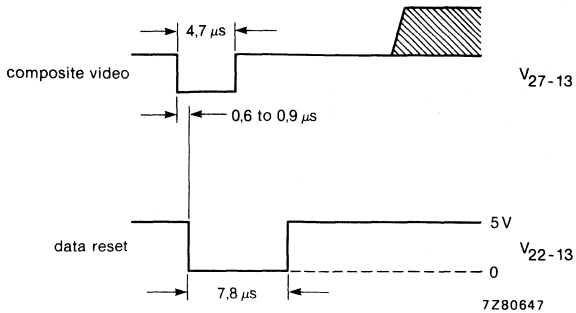


Fig. 3 Data-reset input signal timing in relation to composite video signal.

EUROPEAN COMPUTER CONTROLLED TELETEXT CIRCUIT (EURO CCT)

GENERAL DESCRIPTION

The SAA5240 is a MOS N-channel integrated circuit which performs all the digital logic functions of a 625-line World System Teletext decoder. It operates in conjunction with the teletext video processor SAA5230, standard static RAM's and is controlled via the 2-wire I²C bus. The device can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 10 character matrix
- Field flyback (lines 6 to 22), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language selection of up to three different languages
- 25th display row for software generated status messages
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Ghost row reception option (extension packets)
- Standard I²C bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets:
  SAA5240A; English, German, Swedish
  SAA5240B; Italian , German, French

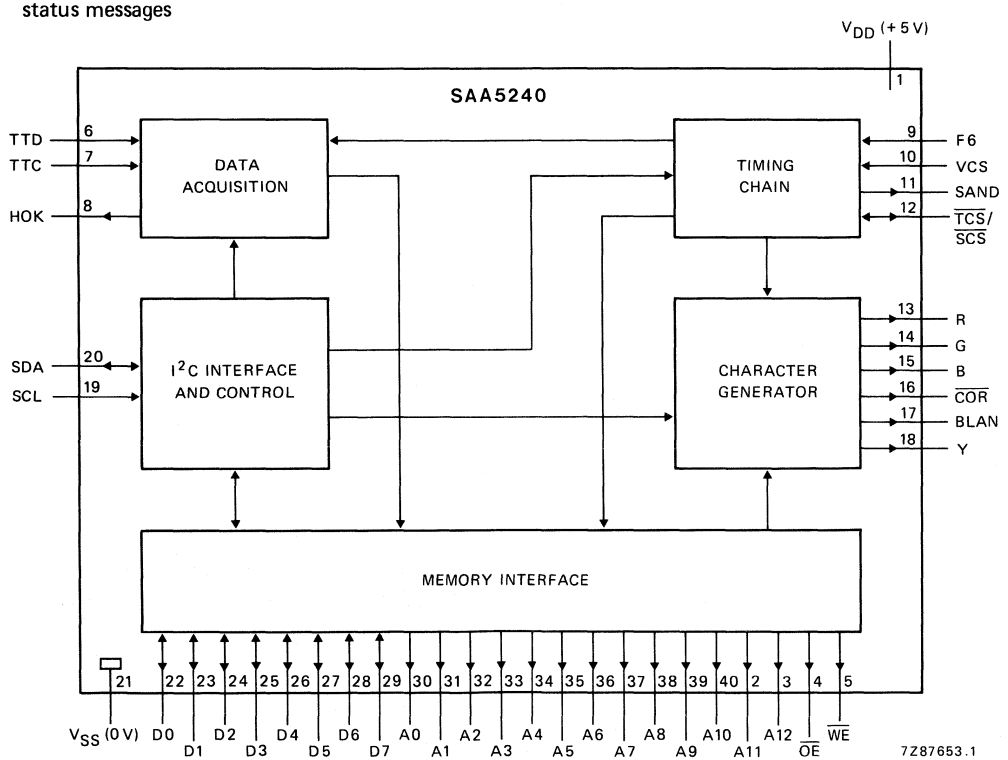


Fig. 1 Block diagram.

PACKAGE OUTLINES 40-lead DIL; plastic (SOT-129).

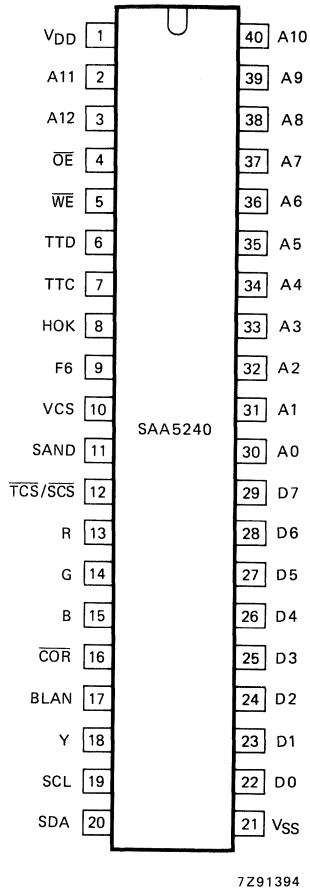


Fig. 2 Pinning diagram.

PINNING

1	V_{DD}	**Power supply**: + 5 V power supply pin.
2, 3, 40	A11, A12, A10	**Chapter Address**: three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
4	$\overline{OE}$	**Output Enable**: active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.
5	$\overline{WE}$	**Write Enable**: active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data**: input from the SAA5230 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct d.c. level following the external a.c. coupling.

7	TTC	**Teletext Clock**: 6,9375 MHz clock input from the SAA5230. It is internally a.c. coupled to an active clamp input buffer.
8	HOK	**Hamming O.K.**: an active high output signal indicating reception of a valid teletext data line with no Hamming errors in the magazine or row bytes. It is reset at line rate.
9	F6	**Character display clock**: 6 MHz clock input from the SAA5230. It is internally a.c. coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync**: input from the SAA5230 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle**: 3-level sandcastle output to the SAA5230 containing the phase locking and colour burst blanking information.
12	$\overline{\text{TCS}}/\overline{\text{SCS}}$	**Text Composite Sync/Scan Composite Sync**: as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig. 6) which is fed to the SAA5230 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Blue, Green**: these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{\text{COR}}$	**Contrast Reduction**: open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking**: open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground**: open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock**: input signal which is the I^2C bus clock from the microcontroller.
20	SDA	**Serial Data**: is the I^2C bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground**: 0 volts.
22-29	DO-D7	**8 RAM data lines**: 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address**: 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 1)	V_{DD}	−0,3 to +7,5 V
Input voltage range		
VCS, SDA, SCL, D0-D7	V_I	−0,3 to +7,5 V
TTC, TTD, F6, $\overline{TCS}/\overline{SCS}$	V_I	−0,3 to +10,0 V
Output voltage range		
SAND, A0-A12, $\overline{OE}$, $\overline{WE}$, D0-D7, SDA, HOK, R, G, B, BLAN, $\overline{COR}$, Y	V_O	−0,3 to +7,5 V
$\overline{TCS}/\overline{SCS}$	V_O	−0,3 to +10,0 V
Storage temperature range	T_{stg}	−20 to +125 °C
Operating ambient temperature range	T_{amb}	−20 to +70 °C

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 1)	I_{DD}	–	160	270	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2,0	–	7,0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
D.C. input voltage range	V_I	−0,3	–	+ 10,0	V
A.C. input voltage (peak-to-peak value) F6	$V_{I(p-p)}$	1,0	–	7,0	V
A.C. input voltage (peak-to-peak value) TTC	$V_{I(p-p)}$	1,5	–	7,0	V
Input peaks relative to 50% duty cycle	± V_P	0,2	–	3,5	V
TTC clock frequency	f_{TTC}	–	6,9375	–	MHz
F6 clock frequency	f_{F6}	–	6,0	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5,5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5,5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,5	–	10,0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 0 to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 0,4 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
at I_{OH} = 0,1 mA	V_{OH}	2,4	–	6,0	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5,5 V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	0	–	0,5	V
Output fall time between 3,0 V and 1,0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5,5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
HOK (note 9)					
Output voltage LOW at I_{OL} = 0,4 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0,2 mA	V_{OL}	0	–	0,25	V
Output voltage INTERMEDIATE at I_{OL} = ± 10 μA	V_{OI}	1,1	–	3,1	V

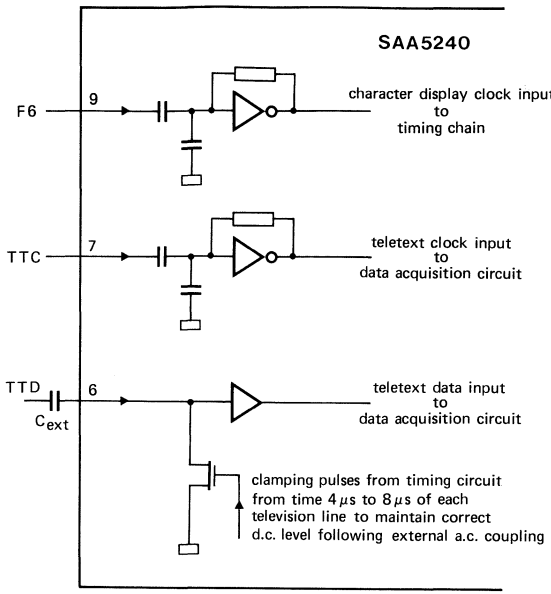
CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −10 μA	V_{OH}	4,0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0,4 V and 1,1 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 2,9 V and 4,0 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 4,0 V and 0,4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{\text{COR}}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0,4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1,0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6,0	V
Output fall time with a load resistor of 1,2 kΩ to 6 V and measured between 5,5 V and 1,5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1,2 kΩ to 6 V and measured on the falling edges at 3,5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I²C bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	170	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low to high transition	$t_{SU;STA}$	4	–	–	μs

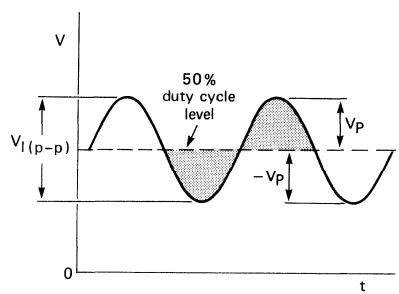
parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	500	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	500	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns

Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig. 3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable $1 \geqslant 2{,}0$ V; data stable $0 \leqslant 0{,}8$ V (see Fig. 4).
5. The TTC and F6 inputs have internal clamping diodes and are a.c. coupled (see Fig. 3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^2C bus timing see Fig. 8.
8. For details of RAM timing see Fig. 9.
9. For details of synchronization and HOK timing see Fig. 5.
10. For details of display output timing see Fig. 7.
11. The I^2C bus timings are referred to $V_{IH} = 3$ V and $V_{IL} = 1{,}5$ V. For waveforms see Fig. 8.
12. The memory interface timings are referred to $V_{IL} = 1{,}5$ V. For waveforms see Fig. 9.



(a)

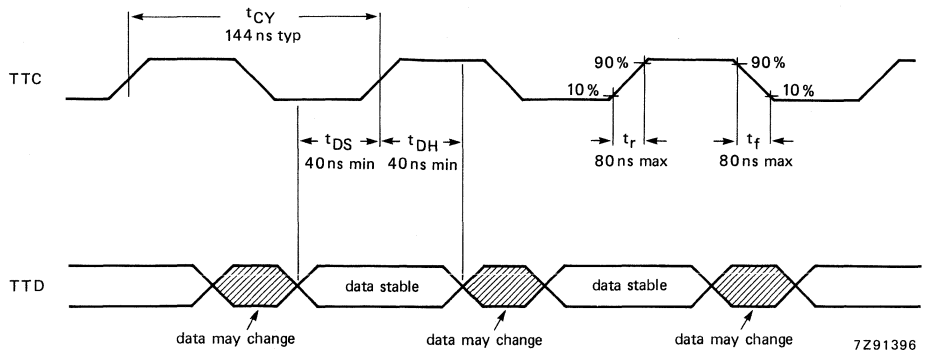


shaded regions equal in area

7Z91395

(b)

Fig. 3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is $\geqslant$ 2,0 V; 0 is $\leqslant$ 0,8 V.

Fig. 4 Teletext data input timing.

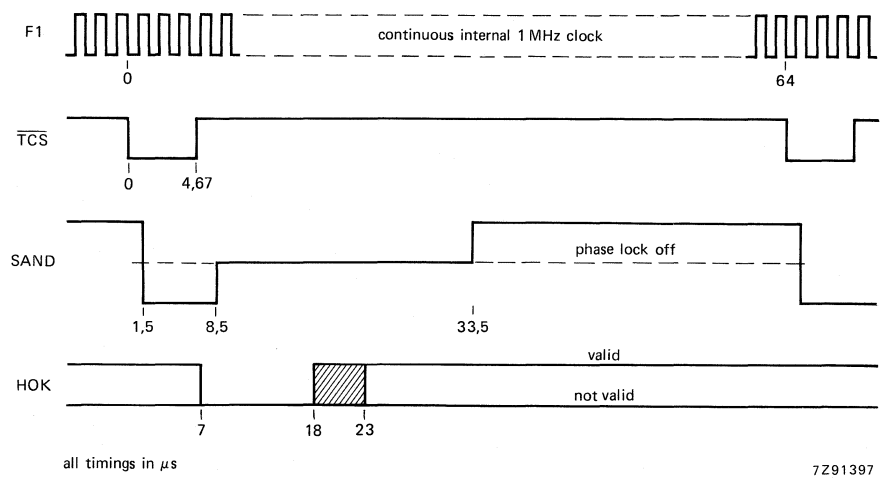
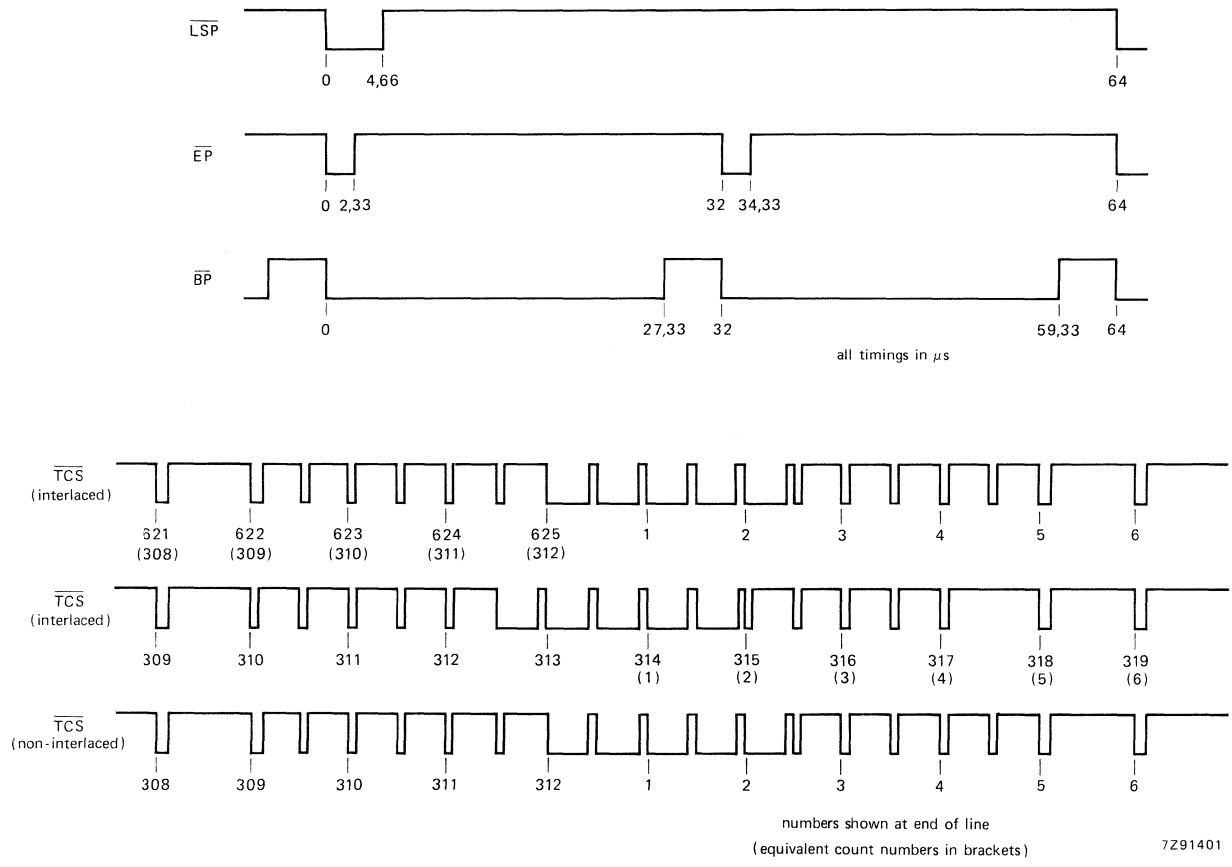


Fig. 5 Synchronization and HOK timing.



Line sync pulses ($\overline{\text{LSP}}$), equalizing pulses ($\overline{\text{EP}}$) and broad pulses ($\overline{\text{BP}}$) are combined to provide the text composite sync waveform ($\overline{\text{TCS}}$) as shown. All timings measured from falling edge of $\overline{\text{LSP}}$ with a tolerance of ± 100 ns.

Fig. 6 Composite sync waveforms.

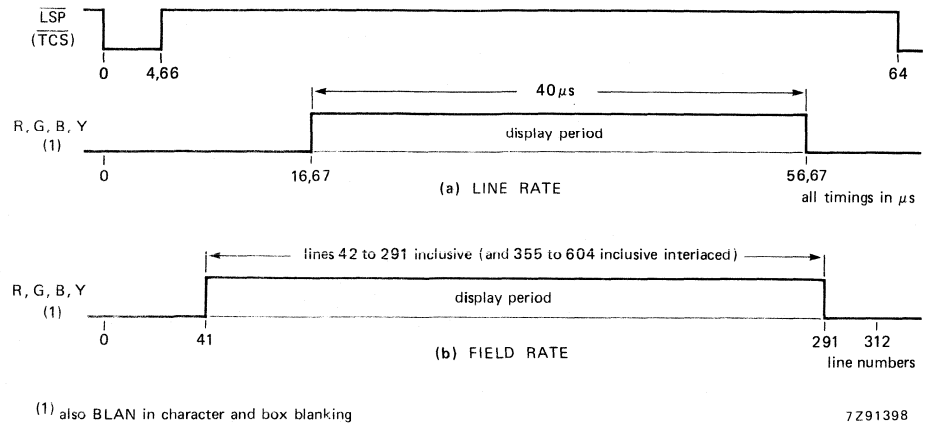


Fig. 7 Display output timing (a) line rate (b) field rate.

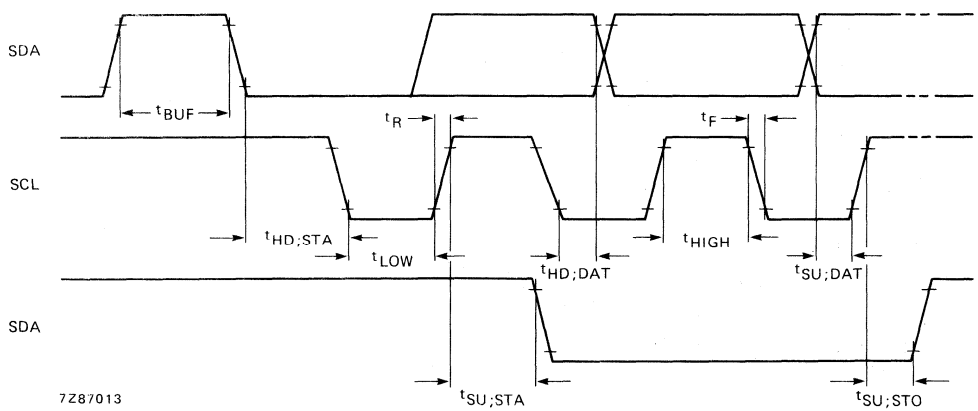


Fig. 8 I^2C bus timing.

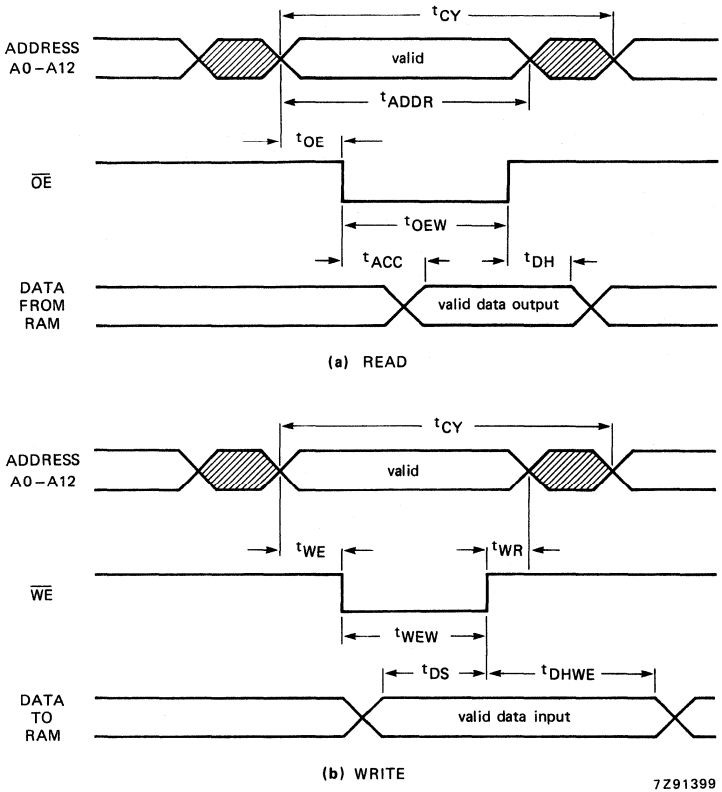
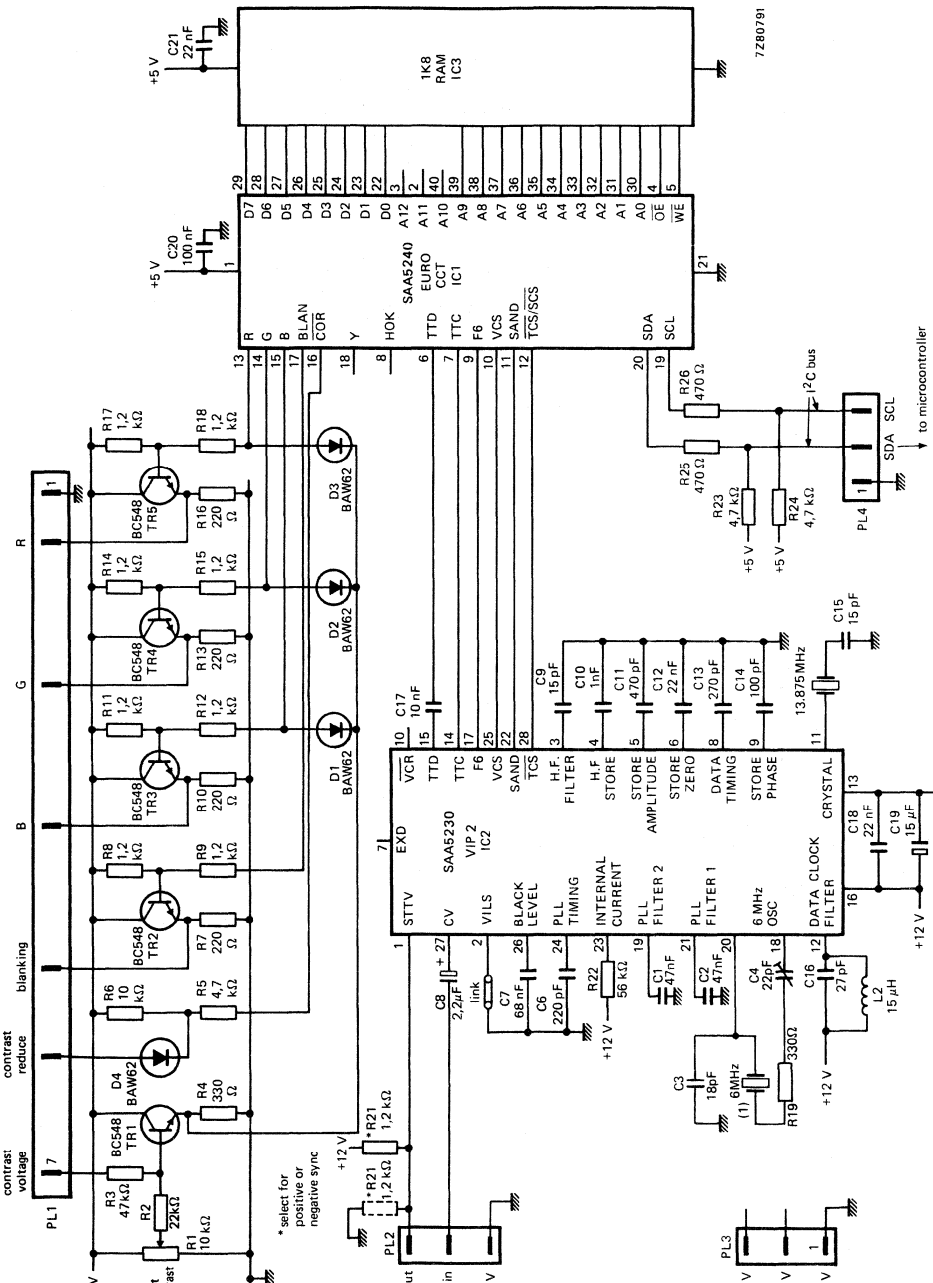


Fig. 9 Memory interface timing (a) read (b) write.

APPLICATION INFORMATION



(1) Quartz crystal e.g. catalogue number 4322 143 04101. Adjust the free-running frequency to 6000,2 kHz ± 0,2 kHz.

Fig. 10 EURO CCT based single-page decoder circuit diagram.

APPLICATION INFORMATION (continued)

EURO CCT page memory organization

The organization of a page memory is shown in Fig. 11. The EURO CCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF CCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

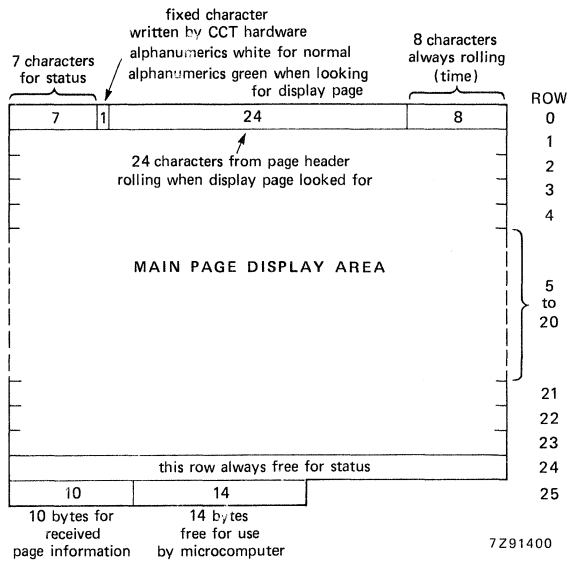


Fig. 11 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine	page number	MU	minutes units	page sub-code
PU	page units		MT	minutes tens	
PT	page tens		HU	hours units	
PBLF	page being looked for		HT	hours tens	
$\overline{\text{FOUND}}$	LOW for page has been found		C4-C14	transmitted control bits	
HAM.ER	Hamming error in corresponding byte				

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by EURO CCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

EURO CCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 EURO CCT register map

D7	D6	D5	D4	D3	D2	D1	D0		
TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	GHOST ROW ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode
–	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request address
–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
–	–	–	–	–	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash/subtitle)
STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
–	–	–	–	CLEAR MEM.	A2	A1	A0	R8	Active chapter
–	–	–	R4	R3	R2	R1	R0	R9	Active row
–	–	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11	Active data

– bit does not exist

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

APPLICATION INFORMATION (continued)

Table 2 (continued)

Where:

R1 Mode	
T0, T1	interlace/non interlace 312/313 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full channel mode
$\overline{7+P}$/8 BIT	7 bits with parity checking or 8-bit mode
TA, TB	test bits; 0 for normal operation
R2 Page request address	
START COLUMN	start column for page request data
ACQ CCT	selects one of four acquisition circuits
BANK SELECT	selects bank of four pages being addressed for acquisition
R3 Page request data	see Table 3
R4 Display chapter	determines which of the 8 pages is displayed
R5, R6 Display control	for normal and newsflash/subtitle
PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode	
BOX ON 0 (1-23, $\overline{24}$)	boxing function allowed on row 0 (row 1-23, 24)
STATUS ROW $\overline{\text{BTM}}$/TOP	row 25 displayed above or below the main text
R8 to R11	active chapter, row, column and data information written to or read from page memory via the I^2C bus.

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

Abbreviations are as for Table 1 except for D0 CARE bits.
When the D0 CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the D0 CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
Columns auto-increment on successive I^2C transmission bytes.

APPLICATION INFORMATION (continued)

CHARACTER SETS

The UK teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14 as shown in Table 4. The basic 96 character sets differ only in the 13 national option characters as indicated in Tables 8 and 9 with reference to their table position in the basic character matrix shown in Table 7. EURO CCT automatically decodes control bits C12 to C14. Other combinations of C12 to C14 are defaulted to SAA5240A (English); SAA5240B (German). With 8-bit decoding the character matrices are shown in Tables 5 and 6.

Table 4 Selection of national character sets

PHCB	ENGLISH	GERMAN	SWEDISH	ITALIAN	FRENCH
C12	0	0	0	0	1
C13	0	0	1	1	0
C14	0	1	0	1	0

Where:

PHCB page header control bits.

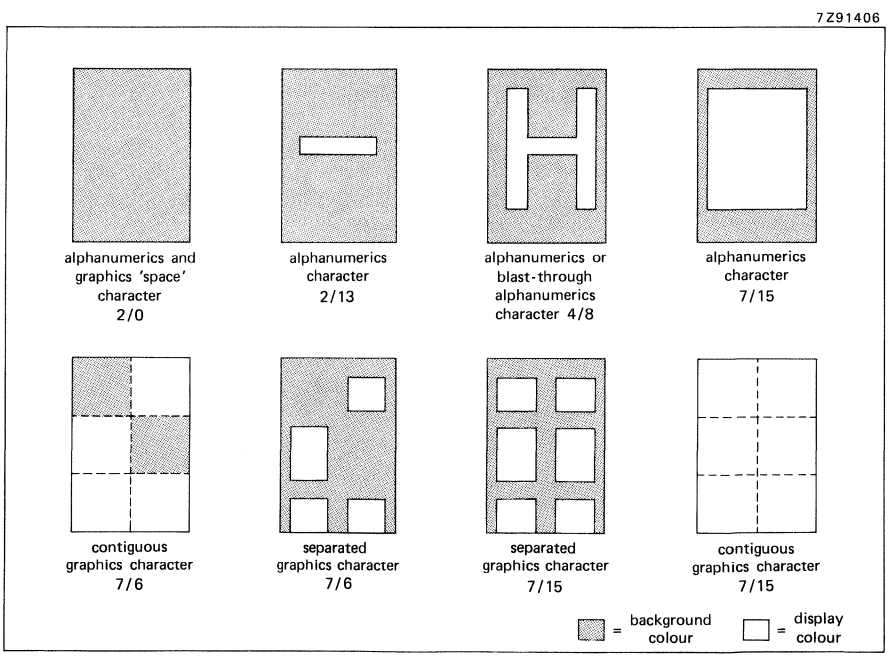


Fig. 12 Character format.

Table 5 Character data input decoding (SAA5240A)

BITS b_8	0	0	0 or 1		0 or 1		0 or 1	0 or 1	0 or 1		0 or 1		1	1
b_7	0	0	0		0		1	1	1		1		0	0
b_6	0	0	1		1		0	0	0		1		0	0
b_5	0	1	0		1		0	1	0		1		0	1
b_4 b_3 b_2 b_1 / row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9
0 0 0 0 / 0	alpha–numerics black	graphics black			0		§	P	°		p		@	É
0 0 0 1 / 1	alpha–numerics red	graphics red	!		1		A	Q	a		q		—	é
0 0 1 0 / 2	alpha–numerics green	graphics green	"		2		B	R	b		r		¼	ä
0 0 1 1 / 3	alpha–numerics yellow	graphics yellow	#		3		C	S	c		s		£	#
0 1 0 0 / 4	alpha–numerics blue	graphics blue	$		4		D	T	d		t		$	Ø
0 1 0 1 / 5	alpha–numerics magenta	graphics magenta	%		5		E	U	e		u		←	ø
0 1 1 0 / 6	alpha–numerics cyan	graphics cyan	&		6		F	V	f		v		↑	Å
0 1 1 1 / 7	alpha–numerics white **	graphics white	'		7		G	W	g		w		→	å
1 0 0 0 / 8	flash	conceal display	(		8		H	X	h		x		↓	Ü
1 0 0 1 / 9	steady **	contiguous graphics **	)		9		I	Y	i		y		½	ü
1 0 1 0 / 10	end box **	separated graphics	*		:		J	Z	j		z		°	→
1 0 1 1 / 11	start box	ESC *	+		;		K	Ä	k		ä		¼	←
1 1 0 0 / 12	normal height **	black background **	,		<		L	Ö	l		ö		½	Ö
1 1 0 1 / 13	double height	new background	—		=		M	Ü	m		ü		→	Ä
1 1 1 0 / 14	SO *	hold graphics	.		>		N	^	n		ß		↑	Ü
1 1 1 1 / 15	SI *	release graphics **	/		?		O	_	o				#	

7Z91402

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Table 6 Character data input decoding (SAA5240B)

BITS b_8				0	0	0 or 1		0 or 1		0 or 1	0 or 1	0 or 1		0 or 1		1	1
b_7				0	0	0		0		1	1	1		1		0	0
b_6				0	0	1		1		0	0	1		1		0	0
b_5				0	1	0		1		0	1	0		1		0	1
b_4	b_3	b_2	b_1	column / row 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9
0	0	0	0	0	alpha–numerics black	graphics black												
0	0	0	1	1	alpha–numerics red	graphics red												
0	0	1	0	2	alpha–numerics green	graphics green												
0	0	1	1	3	alpha–numerics yellow	graphics yellow												
0	1	0	0	4	alpha–numerics blue	graphics blue												
0	1	0	1	5	alpha–numerics magenta	graphics magenta												
0	1	1	0	6	alpha–numerics cyan	graphics cyan												
0	1	1	1	7	alpha–numerics white **	graphics white												
1	0	0	0	8	flash	conceal display												
1	0	0	1	9	steady **	contiguous graphics **												
1	0	1	0	10	end box **	separated graphics												
1	0	1	1	11	start box	ESC *												
1	1	0	0	12	normal height **	black back–ground **												
1	1	0	1	13	double height	new back–ground												
1	1	1	0	14	SO *	hold graphics												
1	1	1	1	15	SI *	release graphics **												

7Z91484

* These control characters are reserved for compatibity with other data codes.

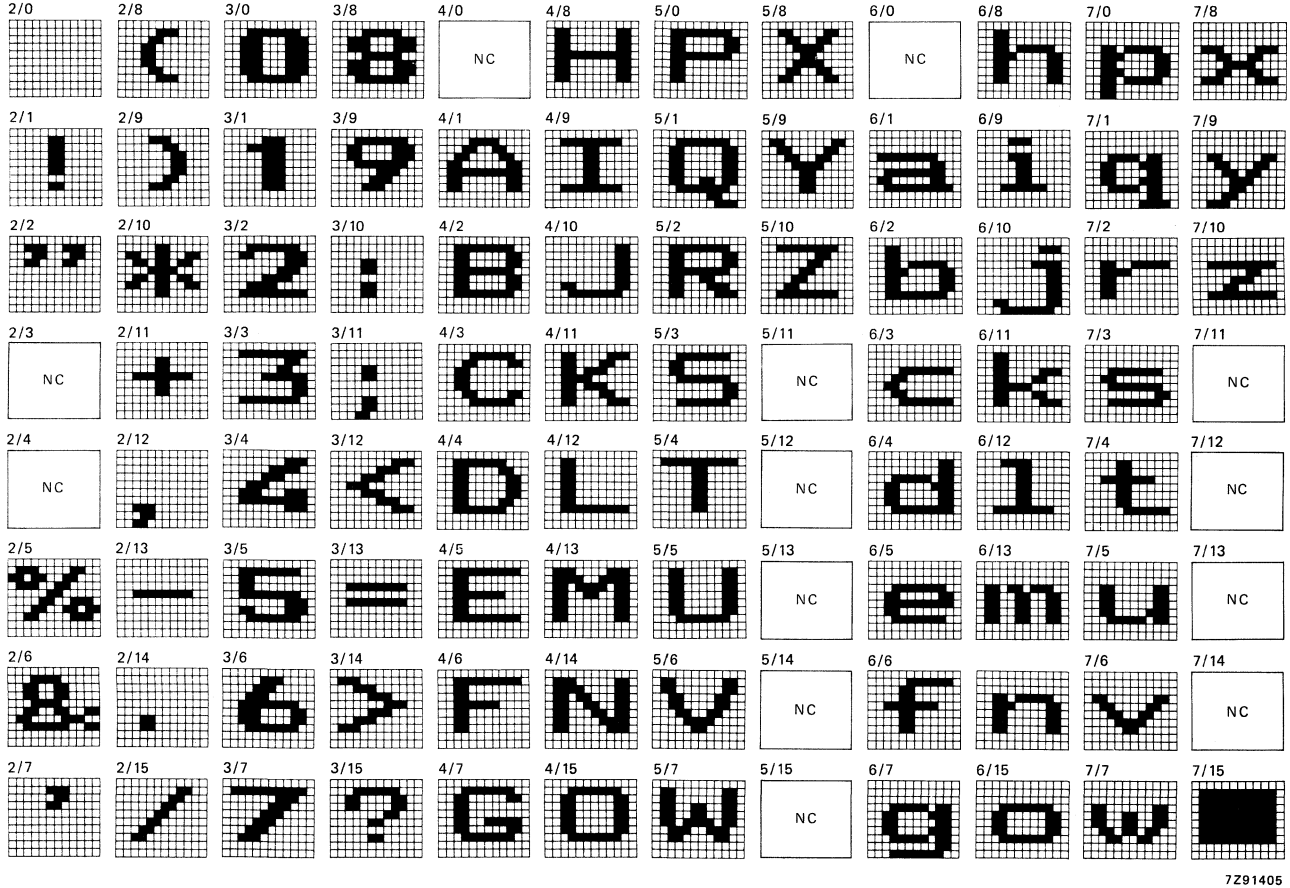
** These control characters are presumed before each row begins.

Notes to Tables 5 and 6

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. The SAA5240A national option characters are shown in Table 8.
6. The SAA5240B national option characters are shown in Table 9.
7. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters to combine with character 8/5.
8. With bit 8 = 0 national option characters will be decoded according to the setting of control bits C12 to C14 (see Table 4).

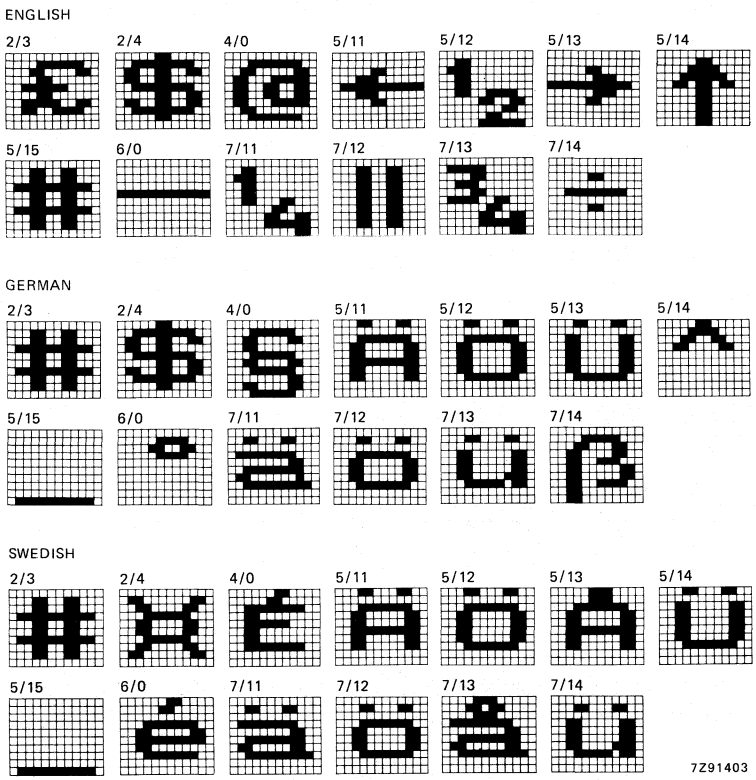
APPLICATION INFORMATION (continued)

Table 7 SAA5240 basic character matrix



Where: NC national option character position.

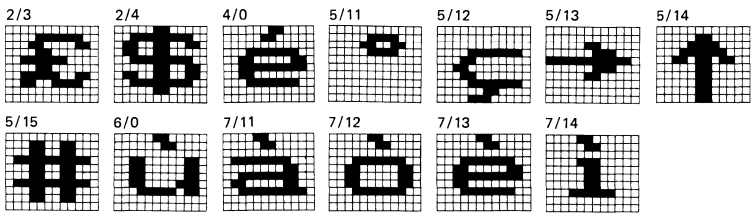
Table 8 SAA5240A character set (national option characters)



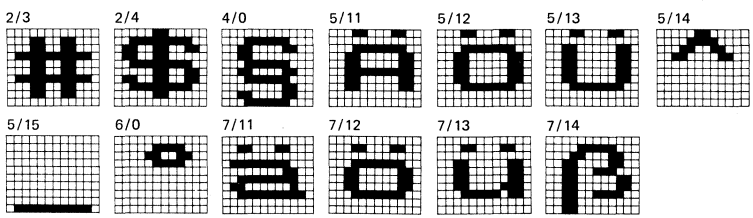
APPLICATION INFORMATION (continued)

Table 9 SAA5240B character set (national option characters)

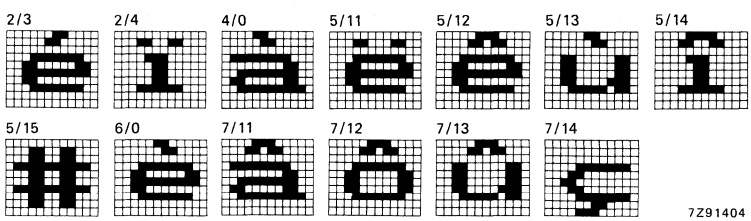
ITALIAN



GERMAN



FRENCH



7Z91404

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

SINGLE-CHIP COLOUR CRT CONTROLLER (EUROM)

GENERAL DESCRIPTION

The SAA5350 EUROM is a single-chip VLSI NMOS crt controller capable of handling all display functions required by the CEPT videotex terminal, model A4. Only minimal hardware is required to produce a videotex terminal using EUROM – the simplest configuration needs just a microcontroller and 4 Kbytes of display memory.

Features

- Minimal additional hardware required
- Screen formats of 40/80 character by 1-to-25 row display
- 512 alphanumeric or graphical characters on-chip or extendable off-chip
- Serial attribute storage (STACK) and parallel attribute storage
- Dynamically redefinable character (DRCS) capability over full field
- Interfaces with 8/16-bit microprocessors with optional direct memory access
- On-chip scroll map minimizes data to be transferred when scrolling
- On-chip colour map RAM (4096 locations) and three on-chip digital-to-analogue converters allow 32 colours on-screen
- On-chip digital-to-analogue converters are non-linear to compensate for crt non-linearity
- Memory interface capable of supporting multi-page terminals. EUROM can access up to 128 Kbytes of display memory
- Programmable cursor
- Programmable local status row
- Three synchronization modes:

stand-alone	built-in oscillator operating with an external 6 MHz crystal
simple slave	directly synchronized from the source of text composite sync
phase-locked slave	indirect synchronization allows picture-in-text displays (e.g. VCR/VLP video with text overlay)

- On-chip timing composite sync output
- Zoom feature which allows the height of any group of rows to be increased to enhance legibility

PACKAGE OUTLINE

40-lead DIL; plastic (SOT-129).

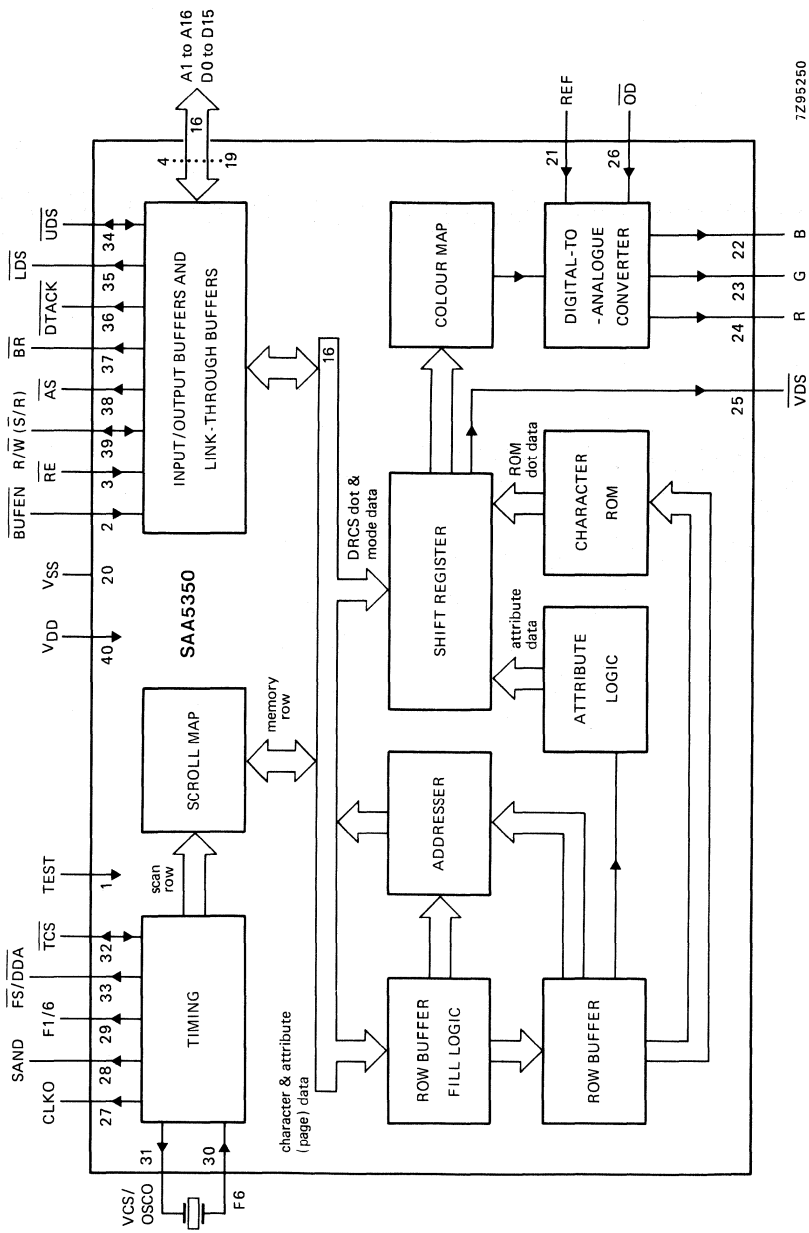


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

1	TEST	Input to be connected to V_{SS}.
2	$\overline{BUFEN}$	Buffer enable input to the 8-bit link-through buffer.
3	$\overline{RE}$	Register enable input. This enables A1 to A6 and $\overline{UDS}$ as inputs, and D8 to D15 as input/outputs.
4 to 19	A16 to A1/ D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer.
20	V_{SS}	Ground (0 V).
21	REF	Analogue reference input.
22	B	Analogue outputs (signals are gamma-corrected).
23	G	
24	R	
25	$\overline{VDS}$	Switching output for dot, screen (row), box and window video data; for use when video signal is present (e.g. from tv, VLP, alpha + photographic layer). This output is LOW for tv display and HIGH for text and will interface directly with a number of colour decoder ICs (e.g. TDA3560, TDA3505).
26	$\overline{OD}$	Output disable causing R, G, B and $\overline{VDS}$ outputs to go to high-impedance state. Can be used at dot-rate.
27	CLKO	12 MHz clock output for hard-copy dot synchronization (referenced to output dots).
28	SAND	Sandcastle feedback output for SAA5230 teletext video processor or other circuit. Used when the display must be locked to the video source (e.g. VLP). The phase-lock part of the sandcastle waveform can be disabled to allow free-running of the SAA5230 phase-locked loop.
29	F1/6	1 MHz or 6 MHz output.
30	F6	6 MHz clock input (e.g. from SAA5230). Internal a.c. coupling is provided.
31	VCS/OSCO	Video composite sync input (e.g. from SAA5230) for phase reference of vertical display timing when locking to a video source (e.g. VLP) or, in stand-alone sync mode, output from internal oscillator circuit (fixed frequency).
32	$\overline{TCS}$	Text composite sync input/output depending on master/slave status.
33	$\overline{FS}/\overline{DDA}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots).
34	$\overline{UDS}$	Upper data strobe input/output.
35	$\overline{LDS}$	Lower data strobe output.
36	$\overline{DTACK}$	Data transfer acknowledge (open drain output).
37	$\overline{BR}$	Bus request to microprocessor (open drain output).
38	$\overline{AS}$	Address strobe output to external address latches.
39	R/$\overline{W}$ ($\overline{S}$/R)	Read/write input/output. Also serves as send/receive for the link-through buffer.
40	V_{DD}	Positive supply voltage (+ 5 V).

PINNING (continued)

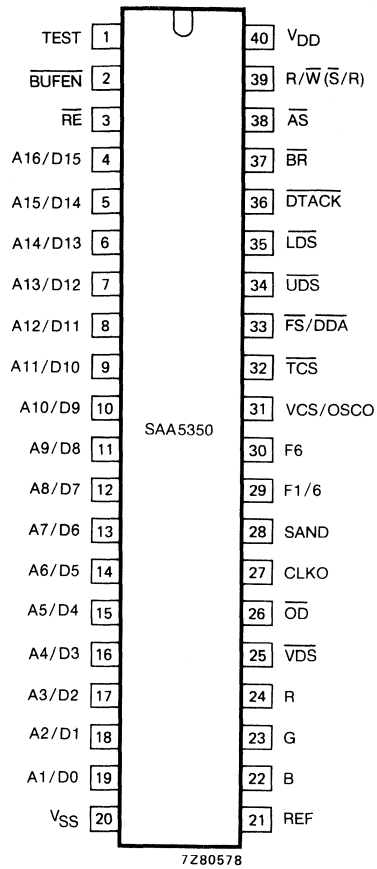


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}	−0,3 to + 7,5 V
Maximum input voltage (except F6, $\overline{TCS}$, REF)	V_{Imax}	−0,3 to + 7,5 V
Maximum input voltage (F6, $\overline{TCS}$)	V_{Imax}	−0,3 to + 10,0 V
Maximum input voltage (REF)	V_{REF}	−0,3 to + 3,0 V
Maximum output voltage	V_{Omax}	−0,3 to + 7,5 V
Maximum output current	I_{Omax}	10 mA
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 40)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 40)	I_{DD}	–	–	350	mA
INPUTS					
F6 (note 1)					
Slave modes (Fig. 3)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	7,0	V
Input peaks relative to 50% duty factor	$\pm V_P$	0,2	–	3,5	V
Input leakage current at V_I = 0 to 10 V; T_{amb} = 25 °C	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	12	pF
Stand-alone mode (Fig. 4)					
Series capacitance of crystal	C_1	–	28	–	fF
Parallel capacitance of crystal	C_0	–	7,1	–	pF
Resonance resistance of crystal	R_r	–	–	60	Ω
Gain of circuit	G	–	–	tbf	V/V
$\overline{\text{BUFEN}}$, $\overline{\text{RE}}$, $\overline{\text{OD}}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input current at V_I = 0 to V_{DD}+0,3 V; T_{amb} = 25 °C	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
REF (Fig. 5)					
Input voltage	V_{REF}	0	1 to 2	2,7	V
Resistance (pin 21 to pin 20) with REF supply and R, G, B outputs OFF	R_{REF}	–	125	–	Ω

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS					
SAND					
Output voltage high level at I_O = 0 to −30 μA	V_{OH}	4,2	–	V_{DD}	V
Output voltage intermediate level at I_O = −30 to + 30 μA	V_{OI}	1,3	2,0	2,7	V
Output voltage low level at I_O = 0,2 mA	V_{OL}	0	–	0,2	V
Load capacitance	C_L	–	–	30	pF
F1/6, CLKO, $\overline{\text{DDA}}$/$\overline{\text{FS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
$\overline{\text{LDS}}$, $\overline{\text{AS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF
$\overline{\text{DTACK}}$, $\overline{\text{BR}}$ (open drain outputs)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	150	pF
Capacitance (OFF state)	C_{OFF}	–	–	7	pF
R, G, B (note 2)					
Output voltage HIGH (note 3) at I_{OH} = −100 μA; V_{REF} = 2,7 V	V_{OH}	2,4	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Output resistance during line blanking	R_{OBL}	–	–	150	Ω
Output capacitance (OFF state)	C_{OFF}	–	–	12	pF
Output leakage current (OFF state) at V_I = 0 to V_{DD}+ 0,3 V; T_{amb} = 25 °C	I_{OFF}	−10	–	+ 10	μA

parameter	symbol	min.	typ.	max.	unit
$\overline{VDS}$					
Output voltage HIGH at $I_{OH} = -250\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 2$ mA	V_{OL}	0	–	0,4	V
Output voltage LOW at $I_{OL} = 1$ mA	V_{OL}	0	–	0,2	V
Output leakage current (OFF state) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_{OFF}	−10	–	+ 10	μA
INPUT/OUTPUTS					
VCS/OSCO					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input current (output OFF) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
$\overline{TCS}$					
Input voltage HIGH	V_{IH}	3,5	–	10,0	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200$ to $100\ \mu A$	V_{OH}	2,4	–	6,0	V
Output voltage LOW at $V_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
A1/D0 to A16/D15, $\overline{UDS}$, R/$\overline{W}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TIMING					
F6 (Fig. 3)					
Rise and fall times	t_r, t_f	10	–	80	ns
Frequency	f_{F6}	5,9	–	6,1	MHz
CLKO, F1/6, R, G, B, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$, $\overline{OD}$ (notes 4, 5 and Fig. 6)					
CLKO HIGH time	t_{CLKH}	30	–	–	ns
CLKO LOW time	t_{CLKL}	20	–	–	ns
CLKO rise and fall times	t_{CLKr} t_{CLKf}	–	–	10	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ change	t_{VCH}	10	–	–	ns
R, G, B, $\overline{VDS}$ valid to CLKO rise	t_{VOC}	10	–	–	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ valid	t_{COV}	–	–	60	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ floating after $\overline{OD}$ fall	t_{FOD}	–	–	30	ns
Skew between outputs R, G, B, $\overline{VDS}$	t_{VS}	–	–	20	ns
R, G, B, $\overline{VDS}$ rise and fall times	t_{Vr}, t_{Vf}	–	–	30	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ active after $\overline{OD}$ rise	t_{AOD}	0	–	–	ns
CLKO HIGH to $\overline{FS}$/$\overline{DDA}$ change	t_{COD}	–	–	55	ns
$\overline{FS}$/$\overline{DDA}$ valid to CLKO rise	t_{DOC}	5	–	–	ns
F1 HIGH time (note 6)	t_{F1H}	–	500	–	ns
F1 LOW time (note 6)	t_{F1L}	–	500	–	ns
F6 HIGH time	t_{F6H}	–	83	–	ns
F6 LOW time	t_{F6L}	–	83	–	ns
$\overline{OD}$ to CLKO rise set-up	t_{ODS}	–	–	45	ns
$\overline{OD}$ to CLKO HIGH hold	t_{ODH}	–	–	0	ns
MEMORY ACCESS TIMING (notes 7, 8, 9 and Fig. 7)					
$\overline{UDS}$, $\overline{LDS}$, $\overline{AS}$					
Cycle time	t_{cyc}	–	500	–	ns
$\overline{UDS}$ HIGH to bus-active for address output	t_{SAA}	75	–	–	ns
Address valid set-up to $\overline{AS}$ fall	t_{ASU}	20	–	–	ns
Address valid hold from $\overline{AS}$ LOW	t_{ASH}	20	–	–	ns
Address float to $\overline{UDS}$ fall	t_{AFS}	0	–	–	ns

parameter	symbol	min.	typ.	max.	unit
$\overline{AS}$ LOW to $\overline{UDS}$ fall delay	t_{ATD}	50	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ HIGH time	t_{HDS}	220	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ LOW time	t_{LDS}	200	–	–	ns
$\overline{AS}$ HIGH time	t_{HAS}	125	–	–	ns
$\overline{AS}$ LOW time	t_{LAS}	320	–	–	ns
$\overline{AS}$ LOW to $\overline{UDS}$ HIGH	t_{AUH}	305	–	–	ns
Data valid set-up to $\overline{UDS}$ rise	t_{DSU}	30	–	–	ns
Data valid hold from $\overline{UDS}$ HIGH	t_{DSH}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{AS}$ rise delay	t_{UAS}	0	–	–	ns
$\overline{AS}$ LOW to data valid	t_{AFA}	–	–	270	ns
Link-through buffers (notes 7, 8 and Fig. 8)					
$\overline{BUFEN}$ LOW to output valid	t_{BEA}	–	–	100	ns
Link-through delay time	t_{LTD}	–	–	85	ns
Input data float prior to direction change	t_{IFR}	0	–	–	ns
Output float after direction change	t_{OFR}	–	–	60	ns
Output float after $\overline{BUFEN}$ HIGH	t_{BED}	–	–	60	ns
Microprocessor READ from EUROM (Fig. 9)					
R/$\overline{W}$ HIGH set-up to $\overline{UDS}$ fall	t_{RUD}	0	–	–	ns
$\overline{UDS}$ LOW to returned-data access time	t_{UDA}	–	–	210	ns
$\overline{RE}$ LOW to returned data access time	t_{REA}	–	–	210	ns
Data valid to $\overline{DTACK}$ LOW delay	t_{DTL}	−20	–	–	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	50	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	0	–	–	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ fall	t_{UDR}	0	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DSD}	190	–	260	ns
Address valid to $\overline{UDS}$ fall	t_{AUL}	0	–	–	ns

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
MEMORY ACCESS TIMING (continued)					
Microprocessor WRITE to EUROM (Fig. 10)					
Write cycle time (note 10)	t_{WCY}	500	–	–	ns
R/$\overline{W}$ LOW set-up to $\overline{UDS}$ fall	t_{WUD}	0	–	–	ns
$\overline{RE}$ LOW to $\overline{UDS}$ fall	t_{RES}	30	–	–	ns
Address valid to $\overline{UDS}$ fall	t_{ASS}	30	–	–	ns
$\overline{UDS}$ LOW time	t_{LUS}	100	–	–	ns
Data valid to $\overline{UDS}$ rise	t_{DSS}	80	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DTA}	0	–	60	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	50	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	0	–	–	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ rise	t_{UDW}	0	–	–	ns
F1/6 to memory access cycle (Fig. 11)					
$\overline{UDS}$ HIGH to F6 (component of F1/6) rise	t_{UF6}	20	–	–	ns
F6 (component of F1/6) HIGH to $\overline{UDS}$ rise	t_{F6U}	40	–	–	ns
SYNCHRONIZATION and BLANKING					
$\overline{TCS}$, SAND, $\overline{FS}$/$\overline{DDA}$					
See Fig. 12 for timing relationships and Fig. 13 for vertical sync and blanking waveforms.					

Notes to the characteristics

1. Pin 30 must be biased externally as it is internally a.c. coupled.
2. 16-level analogue voltage outputs.
3. Output voltage guaranteed when programmed for top level.
4. CLKO, R, G, B, F1/6, $\overline{VDS}$: C_L = 25 pF
   $\overline{FS}$/$\overline{DDA}$: C_L = 50 pF
5. CLKO, F1/6, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$: reference levels = 0,8 to 2,0 V
   R, G, B: reference levels = 0,8 to 2,0 V with V_{REF} = 2,7 V
6. These times may momentarily be reduced to a nominal 83 ns in slave-sync mode at the moment of re-synchronization.
7. C_L = 150 pF.
8. Reference levels = 0,8 to 2,0 V.
9. F6 input at 6 MHz.
10. Microprocessor write cycle times of less than 500 ns are permitted but often result in Wait States being generated, the precise timing of $\overline{DTACK}$ will then depend on the internal synchronization time.

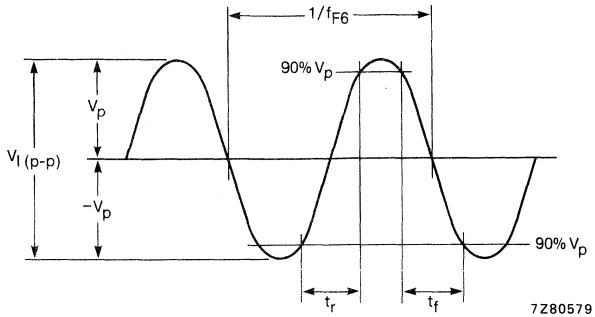
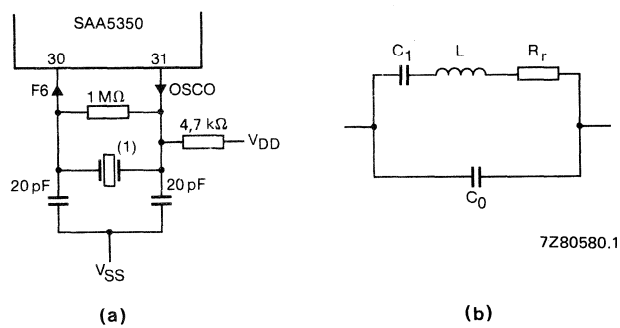


Fig. 3 F6 input waveform.



(1) Catalogue number of crystal: 4322 143 04101

Fig. 4(a) Oscillator circuit for SAA5350 stand-alone sync mode and (b) equivalent circuit of crystal at resonance (see **characteristics** for values).

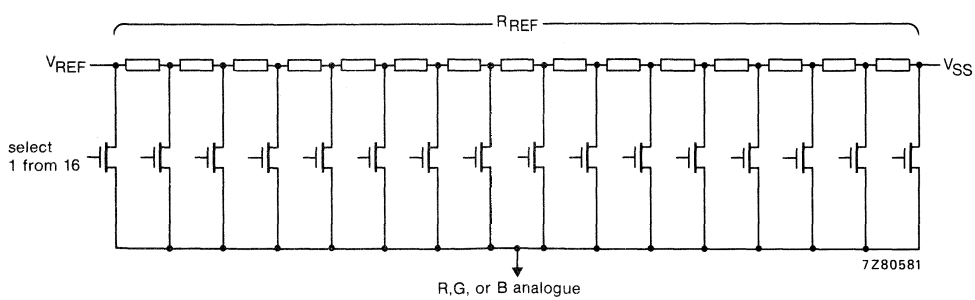


Fig. 5 Circuit arrangement giving one-of-sixteen reference voltage levels for the R, G or B analogue outputs.

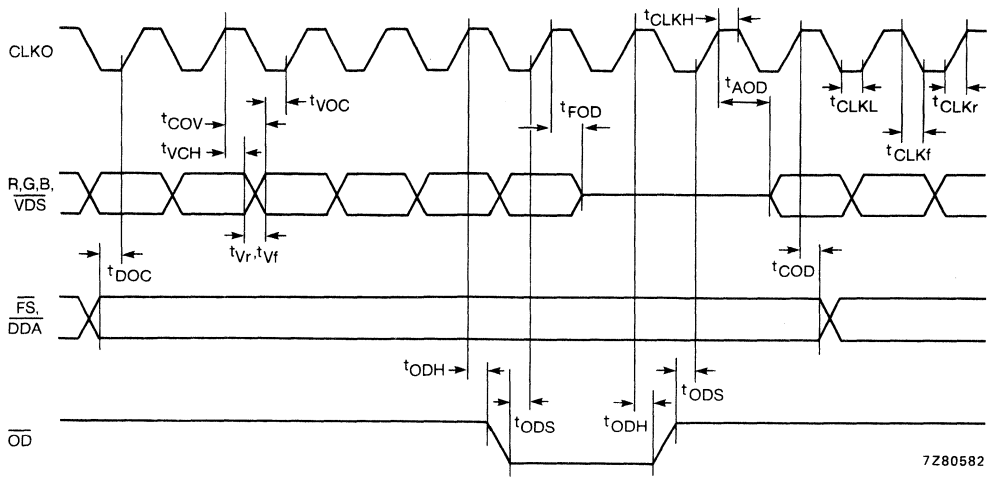


Fig. 6 Video timing.

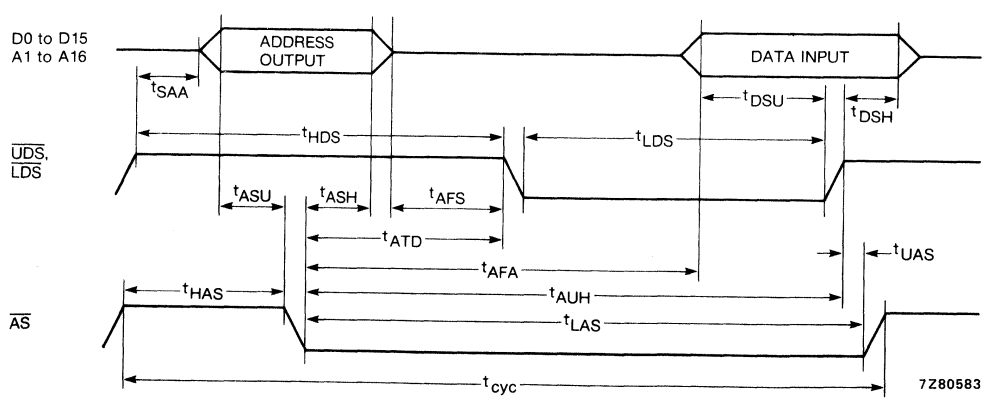


Fig. 7 Memory access timing.

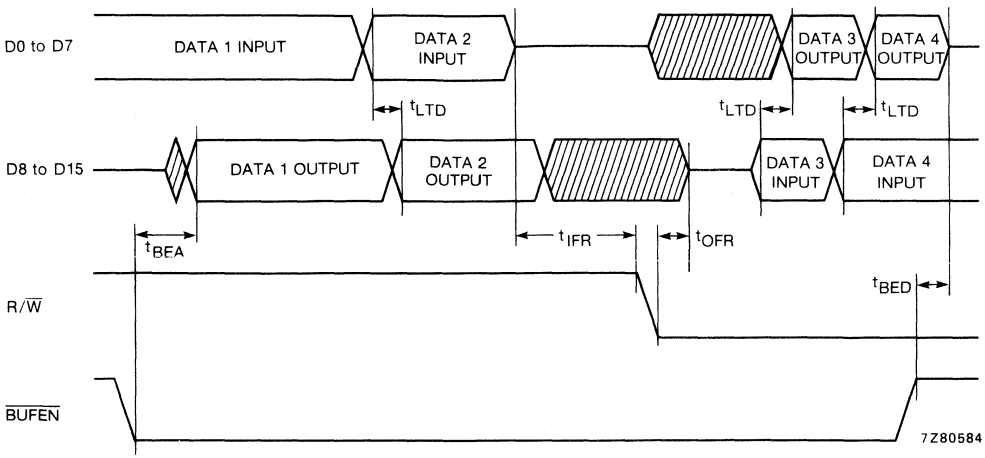


Fig. 8 Timing of link-through buffers.

DEVELOPMENT DATA

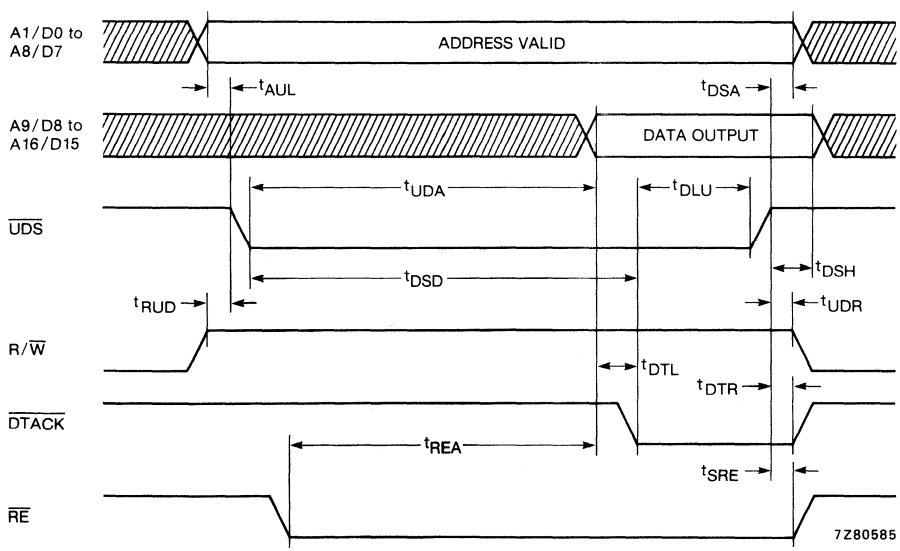


Fig. 9 Timing of microprocessor read from EUROM.

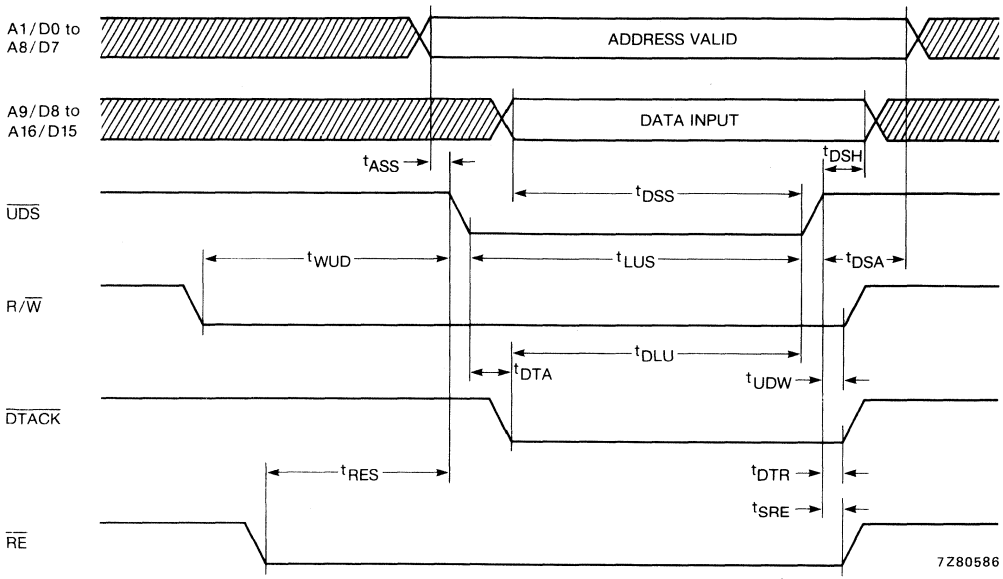


Fig. 10 Timing of microprocessor write to EUROM.

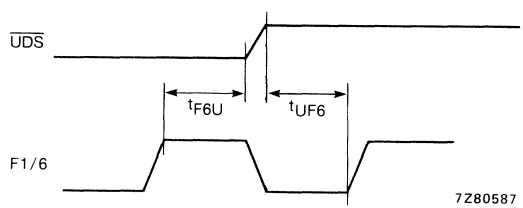


Fig. 11 Timing of F1/6 to memory access cycle.

DEVELOPMENT DATA

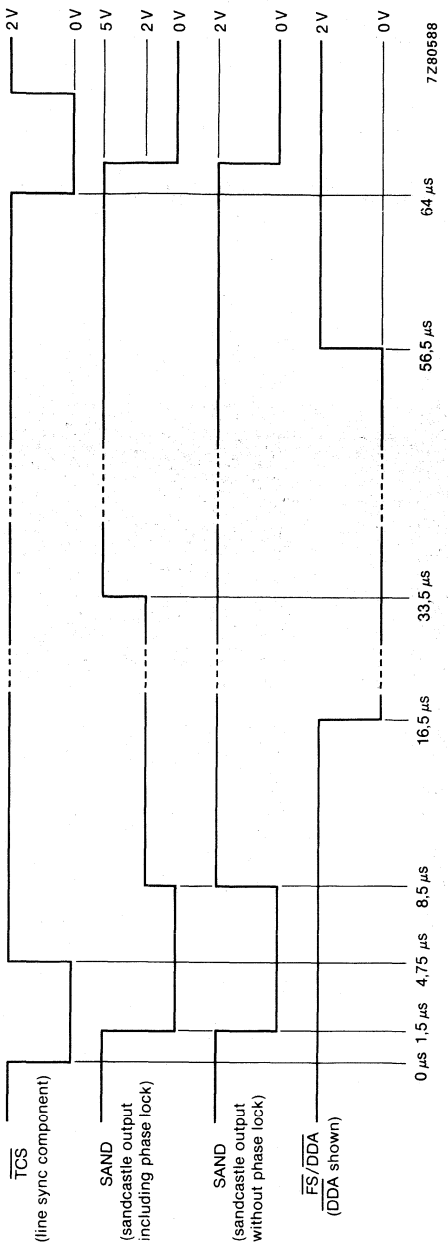


Fig. 12 Timing of synchronization and blanking outputs; all timings are nominal and assume $f_{F6} = 6$ MHz.

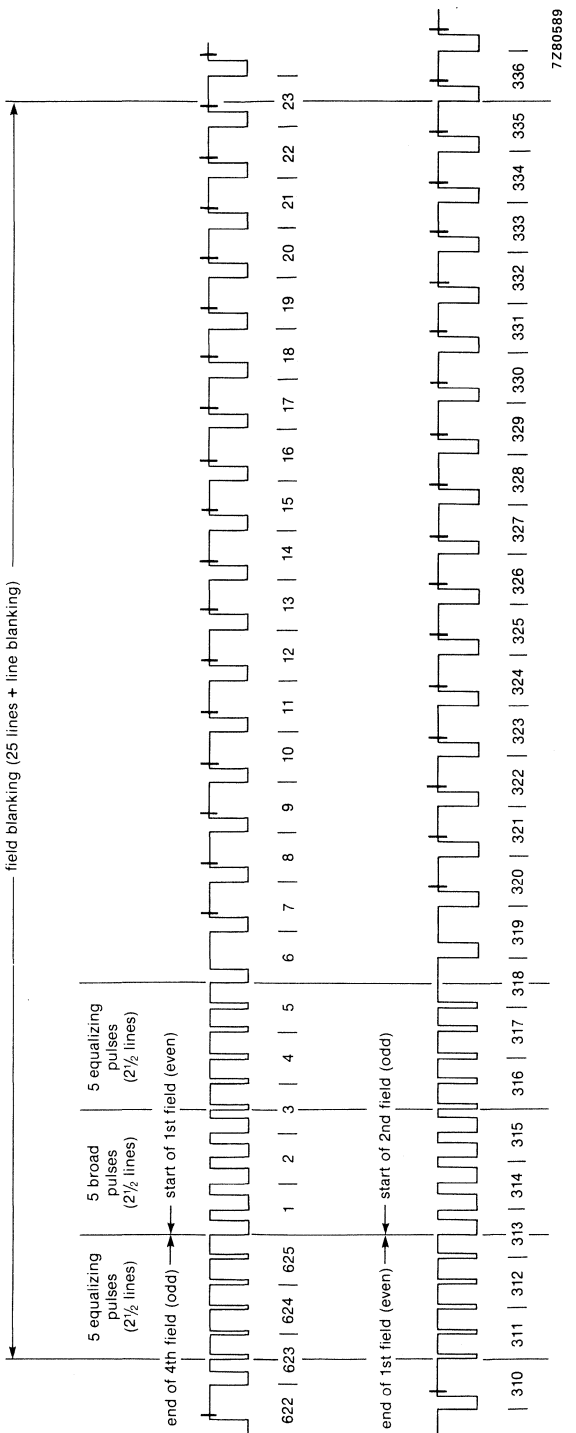


Fig. 13 Vertical synchronization and blanking waveforms; separation of broad pulses = 4,75 μs; equalizing pulse widths = 2,25 μs.

APPLICATION INFORMATION

More detailed application information is available on request

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Fig. 14, reference should also be made to the block diagram Fig. 1.

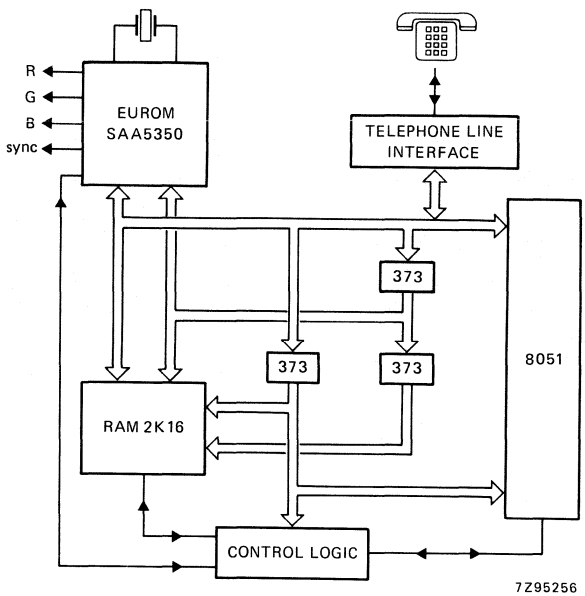


Fig. 14 Basic videotex decoder configuration.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows – each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colours, and during the display time it is also used for addressing DRCS characters.

Timing

The timing chain operates from an external 6 MHz clock or an on-chip fixed-frequency crystal oscillator. The basic video format is 40 characters per row, 24/25 rows per page and 10 video lines per row. EUROM will also operate with 20/21 rows per page and 12 video lines per row. The two extra lines per row are added symmetrically and contain background colour only for ROM-based alpha-numeric characters. DRCS characters, block and smooth mosaics and line drawing characters occupy all 12 lines.

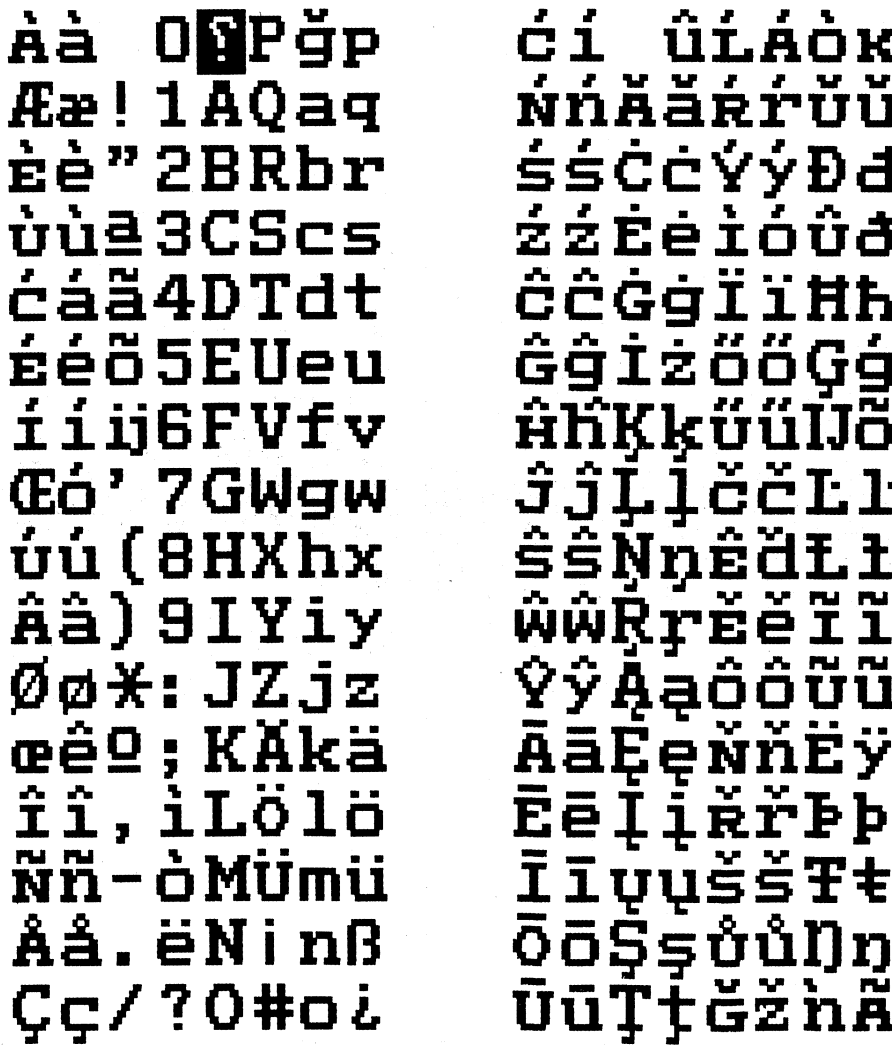
The display is generated to the normal 625-line/50 Hz scanning standard (interlaced or non-interlaced). In addition to composite sync (pin 32) for conventional timebases, a clock output at 1 MHz or 6 MHz (pin 29) is available for driving other videotex devices, and a 12 MHz clock (pin 27) is available for hard-copy dot synchronization. A defined-display-area timing signal (pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

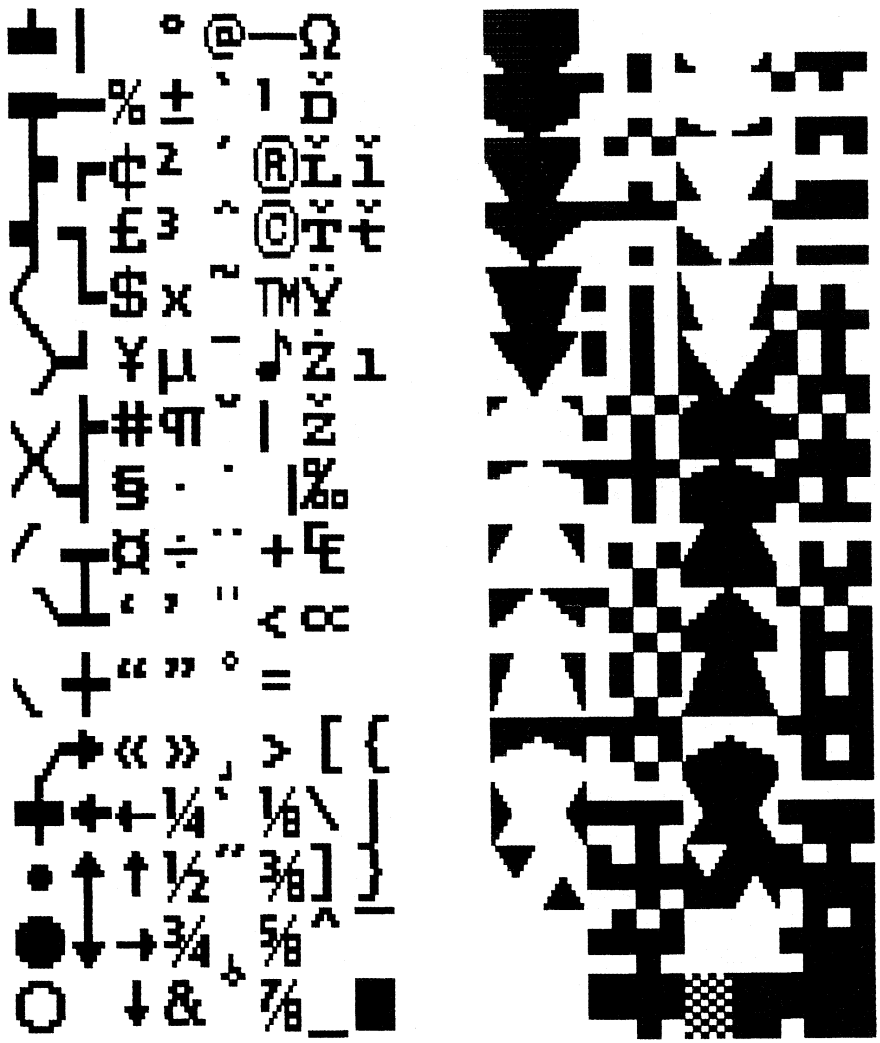
Character generation

EUROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters and four are stored in an external RAM. The contents of the fixed character tables (Tables 0 to 3) are shown in Figs 15 and 16.



(a) (b)

Fig. 15 On-chip characters: (a) Table 0; (b) Table 1.



(a) (b)

Fig. 16 On-chip characters: (a) Table 2; (b) Table 3.

APPLICATION INFORMATION (continued)

Character generation (continued)

The 128 most commonly used characters are contained in Table 0, these are the standard upper and lower-case letters of the Roman alphabet, numerals, punctuation and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set and accents without associated symbols are contained in Table 2. Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row so allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.
Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Colour map and digital-to-analogue converters

The colour map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D-A converter. The resulting R, G and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground colour, background colour, lining and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-Videotex applications, the device will also support the following operating modes:

Explicit fill mode. An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode. When operating with 80 characters per row, the available display attributes are eight foreground colours, eight (potentially different) background colours (including transparent) as well as underline and blink.

Full field DRCS mode. This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a 'bit map'. All ROM-based characters and all display attributes remain available.

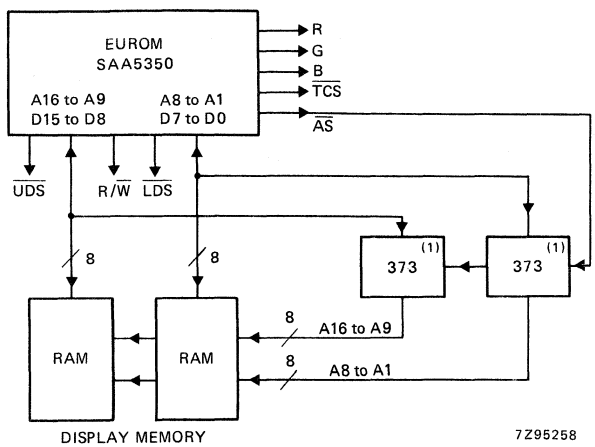
MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

- EUROM fetches data from the display memory
- The microprocessor reads from, or writes to, EUROM's internal register map
- The microprocessor accesses the display memory

EUROM access to display memory (Figs 17 and 18)

EUROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 500 ns. The address strobe ($\overline{AS}$) signal from EUROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most-significant) and lower (least-significant) display information and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/$\overline{W}$ is included although EUROM only reads from the display memory.



(1) 74LS373 octal transparent latch (3-state)

Fig. 17 Simple RAM interface circuit for display memory access.

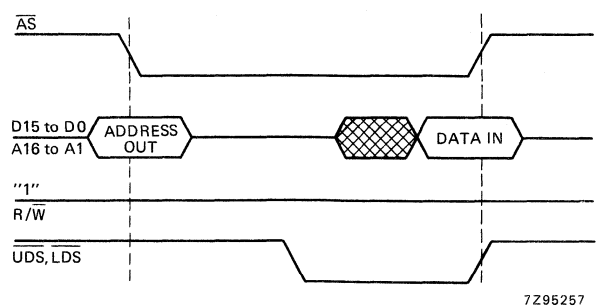


Fig. 18 Bus timing for display memory access.

APPLICATION INFORMATION (continued)

EUROM access to display memory (continued)

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even numbered bytes use the upper (most-significant) part of the bus as shown in Fig. 19. The word addresses are numerically the same as the upper byte that they contain — there are no odd-numbered word addresses.

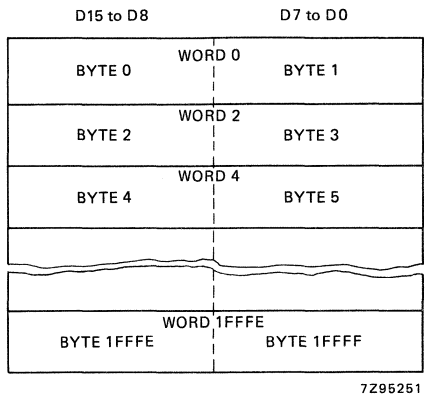


Fig. 19 Display memory word/byte organization.

Warning time

As EUROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by EUROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and EUROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that EUROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of EUROM's bus activity is programmable to be between 0 and 23 μs.

Microprocessor access to register map

EUROM has a set of internal registers which, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of the data bus (Fig. 20). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

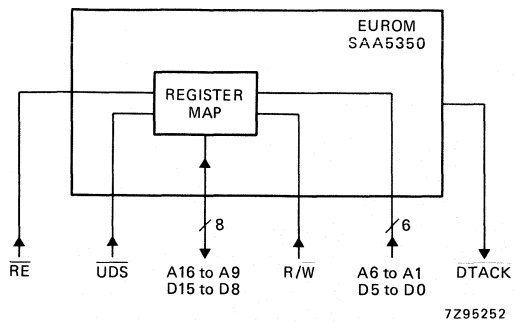


Fig. 20 Microprocessor access to register map.

The main data and address paths used in a connected 68000 interface are shown in Fig. 21. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to EUROM via the octal buffers (74LS244). At the same time the bidirectional buffers (74LS245) disable the signals from the low order data bus of the 68000.

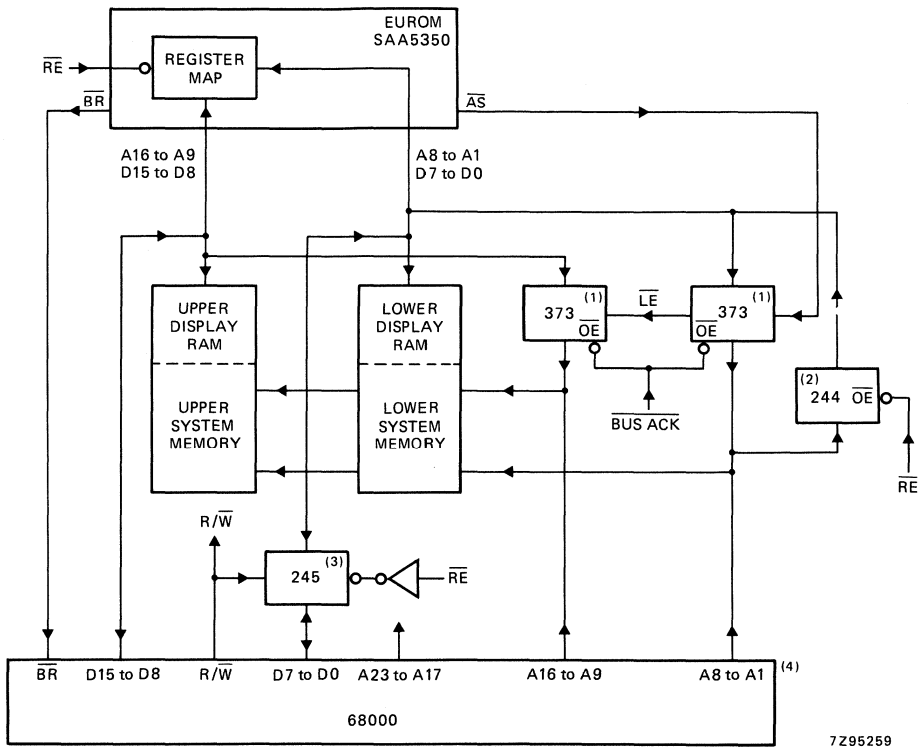
The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by EUROM as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of EUROM's scroll map contents at a location in its main memory.

8-bit microprocessors

Although the control bus is optimised for the SCN68000 16-bit microprocessor unit, EUROM will operate with a number of widely differing industry-standard 8, 16 or more-bit microprocessors or microcontrollers (e.g. SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit wide display memory is made simple by EUROM's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}$/R.

The main data and address paths used in a connected 8-bit microprocessor system are shown in Fig. 22. The interface is similar to that of the 16-bit system but here the display memory does not receive A0 as an address, rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when HIGH).

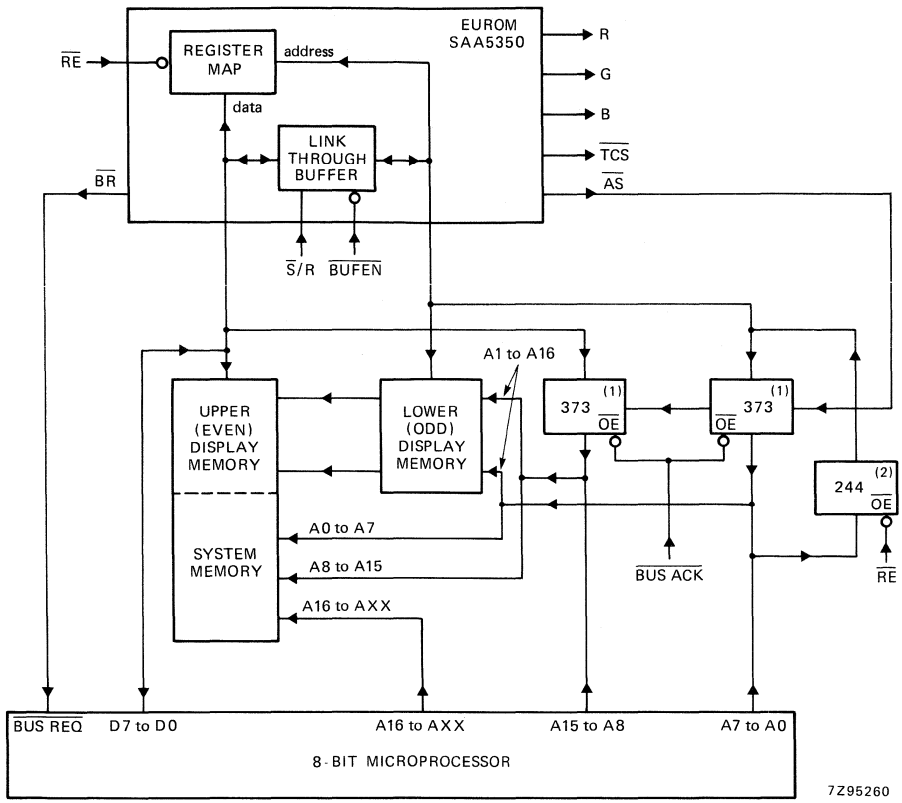
APPLICATION INFORMATION (continued)



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal bus transceiver (3-state)
(4) SCN68000 microprocessor unit

Fig. 21 Connected 16-bit microprocessor system.

DEVELOPMENT DATA



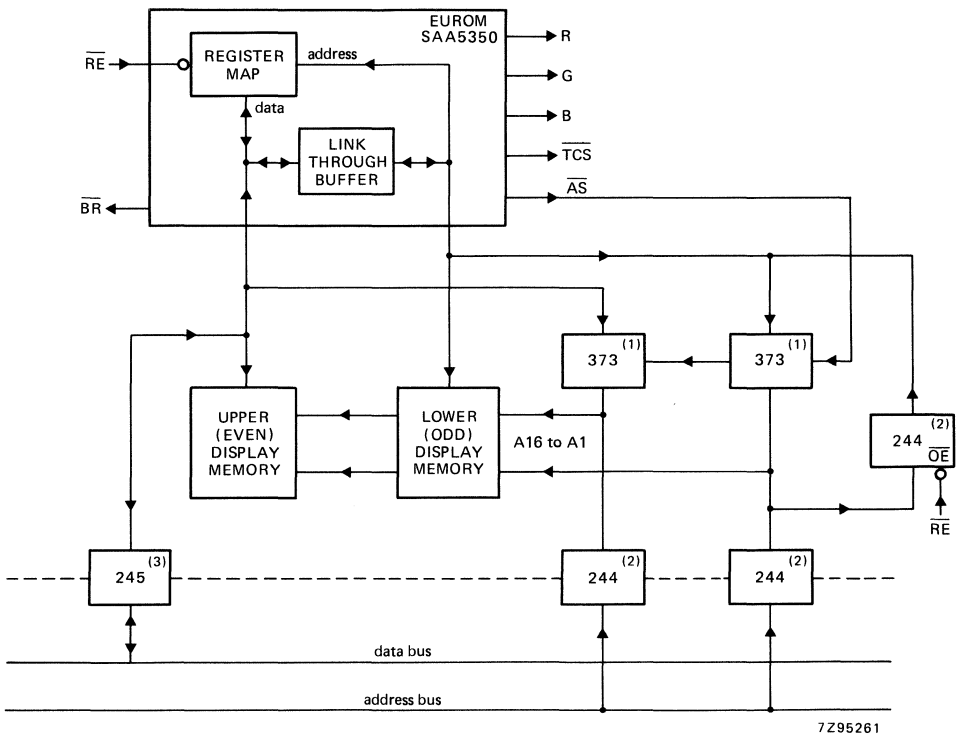
(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)

Fig. 22 Connected 8-bit microprocessor system.

APPLICATION INFORMATION (continued)

Disconnected systems

For many applications it may be desirable to disconnect EUROM and the display memory from the microprocessor and its ROM, RAM and other peripherals by using isolating buffers as shown in Fig. 23. The two parts of the system then operate independently and communicate only when the microprocessor accesses EUROM's register map or the display memory.



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 75LS245 octal bus transceiver (3-state)

Fig. 23 Disconnected 8-bit system.

Synchronization

Stand-alone mode

As a stand-alone device (e.g. in terminal applications) EUROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 6 MHz on-chip oscillator using an external crystal as shown in Fig. 24.

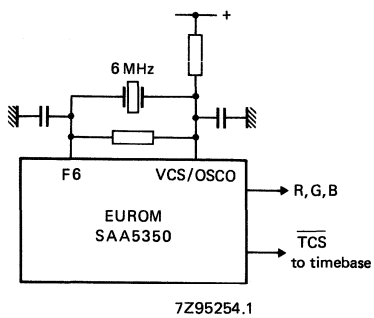


Fig. 24 Stand-alone synchronization mode.

Simple-slave

In the simple-slave mode EUROM synchronizes directly to another device, such as to the $\overline{TCS}$ signal from the SAA5240 European computer-controlled teletext circuit (CCT) or from another EUROM as shown in Fig. 25. EUROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250 ns is built in to avoid resetting the counter at every tv line and so prevents screen jitter.
Field synchronization is made using EUROM's internal field sync separator.

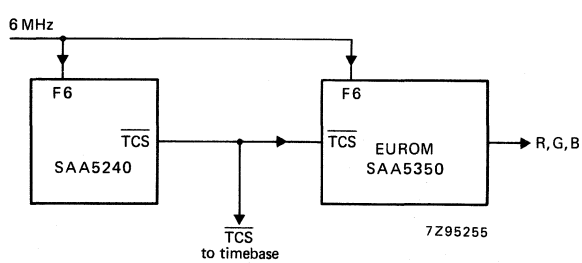


Fig. 25 Simple-slave (direct sync) mode.

APPLICATION INFORMATION (continued)

Synchronization (continued)

Phase-locked slave

The phase-locked slave (indirect sync) mode is shown in Fig. 26. A phase-locked VCO in the SAA5230 teletext video processor provides sync to the timebases. When EUROM is active, its horizontal counter forms part of the phase control loop – a horizontal reference is fed back to the SAA5230 from the SAND output and a vertical reference is generated by feeding separated composite sync to EUROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from EUROM can sync with that from a tv source or a local VLP player, thus giving picture-in-text display possiblities.

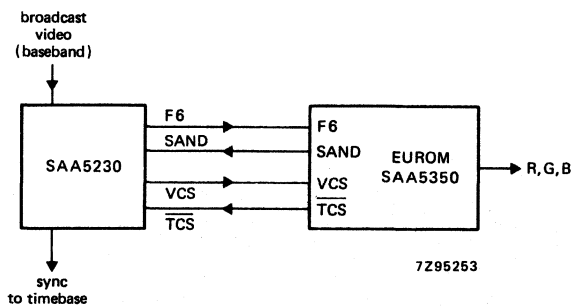


Fig. 26 Phase-locked slave (indirect sync) mode.

SINGLE-CHIP COLOUR CRT CONTROLLER (FTFROM)

GENERAL DESCRIPTION

The SAA5355 FTFROM (Five-Two-Five-ROM) is a single-chip VLSI NMOS crt controller capable of handling the display functions required for a 525-line, level-3 videotex decoder. Only minimal hardware is required to produce a videotex terminal using FTFROM — the simplest configuration needs just a microcontroller and 4 Kbytes of display memory.

Features

- Minimal additional hardware required
- Screen formats of 40/80 character by 1-to-25 row display
- 512 alphanumeric or graphical characters on-chip or extendable off-chip
- Serial attribute storage (STACK) and parallel attribute storage
- Dynamically redefinable character (DRCS) capability over full field
- Interfaces with 8/16-bit microprocessors with optional direct memory access
- On-chip scroll map minimizes data to be transferred when scrolling
- 32 on-screen colours redefinable from a palette of 4096
- Three on-chip digital-to-analogue converters which compensate for crt non-linearity
- Memory interface capable of supporting multi-page terminals. FTFROM can access up to 128 Kbytes of display memory
- Programmable cursor
- Programmable local status row
- Three synchronization modes:

stand-alone	built-in oscillator operating with an external 6,041957 MHz crystal
simple slave	directly synchronized from the source of text composite sync
phase-locked slave	indirect synchronization allows picture-in-text displays (e.g. VCR/VLP video with text overlay)

- On-chip timing with composite sync output
- Zoom feature which allows the height of any group of rows to be increased to enhance legibility

PACKAGE OUTLINE

40-lead DIL; plastic (SOT-129).

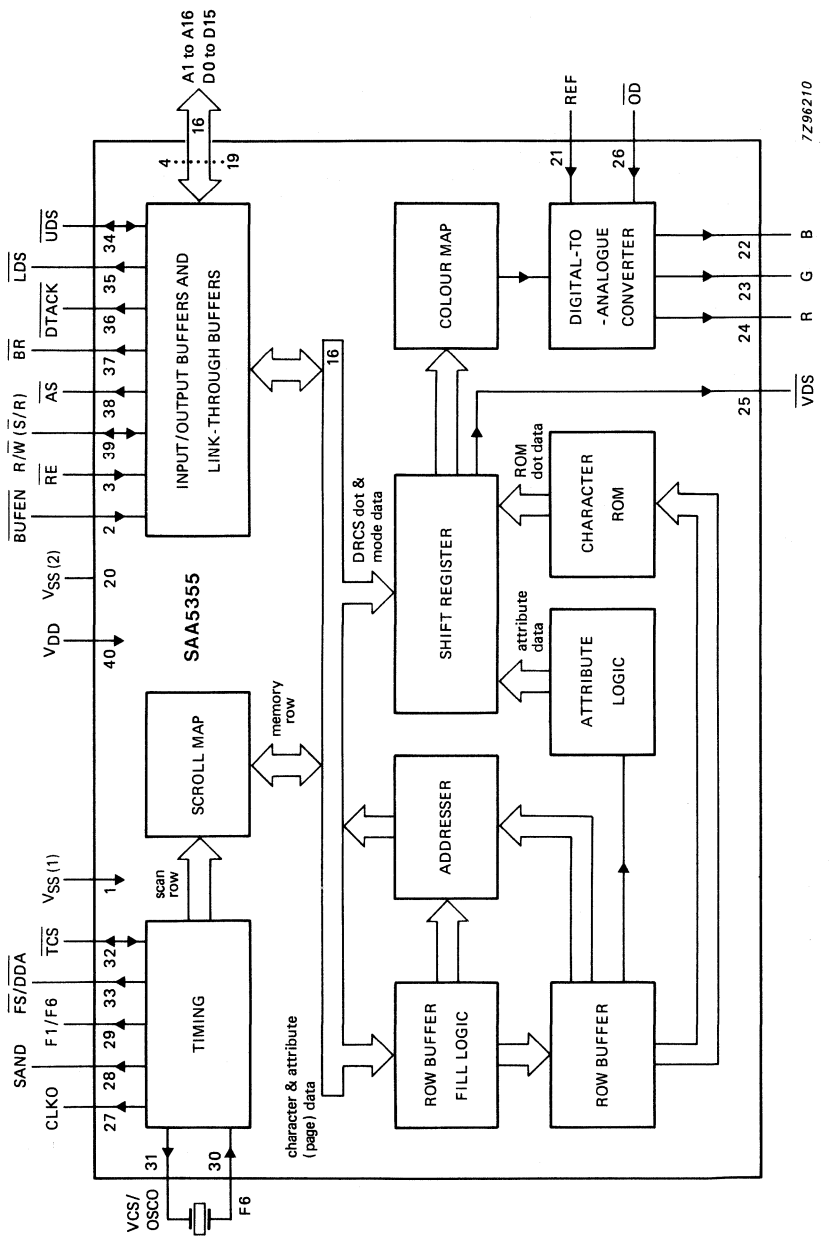


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

1	$V_{SS(1)}$	Ground (0 V).
2	$\overline{BUFEN}$	Buffer enable input to the 8-bit link-through buffer.
3	$\overline{RE}$	Register enable input. This enables A1 to A6 and $\overline{UDS}$ as inputs, and D8 to D15 as input/outputs.
4 to 19	A16 to A1/ D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer.
20	$V_{SS(2)}$	Ground (0 V).
21	REF	Analogue reference input.
22	B	Analogue outputs (signals are gamma-corrected).
23	G	
24	R	
25	$\overline{VDS}$	Switching output for dot, screen (row), box and window video data; for use when video signal is present (e.g. from tv, VLP, alpha + photographic layer). This output is LOW for tv display and HIGH for text and will interface directly with a number of colour decoder ICs (e.g. TDA3563, TDA3562A).
26	$\overline{OD}$	Output disable causing R, G, B and $\overline{VDS}$ outputs to go to high-impedance state. Can be used at dot-rate.
27	CLKO	12 MHz clock output for hard-copy dot synchronization (referenced to output dots).
28	SAND	Sandcastle feedback output for SAA5230 teletext video processor or other circuit. Used when the display must be locked to the video source (e.g. VLP). The phase-lock part of the sandcastle waveform can be disabled to allow free-running of the SAA5230 phase-locked loop.
29	F1/F6	1,00699 MHz or 6,041957 MHz output.
30	F6	6,041957 MHz clock input (e.g. from SAA5230). Internal a.c. coupling is provided.
31	VCS/OSCO	Video composite sync input (e.g. from SAA5230) for phase reference of vertical display timing when locking to a video source (e.g. VLP) or, in stand-alone sync mode, output from internal oscillator circuit (fixed frequency).
32	$\overline{TCS}$	Text composite sync input/output depending on master/slave status.
33	$\overline{FS}/\overline{DDA}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots).
34	$\overline{UDS}$	Upper data strobe input/output.
35	$\overline{LDS}$	Lower data strobe output.
36	$\overline{DTACK}$	Data transfer acknowledge (open drain output).
37	$\overline{BR}$	Bus request to microprocessor (open drain output).
38	$\overline{AS}$	Address strobe output to external address latches.
39	R/$\overline{W}$ ($\overline{S}$/R)	Read/write input/output. Also serves as send/receive for the link-through buffer.
40	V_{DD}	Positive supply voltage (+ 5 V).

PINNING (continued)

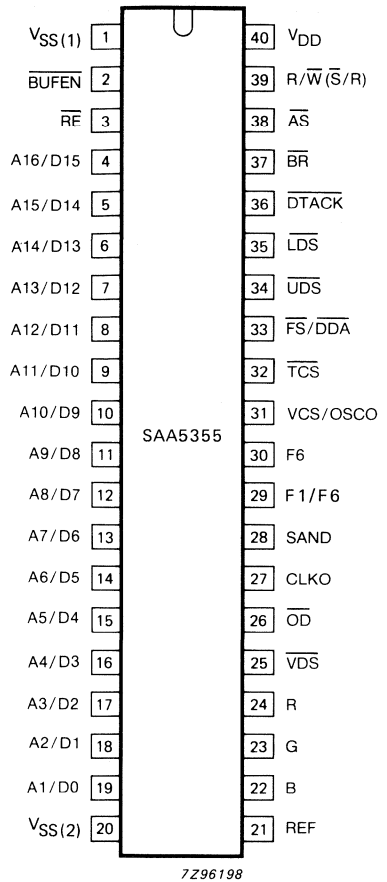


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}	−0,3 to + 7,5 V
Maximum input voltage (except F6, $\overline{TCS}$, REF)	V_{Imax}	−0,3 to + 7,5 V
Maximum input voltage (F6, $\overline{TCS}$)	V_{Imax}	−0,3 to + 10,0 V
Maximum input voltage (REF)	V_{REF}	−0,3 to + 3,0 V
Maximum output voltage	V_{Omax}	−0,3 to + 7,5 V
Maximum output current	I_{Omax}	10 mA
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V ± 5%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 40)	V_{DD}	4,75	5,0	5,25	V
Supply current (pin 40)	I_{DD}	–	–	350	mA
INPUTS					
F6 (note 1)					
Slave modes (Fig. 3)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	7,0	V
Input peaks relative to 50% duty factor	$\pm V_P$	0,2	–	3,5	V
Input leakage current at V_I = 0 to 10 V; T_{amb} = 25 °C	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	12	pF
Stand-alone mode (Fig. 4)					
Series capacitance of crystal	C_1	–	28	–	fF
Parallel capacitance of crystal	C_0	–	7,1	–	pF
Resonance resistance of crystal	R_r	–	–	60	Ω
Gain of circuit	G	–	–	*	V/V
$\overline{\text{BUFEN}}$, $\overline{\text{RE}}$, $\overline{\text{OD}}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input current at V_I = 0 to V_{DD}+ 0,3 V; T_{amb} = 25 °C	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
REF (Fig. 5)					
Input voltage	V_{REF}	0	1 to 2	2,7	V
Resistance (pin 21 to pin 20) with REF supply and R, G, B outputs OFF	R_{REF}	–	125	–	Ω

* Value under investigation.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS					
SAND					
Output voltage high level at I_O = 0 to −10 μA	V_{OH}	4,2	–	V_{DD}	V
Output voltage intermediate level at I_O = −10 to + 10 μA	V_{OI}	1,3	2,0	2,7	V
Output voltage low level at I_O = 0,2 mA	V_{OL}	0	–	0,2	V
Load capacitance	C_L	–	–	130	pF
F1/F6, CLKO, $\overline{\text{DDA}}$/$\overline{\text{FS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
$\overline{\text{LDS}}$, $\overline{\text{AS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF
$\overline{\text{DTACK}}$, $\overline{\text{BR}}$ (open drain outputs)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	150	pF
Capacitance (OFF state)	C_{OFF}	–	–	7	pF
R, G, B (note 2)					
Output voltage HIGH (note 3) at I_{OH} = −100 μA; V_{REF} = 2,7 V	V_{OH}	2,4	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Output resistance during line blanking	R_{OBL}	–	–	150	Ω
Output capacitance (OFF state)	C_{OFF}	–	–	12	pF
Output leakage current (OFF state) at V_I = 0 to V_{DD} + 0,3 V; T_{amb} = 25 °C	I_{OFF}	−10	–	+ 10	μA

parameter	symbol	min.	typ.	max.	unit
$\overline{VDS}$					
Output voltage HIGH at $I_{OH} = -250\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 2$ mA	V_{OL}	0	–	0,4	V
Output voltage LOW at $I_{OL} = 1$ mA	V_{OL}	0	–	0,2	V
Output leakage current (OFF state) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_{OFF}	−10	–	+ 10	μA
INPUT/OUTPUTS					
VCS/OSCO					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input current (output OFF) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Load capacitance	C_L	–	–	50	pF
$\overline{TCS}$					
Input voltage HIGH	V_{IH}	3,5	–	10,0	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200$ to $100\ \mu A$	V_{OH}	2,4	–	6,0	V
Output voltage LOW at $V_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
A1/D0 to A16/D15, $\overline{UDS}$, R/$\overline{W}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TIMING (note 4)					
F6 (Fig. 3)					
Rise and fall times	t_r, t_f	10	–	80	ns
Frequency	f_{F6}	5,9	–	6,1	MHz
CLKO, F1/F6, R, G, B, $\overline{VDS}$ $\overline{FS}$/$\overline{DDA}$, $\overline{OD}$ (notes 5, 6 and Fig. 6)					
CLKO HIGH time	t_{CLKH}	25	–	–	ns
CLKO LOW time	t_{CLKL}	15	–	–	ns
CLKO rise and fall times	t_{CLKr} t_{CLKf}	–	–	10	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ change	t_{VCH}	10	–	–	ns
R, G, B, $\overline{VDS}$ valid to CLKO rise	t_{VOC}	10	–	–	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ valid	t_{COV}	–	–	60	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ floating after $\overline{OD}$ fall	t_{FOD}	0	–	30	ns
Skew between outputs R, G, B, $\overline{VDS}$	t_{VS}	–	–	20	ns
R, G, B, $\overline{VDS}$ rise and fall times	t_{Vr}, t_{Vf}	–	–	30	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ active after $\overline{OD}$ rise	t_{UOD}	0	–	60	ns
CLKO HIGH to $\overline{FS}$/$\overline{DDA}$ change	t_{DCH}	10	–	60	ns
$\overline{FS}$/$\overline{DDA}$ valid to CLKO rise	t_{DOC}	5	–	–	ns
F1 HIGH time (note 7)	t_{F1H}	–	500	–	ns
F1 LOW time (note 7)	t_{F1L}	–	500	–	ns
F6 HIGH time	t_{F6H}	–	83	–	ns
F6 LOW time	t_{F6L}	–	83	–	ns
$\overline{OD}$ to CLKO rise set-up	t_{ODS}	–	–	45	ns
$\overline{OD}$ to CLKO HIGH hold	t_{ODH}	–	–	0	ns
MEMORY ACCESS TIMING (notes 8, 9 and Fig. 7)					
$\overline{UDS}$, $\overline{LDS}$, $\overline{AS}$					
Cycle time	t_{cyc}	–	500	–	ns
$\overline{UDS}$ HIGH to bus-active for address output	t_{SAA}	75	–	–	ns
Address valid set-up to $\overline{AS}$ fall	t_{ASU}	20	–	–	ns
Address valid hold from $\overline{AS}$ LOW	t_{ASH}	20	–	–	ns
Address float to $\overline{UDS}$ fall	t_{AFS}	0	–	–	ns

parameter	symbol	min.	typ.	max.	unit
$\overline{AS}$ LOW to $\overline{UDS}$ fall delay	t_{ATD}	50	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ HIGH time	t_{HDS}	220	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ LOW time	t_{LDS}	200	–	–	ns
$\overline{AS}$ HIGH time	t_{HAS}	125	–	–	ns
$\overline{AS}$ LOW time	t_{LAS}	320	–	–	ns
$\overline{AS}$ LOW to $\overline{UDS}$ HIGH	t_{AUH}	305	–	–	ns
Data valid set-up to $\overline{UDS}$ rise	t_{DSU}	30	–	–	ns
Data valid hold from $\overline{UDS}$ HIGH	t_{DSH}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{AS}$ rise delay	t_{UAS}	0	–	15	ns
$\overline{AS}$ LOW to data valid	t_{AFA}	–	–	275	ns
Link-through buffers (notes 8, 9 and Fig. 8)					
$\overline{BUFEN}$ LOW to output valid	t_{BEA}	–	–	100	ns
Link-through delay time	t_{LTD}	–	–	85	ns
Input data float prior to direction change	t_{IFR}	0	–	–	ns
Output float after direction change	t_{OFR}	–	–	60	ns
Output float after $\overline{BUFEN}$ HIGH	t_{BED}	–	–	60	ns
Microprocessor READ from FTFROM (Fig. 9)					
R/$\overline{W}$ HIGH set-up to $\overline{UDS}$ fall	t_{RUD}	0	–	–	ns
$\overline{UDS}$ LOW to returned-data access time	t_{UDA}	–	–	210	ns
$\overline{RE}$ LOW to returned data access time	t_{REA}	–	–	210	ns
Data valid to $\overline{DTACK}$ LOW delay	t_{DTL}	40	–	–	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ fall	t_{UDR}	0	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DSD}	250	–	350	ns
Address valid to $\overline{UDS}$ fall	t_{AUL}	0	–	–	ns

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
MEMORY ACCESS TIMING (continued)					
Microprocessor WRITE to FTFROM (Fig. 10)					
Write cycle time (note 10)	t_{WCY}	500	–	–	ns
R/$\overline{W}$ LOW set-up to $\overline{UDS}$ fall	t_{WUD}	0	–	–	ns
$\overline{RE}$ LOW to $\overline{UDS}$ fall	t_{RES}	30	–	–	ns
Address valid to $\overline{UDS}$ fall	t_{ASS}	30	–	–	ns
$\overline{UDS}$ LOW time	t_{LUS}	100	–	–	ns
Data valid to $\overline{UDS}$ rise	t_{DSS}	80	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DTA}	0	–	60	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ rise	t_{UDW}	0	–	–	ns
F1/F6 to memory access cycle (Fig. 11)					
$\overline{UDS}$ HIGH to F6 (component of F1/F6) rise	t_{UF6}	20	–	–	ns
F6 (component of F1/F6) HIGH to $\overline{UDS}$ rise	t_{F6U}	40	–	–	ns
SYNCHRONIZATION and BLANKING					
$\overline{TCS}$, SAND, $\overline{FS}$/$\overline{DDA}$					
See Fig. 12 for timing relationships and Fig. 13 for vertical sync and blanking waveforms.					

Notes to the characteristics

1. Pin 30 must be biased externally.
2. 16-level analogue voltage outputs.
3. Output voltage guaranteed when programmed for top level.
4. All timings are related to a 6,00 MHz clock.
5. CLKO, R, G, B, F1/F6, $\overline{VDS}$: C_L = 25 pF.
   $\overline{FS}$/$\overline{DDA}$: C_L = 50 pF
6. CLKO, F1/F6, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$: reference levels = 0,8 to 2,0 V
   R, G, B: reference levels = 0,8 to 2,0 V with V_{REF} = 2,7 V
7. These times may momentarily be reduced to a nominal 83 ns in slave-sync mode at the moment of re-synchronization.
8. C_L = 150 pF.
9. Reference levels = 0,8 to 2,0 V.
10. Microprocessor write cycle times of less than 500 ns are permitted but often result in Wait States being generated, the precise timing of $\overline{DTACK}$ will than depend on the internal synchronization time.

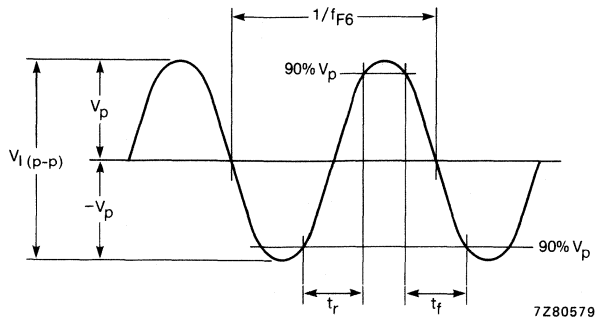
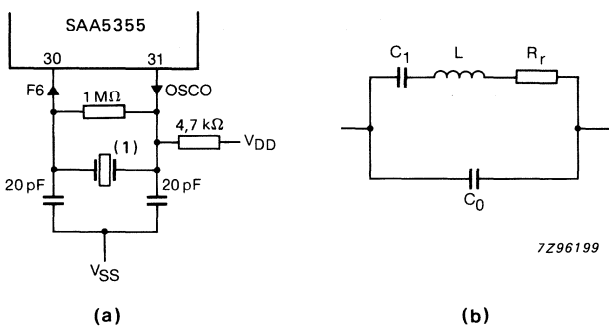


Fig. 3 F6 input waveform.



(1) for 525-line operation, frequency = 6,041957 MHz.

Fig. 4(a) Oscillator circuit for SAA5355 stand-alone sync mode and (b) equivalent circuit of crystal at resonance (see **characteristics** for values).

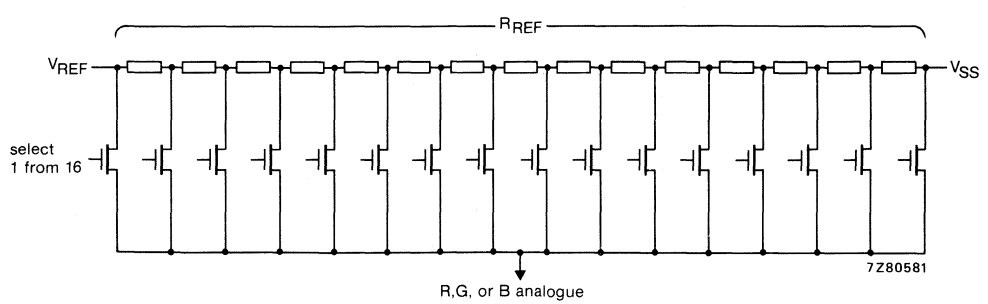


Fig. 5 Circuit arrangement giving one-of-sixteen reference voltage levels for the R, G or B analogue outputs.

DEVELOPMENT DATA

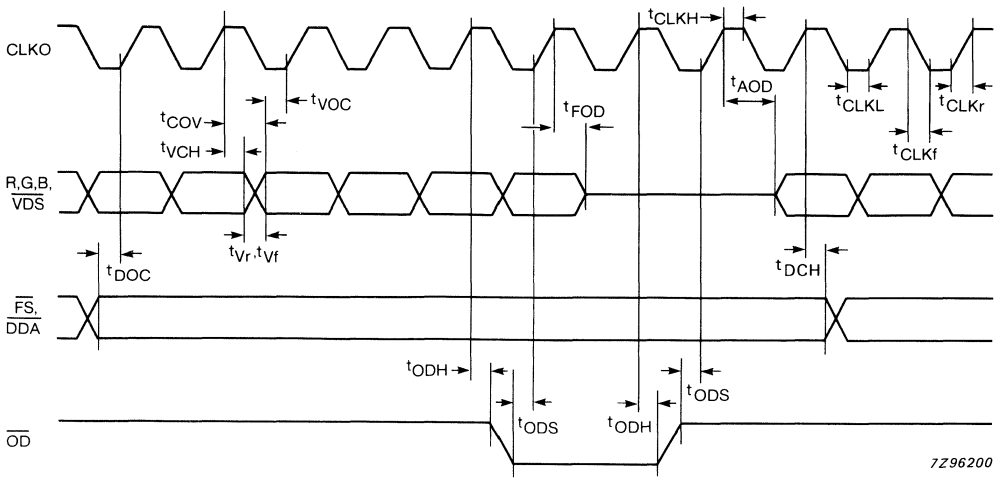


Fig. 6 Video timing.

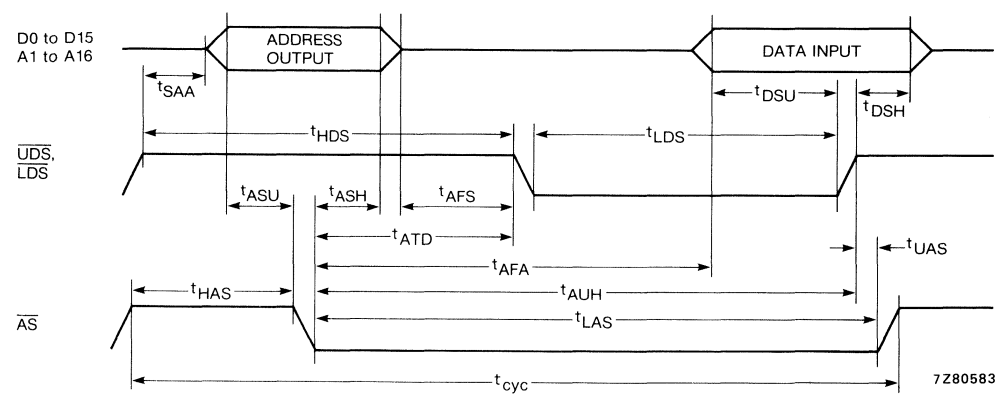


Fig. 7 Memory access timing.

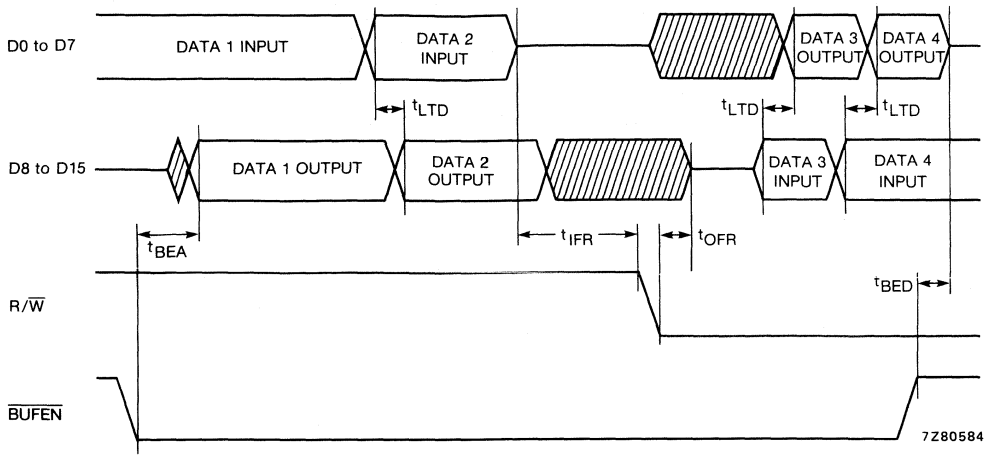


Fig. 8 Timing of link-through buffers.

DEVELOPMENT DATA

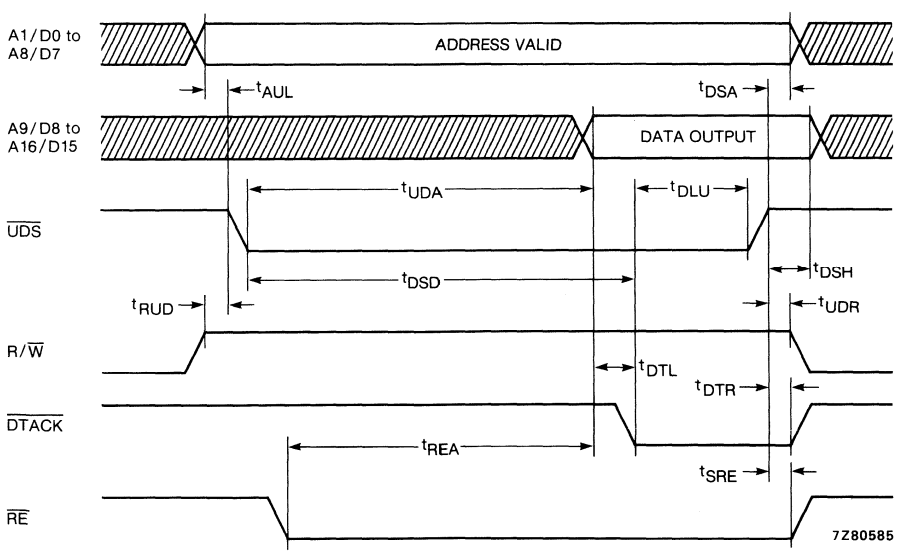


Fig. 9 Timing of microprocessor read from FTFROM.

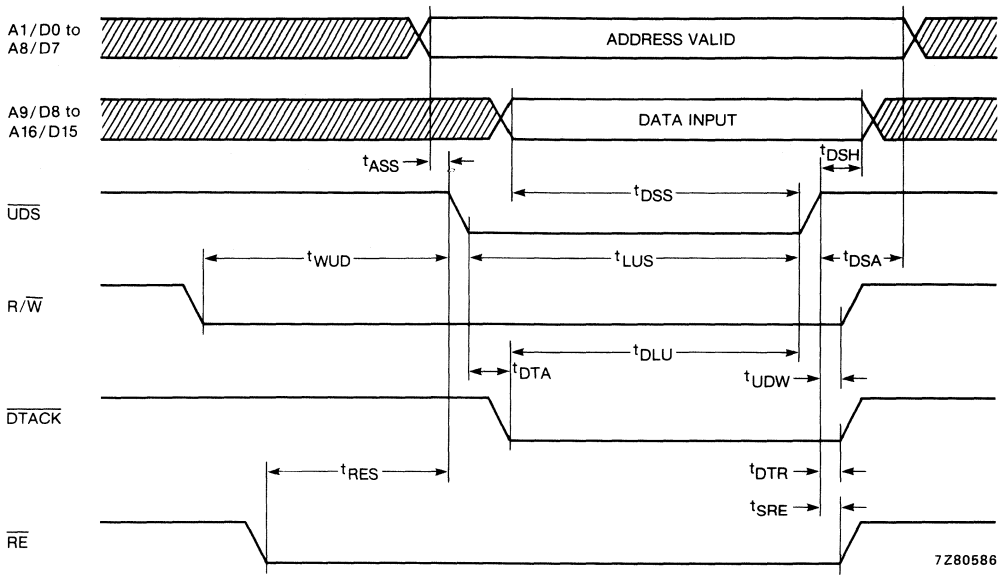


Fig. 10 Timing of microprocessor write to FTFROM.

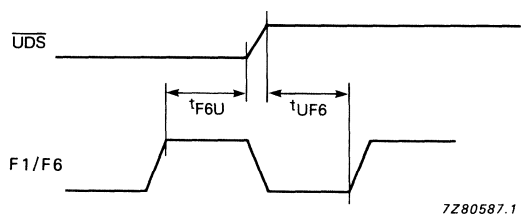


Fig. 11 Timing of F1/F6 to memory access cycle.

DEVELOPMENT DATA

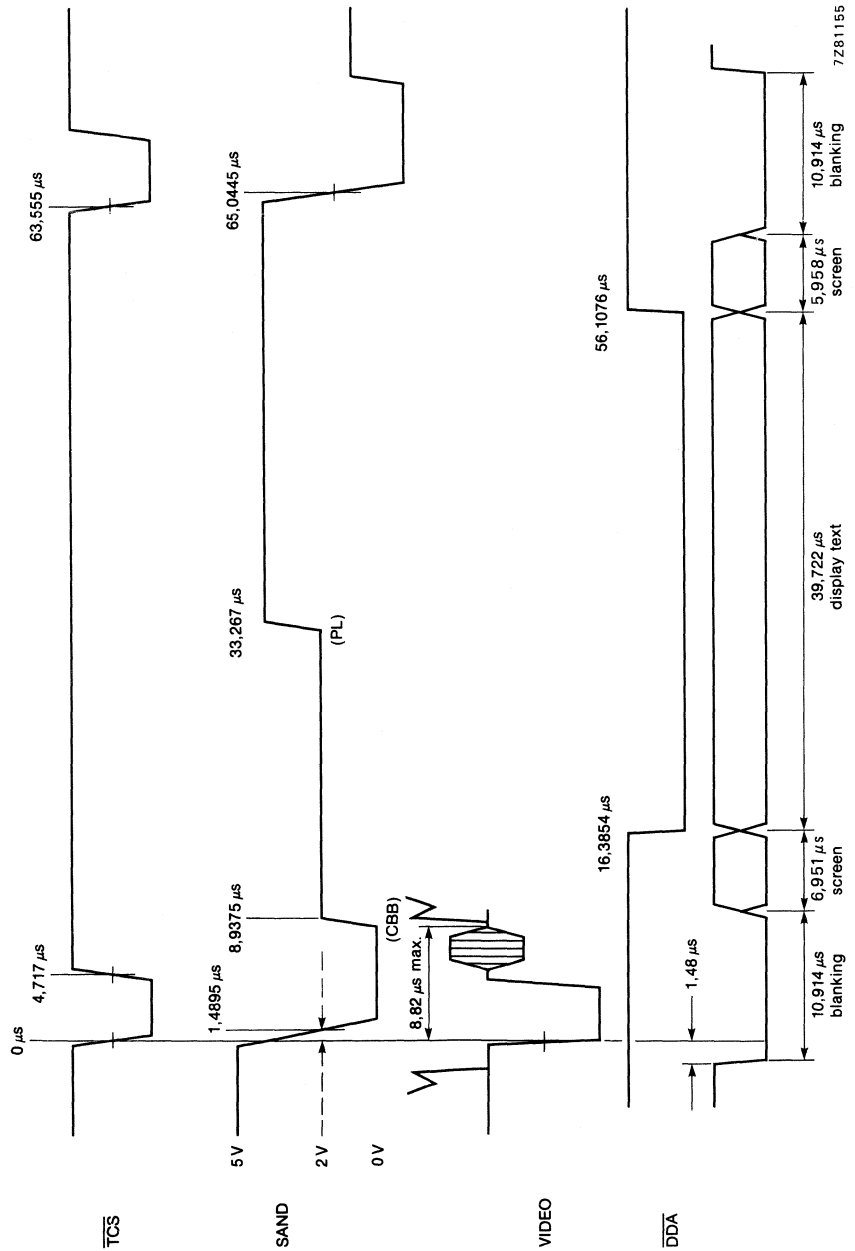


Fig. 12 Timing of synchronization and blanking outputs; all timings are nominal and assume $f_{F6} = 6{,}041957$ MHz.

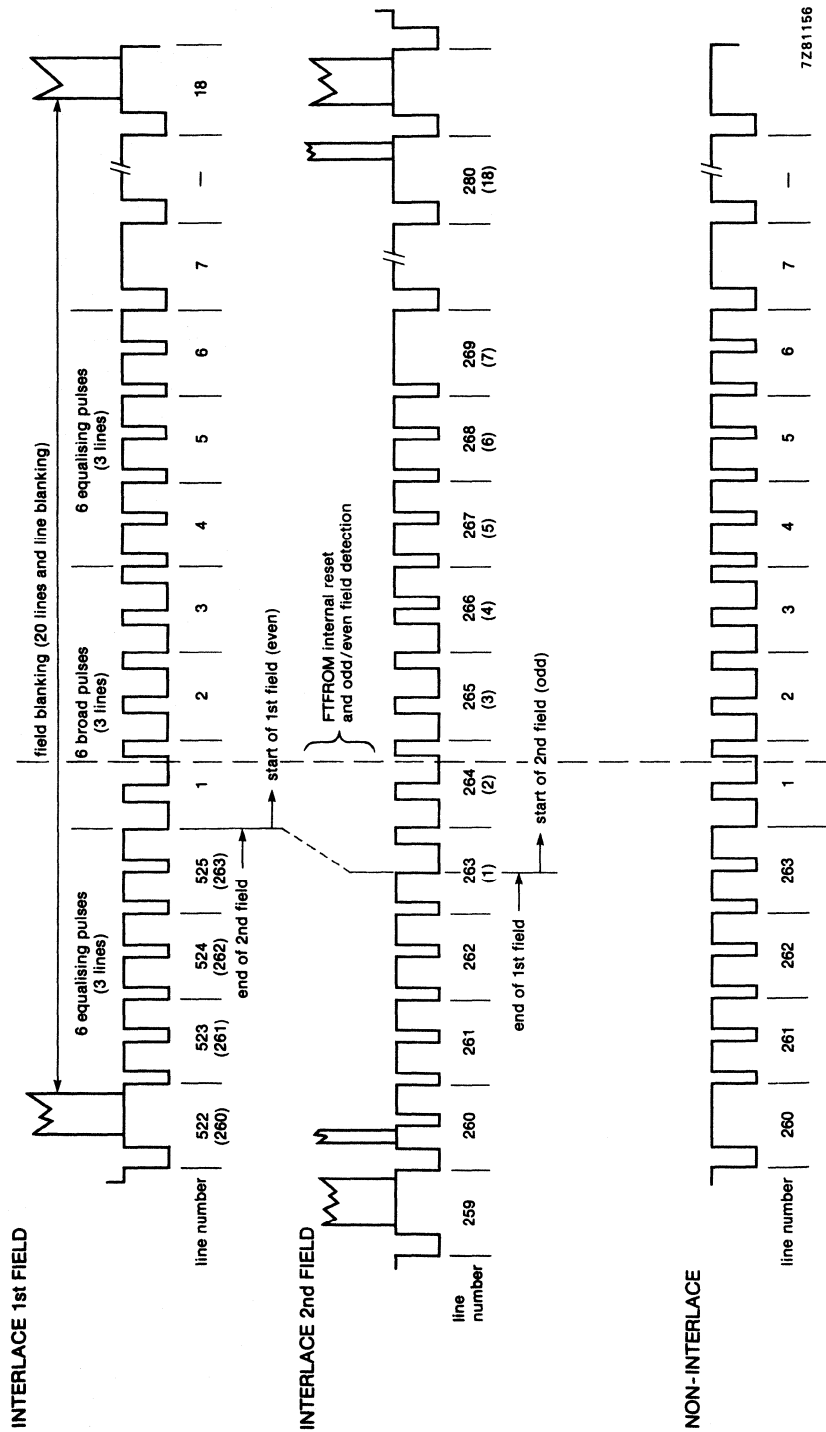


Fig. 13 Vertical synchronization and blanking waveforms; separation of broad pulses = 4,717 μs; equalizing pulse widths = 2,23 μs.

APPLICATION INFORMATION

More detailed application information is available on request

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Fig. 14, reference should also be made to the block diagram Fig. 1.

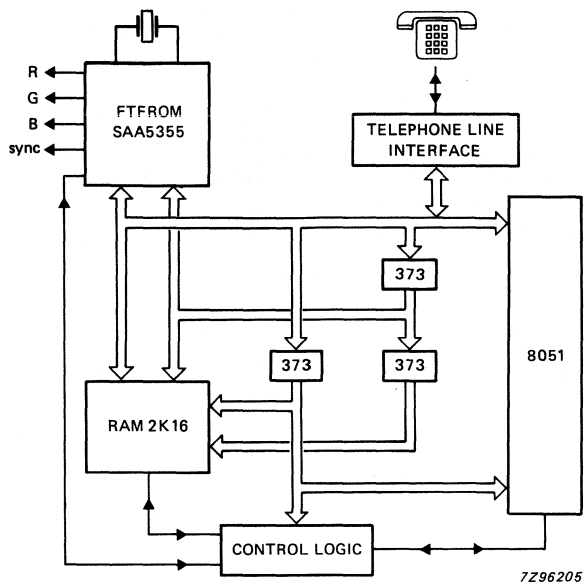


Fig. 14 Basic videotex decoder configuration.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows – each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colours, and during the display time it is also used for addressing DRCS characters.

Timing

The timing chain operates from an external 6,041957 MHz clock or an on-chip fixed-frequency crystal oscillator. The basic video format is 40 characters per row, 20/21 rows per page and 10 video lines per row. FTFROM will also operate with 25 rows per page and 9 video lines per row.

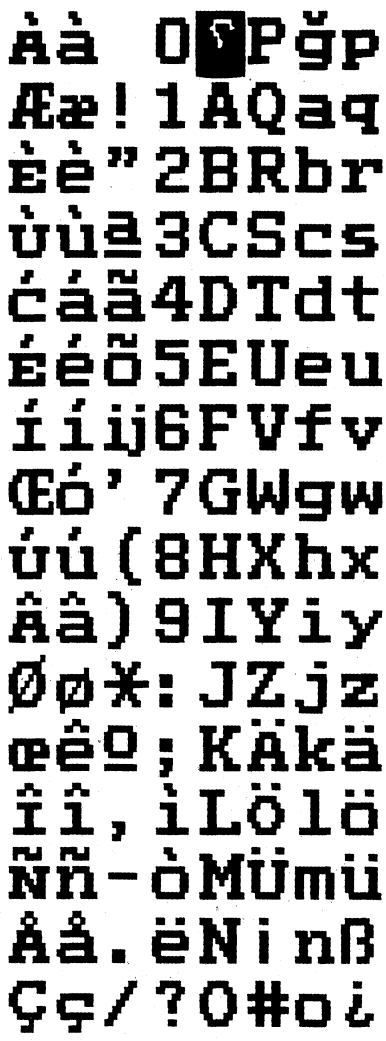
The display is generated to the normal 525-line/59,94 Hz scanning standard (interlaced or non-interlaced). In addition to composite sync (pin 32) for conventional timebases, a clock output at approximately 1 MHz or 6 MHz (pin 29) is available for driving other devices, and a clock output (pin 27) is available for hard-copy dot synchronization. A defined-display-area timing signal (pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

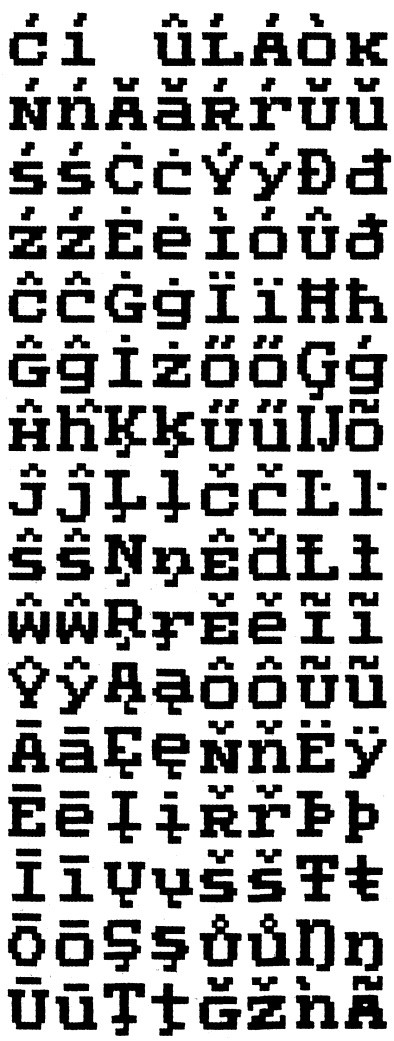
Character generation

FTFROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters and four are stored in an external RAM. The fixed character tables (Tables 0 to 3), shown in Figs 15 and 16, are applicable to 10-lines-per-row applications. For 9 lines per row applications, the characters will be as shown but with the last line removed from alpha characters and line 5 (labelling 0 to 9) removed from mosaic and line drawing characters.



7Z96211

(a)

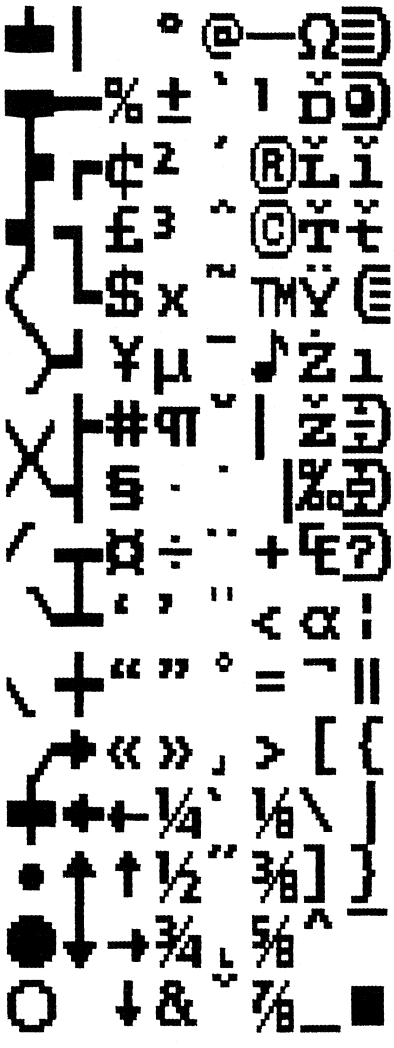


7Z96212

(b)

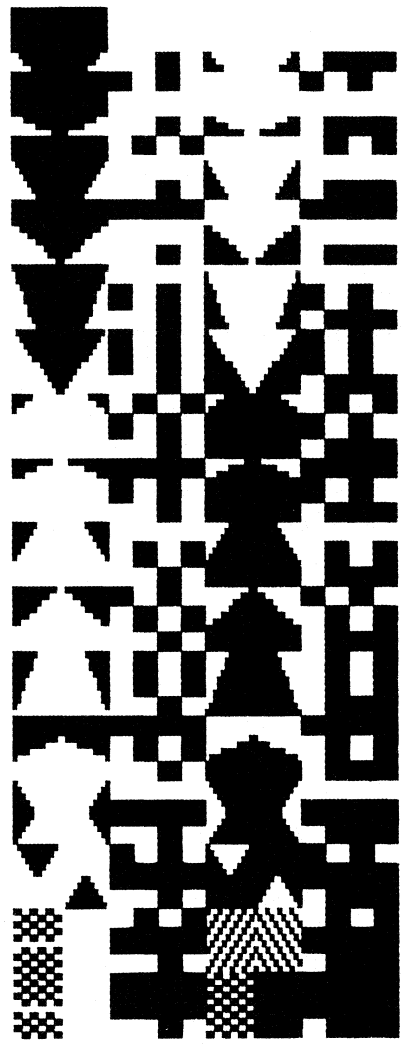
Fig. 15 On-chip characters: (a) Table 0; (b) Table 1.

DEVELOPMENT DATA



7Z96213

(a)



7Z96214

(b)

Fig. 16 On-chip characters: (a) Table 2; (b) Table 3.

APPLICATION INFORMATION (continued)

Character generation (continued)

The 128 most commonly used characters are contained in Table 0, these are the standard upper and lower-case letters of the Roman alphabet, numerals, punctuation and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set and accents without associated symbols are contained in Table 2. Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row so allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.
Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Colour map and digital-to-analogue converters

The colour map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D-A converter. The resulting R, G and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground colour, background colour, lining and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-Videotex applications, the device will also support the following operating modes:

Explicit fill mode. An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode. When operating with 80 characters per row, the available display attributes are eight foreground colours, eight (potentially different) background colours (including transparent) as well as underline and blink.

Full field DRCS mode. This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a 'bit map'. All ROM-based characters and all display attributes remain available.

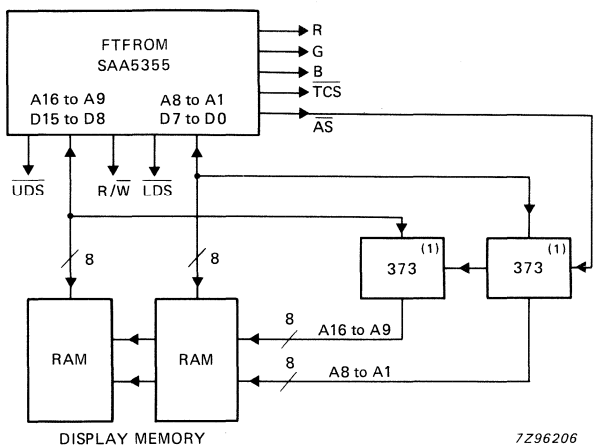
MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

- FTFROM fetches data from the display memory
- The microprocessor reads from, or writes to, FTFROM's internal register map
- The microprocessor accesses the display memory

FTFROM access to display memory (Figs 17 and 18)

FTFROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 496,5 ns (F6 = 6,041957 MHz). The address strobe ($\overline{AS}$) signal from FTFROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most-significant) and lower (least-significant) display information and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/$\overline{W}$ is included although FTFROM only reads from the display memory.



(1) 74LS373 octal transparent latch (3-state)

Fig. 17 Simple RAM interface circuit for display memory access.

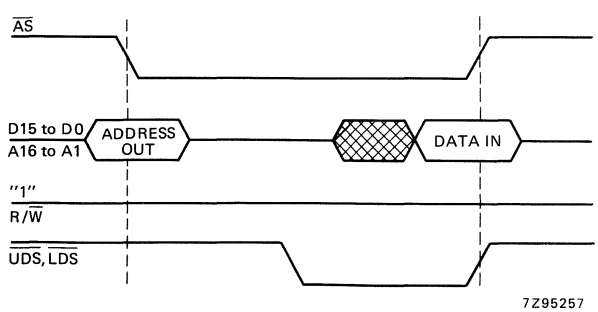


Fig. 18 Bus timing for display memory access.

APPLICATION INFORMATION (continued)

FTFROM access to display memory (continued)

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even numbered bytes use the upper (most-significant) part of the bus as shown in Fig. 19. The word addresses are numerically the same as the upper byte that they contain — there are no odd-numbered word addresses.

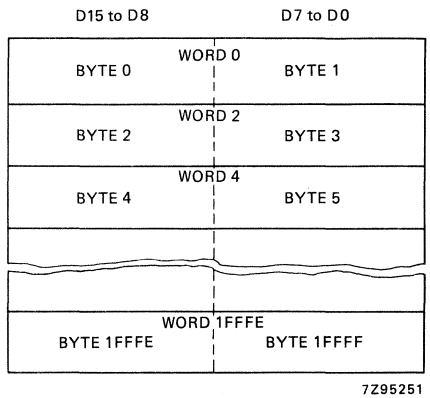


Fig. 19 Display memory word/byte organization.

Warning time

As FTFROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by FTFROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and FTFROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that FTFROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of FTFROM's bus activity is programmable to be between 0 and 22,84 μs.

Microprocessor access to register map

FTFROM has a set of internal registers which, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of the data bus (Fig. 20). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

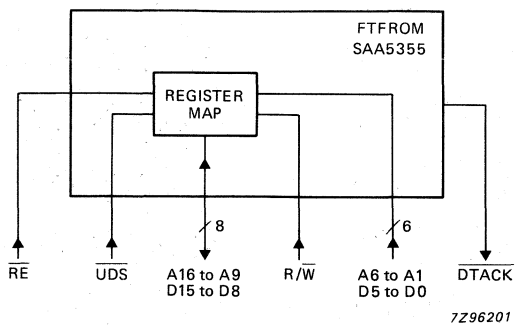


Fig. 20 Microprocessor access to register map.

The main data and address paths used in a connected 68000 interface are shown in Fig. 21. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to FTFROM via the octal buffers (74LS244). At the same time the bidirectional buffers (74LS245) disable the signals from the low order data bus of the 68000.

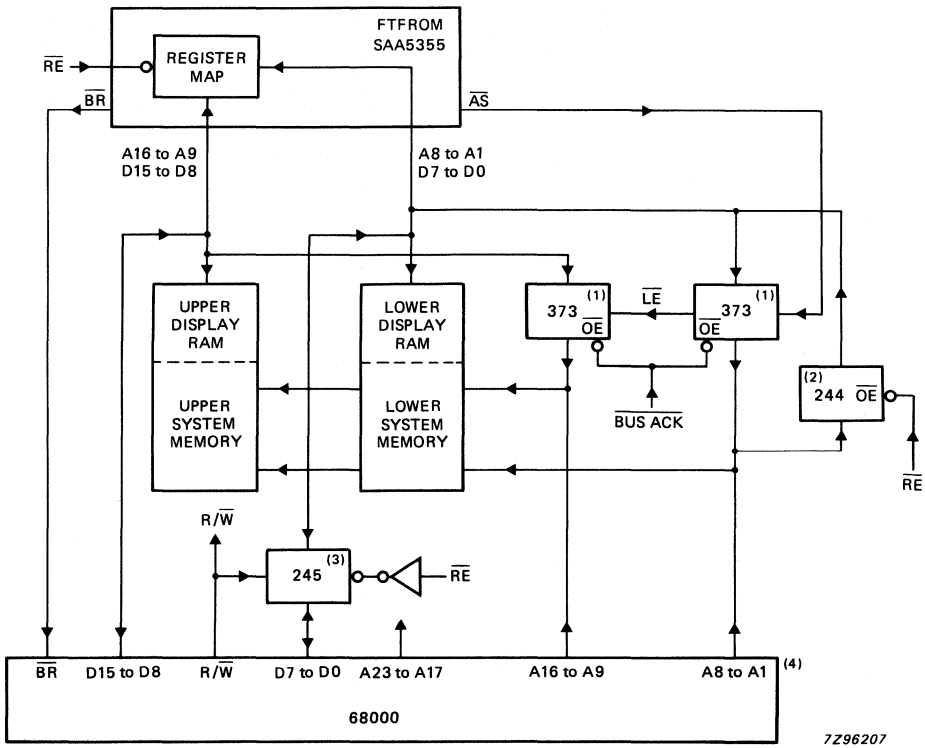
The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by FTFROM as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of FTFROM's scroll map contents at a location in its main memory.

8-bit microprocessors

Although the control bus is optimised for the SCN68000 16-bit microprocessor unit, FTFROM will operate with a number of widely differing industry-standard 8, 16 or more-bit microprocessors or microcontrollers (e.g. SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit wide display memory is made simple by FTFROM's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}$/R.

The main data and address paths used in a connected 8-bit microprocessor system are shown in Fig. 22. The interface is similar to that of the 16-bit system but here the display memory does not receive A0 as an address, rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when HIGH).

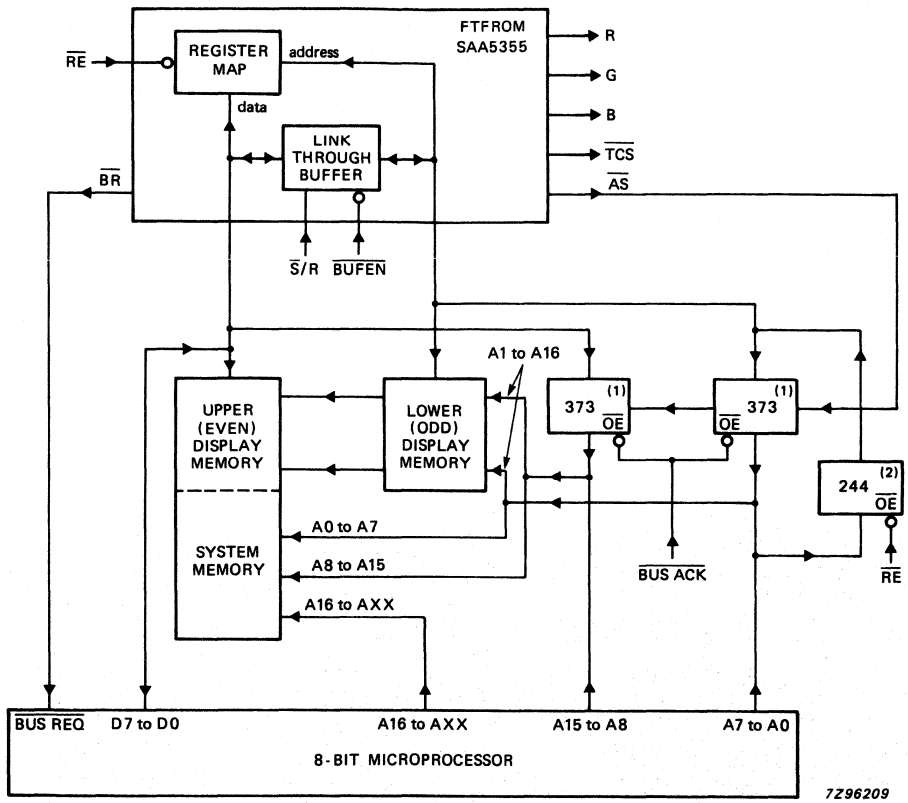
APPLICATION INFORMATION (continued)



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal transceiver (3-state)
(4) SCN68000 microprocessor unit

Fig. 21 Connected 16-bit microprocessor system.

DEVELOPMENT DATA



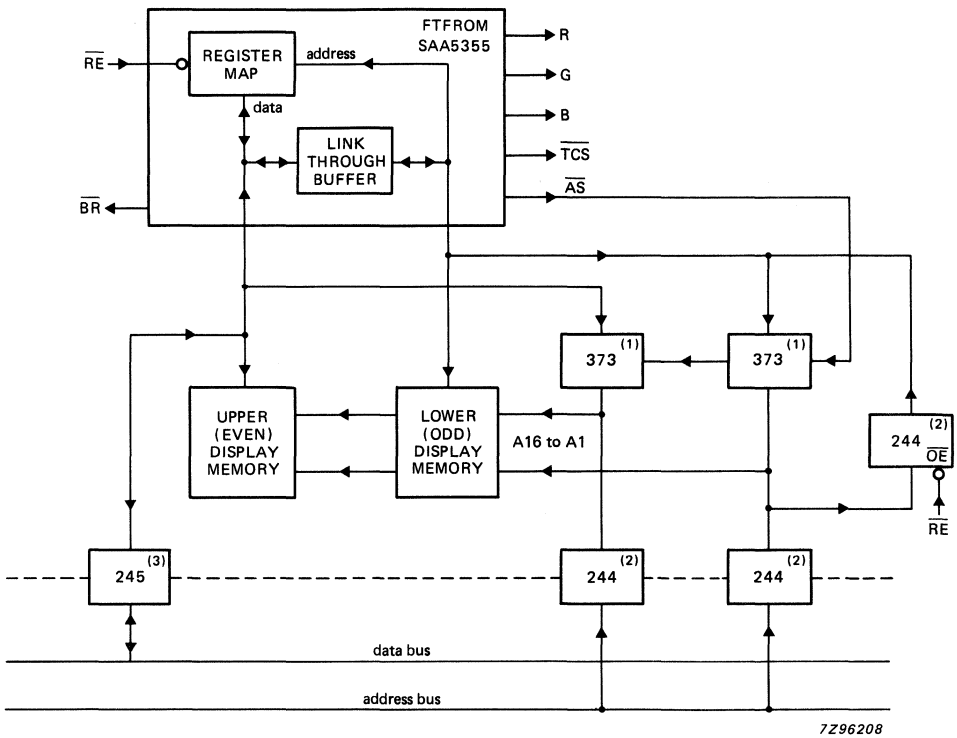
(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)

Fig. 22 Connected 8-bit microprocessor system.

APPLICATION INFORMATION (continued)

Disconnected systems

For many applications it may be desirable to disconnect FTFROM and the display memory from the microprocessor and its ROM, RAM and other peripherals by using isolating buffers as shown in Fig. 23. The two parts of the system then operate independently and communicate only when the microprocessor accesses FTFROM's register map or the display memory.



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal bus transceiver (3-state)

Fig. 23 Disconnected 8-bit system.

Synchronization

Stand-alone mode

As a stand-alone device (e.g. in terminal applications) FTFROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 6,041957 MHz on-chip oscillator using an external crystal as shown in Fig. 24.

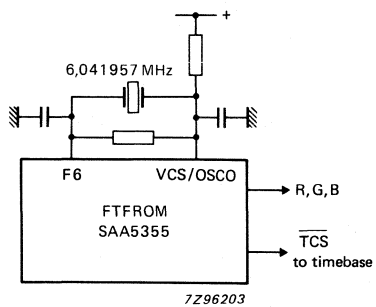


Fig. 24 Stand-alone synchronization mode.

Simple-slave

In the simple-slave mode FTFROM synchronizes directly to another device as shown in Fig. 25. FTFROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250 ns is built in to avoid resetting the counter at every tv line and so prevents screen jitter.
Field synchronization is made using FTFROM's internal field sync separator.

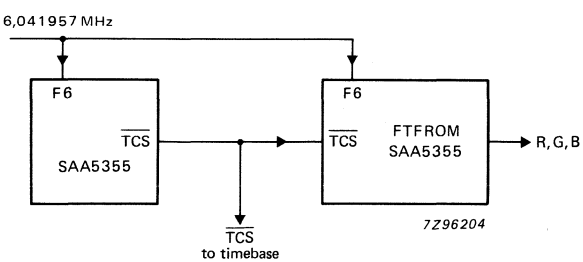


Fig. 25 Simple-slave (direct sync) mode.

APPLICATION INFORMATION (continued)

Synchronization (continued)

Phase-locked slave

The phase-locked slave (indirect sync) mode is shown in Fig. 26. A phase-locked VCO in the SAA5230 teletext video processor provides sync to the timebases. When FTFROM is active, its horizontal counter forms part of the phase control loop – a horizontal reference is fed back to the SAA5230 from the SAND output and a vertical reference is generated by feeding separated composite sync to FTFROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from FTFROM can sync with that from a tv source or a local VLP player, thus giving picture-in-text display possibilities.

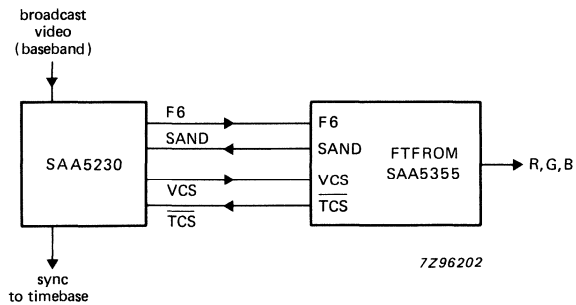


Fig. 26 Phase-locked slave (indirect sync) mode.

317K-BIT CCD MEMORY

GENERAL DESCRIPTION

The SAA9001 is a 1-bit wide, 317,520 bits long charge-coupled shift register, organized in 294 blocks of 1080 bits each. It is intended for use in a tv field memory at a maximum frequency of 21,3 MHz.

The IC is encapsulated in a 28-pin dual-in-line package of which only fifteen pins are used. Power supplies of + 5 and −3,5 V are required. All inputs, outputs and controls are TTL-compatible.

Control is performed by two external signals, memory clock (MC) and memory gating (MG). The circuit has two data inputs (MI_1 and MI_2) and the data may be internally recirculated. An adjustable delay of 0 to 7 bits is incorporated at the output to increment the total delay on a bit-by-bit basis, as programmed by the inputs A0, A1 and A2.

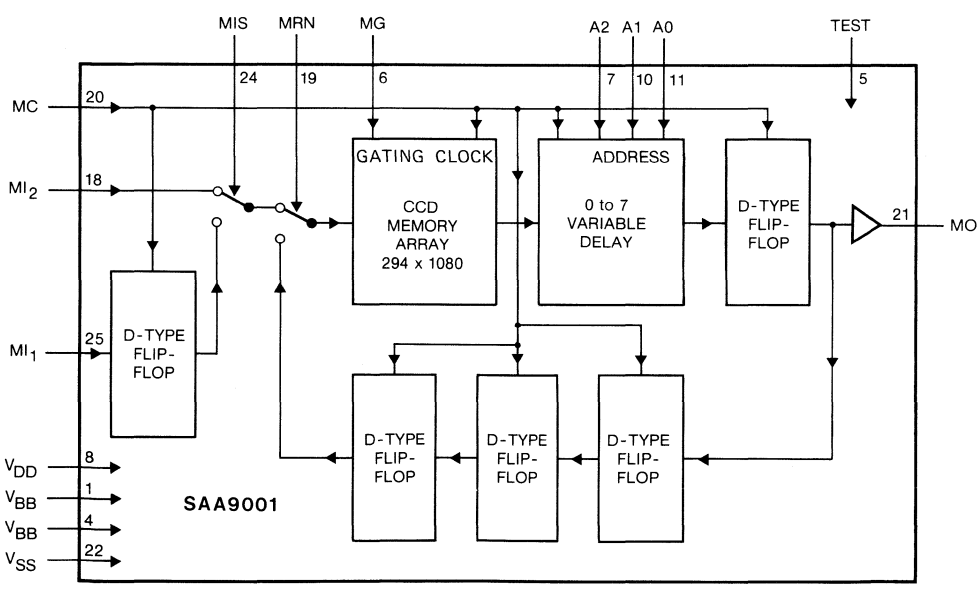


Fig. 1 Block diagram.

PACKAGE OUTLINES

SAA9001PB: 28-lead DIL; plastic (SOT-117).
SAA9001EB: 28-lead DIL; metal ceramic (CERDIL) (SOT-87B).

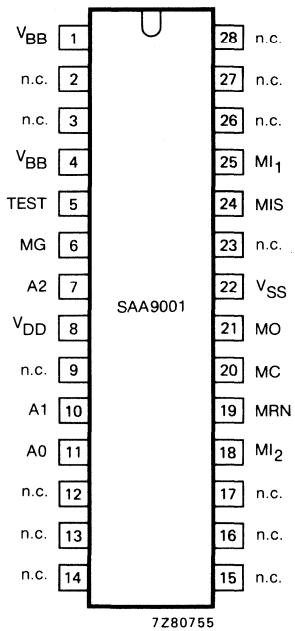


Fig. 2 Pinning diagram.

PINNING

1	V_{BB}	back-bias supply voltage (to be connected to pin 4)
4	V_{BB}	back-bias supply voltage (to be connected to pin 1)
5	TEST	control input for testing purposes only. It is internally connected to V_{SS} via a 1 kΩ (approx.) resistor and needs no external connection
6	MG	memory gating input
7	A2	control input for additional internal delay
8	V_{DD}	positive supply voltage
10	A1	control input for additional internal delay
11	A0	control input for additional internal delay
18	MI_2	memory input-2
19	MRN	memory recirculate control. Recirculation is activated when MRN is LOW
20	MC	memory clock input
21	MO	memory output
22	V_{SS}	negative supply voltage (ground)
24	MIS	memory input select; selects MI_1 or MI_2
25	MI_1	memory input-1

FUNCTIONAL DESCRIPTION

Operation

The memory array is organized to handle data in blocks of 1080 bits and has a capacity of 294 data blocks. The structure of the memory array provides fast, serial data input and output, with parallel transfer of data blocks through the memory. Memory input and output are controlled by the memory gating (MG), the serial output being initiated by the rising edge of MG and the storage of the data present in the memory's input register is performed on the falling edge of MG. In normal operation one cycle of MG is an uninterrupted HIGH level of at least 1080 clock periods (−4 or + 3 clock periods) followed by a LOW level of at least 32 clock periods. Input, output and gating signals are all referred to the rising edge of the memory clock (MC).

The internal recirculation facility is activated when the control input MRN is LOW.

Memory output

Output is enabled when MG is HIGH and data is clocked serially from the memory. Referring to Fig. 3, the first rising clock-edge after the positive transition of MG is defined as clock pulse "0". If the delay control address is A2 = A1 = A0 = 0, then the first bit of the output is valid at clock pulse "17" (the delay of 17 clock periods is due to internal multiplexing of the data in the memory).

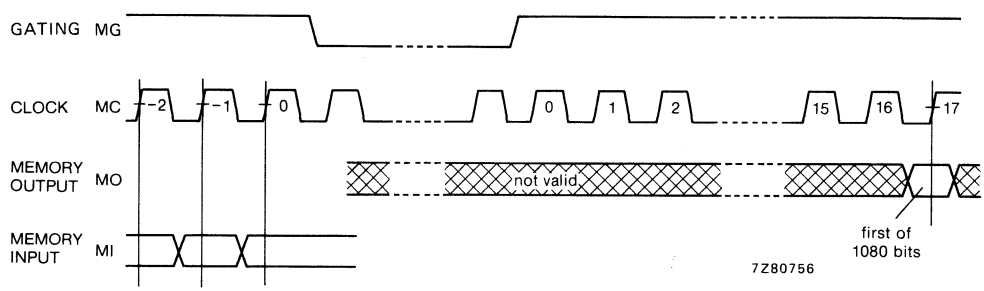


Fig. 3 Memory input and output data timings with respect to the memory clock (MC) for a memory gating (MG) HIGH period that is a multiple of 8 clock periods (no internal rounding of gating period).

The output delay can be increased by the values shown in Table 1 using the internal delay line controlled by A0, A1 and A2.

Table 1 Additional delay control

delay address			additional delay (clock periods)
A2	A1	A0	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

FUNCTIONAL DESCRIPTION (continued)

Data input

Data to be stored is directed to the memory from either MI_1 or MI_2 as selected by the control input MIS (see Table 2). The MI_1 input is delayed by one clock period.

Table 2 Input selection

control input	memory input
MIS = 0	MI_1
MIS = 1	MI_2

Input data is clocked serially into the input register of the CCD memory. When the negative transition of MG occurs, the 1080 bits of data present in the input register are entered into the memory array. If the interval of MG = HIGH is not an exact multiple of eight clock periods then the timing of the negative transition of MG is internally rounded to be an exact multiple of eight clock periods. Note that the data path from input MI_1 has a delay of one clock period and the path from MI_2 is direct.

The length of the MG = HIGH interval required for internal and external recirculation of data is determined as shown in Fig. 4. The positive transition of MG (waveform 1) initiates the serial transfer of data from the output register. Due to multiplexing in the memory, valid data is available after 16 clock periods (waveform 2). After a delay of "A" clock periods, determined by A0, A1 and A2 (waveform 3), and a one-clock-period delay via a D-type flip-flop, the valid data is available at the output pin MO (waveform 4).

Incoming data can be delayed by two amounts: RP (waveform 5), a phase shift introduced when the data is recirculated through an external processing circuit; and ID (waveform 6), a one-clock-period delay when input MI_1 is selected. The negative transition of MG, internally rounded to a multiple of eight clock periods (waveform 7), initiates storage of the last 1080 bits presented at the memory input (waveform 6). Therefore, the MG = HIGH interval is 16 + A + 1 + RP + ID + 1080 clock periods, and this figure is rounded to a multiple of eight. From this, (A + 1 + RP + ID) modulo 8 = 0.

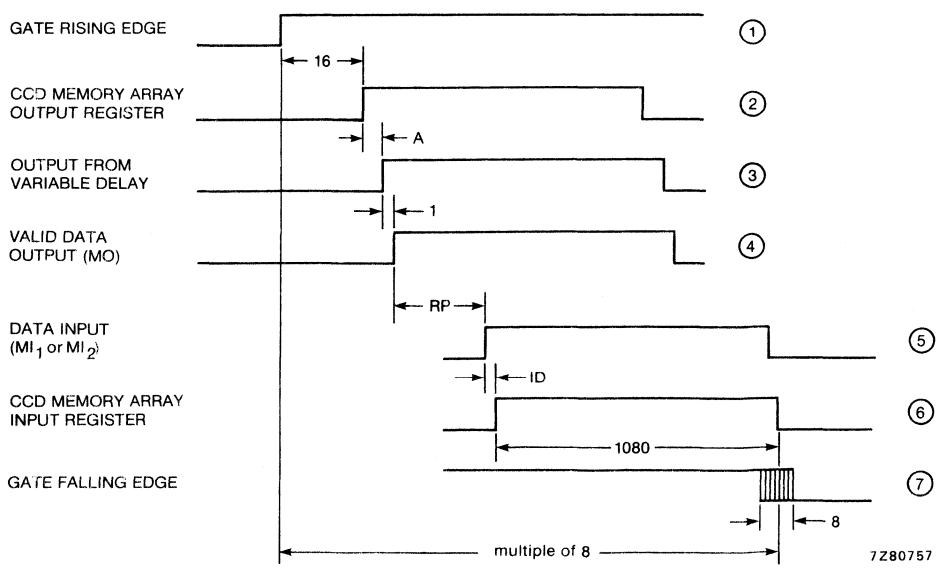


Fig. 4 Determination of memory gating HIGH period.

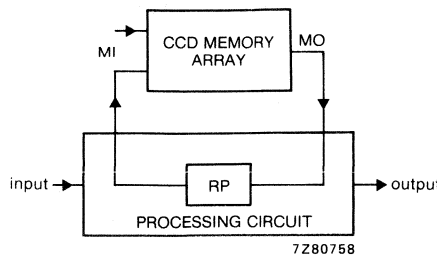


Fig. 5 Recirculation via an external circuit.

During internal recirculation of the data (MRN = LOW), the three D-type flip-flops in the recirculation path give RP a value of three clock periods and ID will be zero. Consequently, the variable delay should be programmed for a delay of A = 4 for proper data retention, i.e. (4 + 1 + 3 + 0) modulo 8 = 0.

In conclusion, to store 1080 bits of valid data and to retrieve at the output 1080 valid data bits, the MG = HIGH interval must be at least 1076 clock periods followed by an MG = LOW interval of at least 32 clock periods. The MG = LOW interval can be reduced to a minimum of 24 clock periods when MG = HIGH is a multiple of eight clock periods.

Fast gating

Fast gating is a method of accelerating the internal transfer of data through the memory at the expense of valid data and is therefore useful for skipping unwanted data blocks. The MG = HIGH interval for fast gating is less than 1076 clock periods to a minimum of 360 clock periods. If the MG = HIGH interval is a multiple of eight clock periods during fast gating, the MG = LOW interval can be reduced to 24 clock periods (min.), otherwise the MG = LOW interval must be at least 32 clock periods. The output data is not valid during fast gating and during the first two data blocks at the output after fast gating has ceased. No valid data is clocked into the input register of the CCD memory during fast gating.

Slow gating

The transfer of data can be decelerated by using slow gating. For this, the MG = HIGH or MG = LOW interval is extended to the maximum waiting time (t_{GW}).

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Voltage on any pin, except V_{BB} (pin 4) and MO (pin 21), with respect to V_{SS}	V_I, V_O	max.	7 V
Back-bias voltage	V_{BB}	min.	−7 V
D.C. output current (sink or source)	I_O	max.	10 mA
Operating ambient temperature range (under d.c. operating conditions)	T_{amb}		0 to 60 °C
Storage temperature range	T_{stg}		−65 to 150 °C
Total power dissipation per package	P_{tot}		1 W

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CAPACITANCE

parameter	symbol	max.	unit
Capacitance at:			
data inputs MI_1, MI_2 (pins 25 and 18)	C_I	9	pF
clock input MC (pin 20)	C_C	9	pF
gating input MG (pin 6)	C_G	9	pF
data output MO (pin 21)	C_O	9	pF
recirculation control MRN (pin 19)	C_{RN}	9	pF
input select control MIS (pin 24)	C_{IS}	9	pF
delay program inputs A0, A1, A2 (pins 11, 10 and 7)	C_A	9	pF

D.C. OPERATING CONDITIONS

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{DD}	4,75	–	5,25	V
Back-bias supply range	V_{BB}	−3,65	–	−3,35	V
Input voltage LOW	V_{IL}	−1,0	–	+ 0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V

D.C. CHARACTERISTICS

T_{amb} = 0 to + 60 °C; V_{DD} = 4,75 to 5,25 V; V_{BB} = −3,5 ± 0,15 V; output not loaded; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Input leakage current at V_i = GND to V_{DD}: MI_1; MI_2; MC; MG; A0; A1; A2; MRN; MIS	I_{LI}	–	–	10	μA
Power supply current from V_{DD} at f = 21,3 MHz	I_{DD}	–	–	70	mA
Output voltage LOW at I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH at I_{OH} = −1 mA	V_{OH}	2,4	–	–	V

A.C. TEST CONDITIONS

Input pulse levels	0,6 and 2,4	V
Rise and fall times between 0,8 and 2,0 V (t_r, t_f)		
clock input MC	$\leqslant 3$	ns
data inputs MI_1, MI_2; gating input MG; control inputs A0, A1, A2, MIS, MRN	$\geqslant 3$	ns
Timing reference levels		
clock input MC	1,5	V
data inputs MI_1, MI_2 and gating input MG	0,8 or 2,0	V
data output MO	0,8 or 2,0	V
Output load	see Fig. 6	

A.C. CHARACTERISTICS

T_{amb} = 0 to 60 °C; V_{DD} = 4,75 to 5,25 V; V_{BB} = −3,5 ± 0,15 V

parameter	symbol	min.	typ.	max.	unit
Clock frequency (note 1)	f_{CL}	–	–	21,3	MHz
Clock LOW time	t_{CL}	18	–	–	ns
Clock HIGH time	t_{CH}	18	–	–	ns
Recirculation time (note 1)	t_R	–	–	27	ms
Waiting time (gating LOW/HIGH time) (note 2)	t_{GW}	–	–	1100	μs
Gating set-up time	t_{GC}	7,5	–	–	ns
Gating hold time	t_{CG}	0,5	–	–	ns
Data set-up time	t_{IC}	7,5	–	–	ns
Data hold time	t_{CI}	0,5	–	–	ns
Output hold time	t_{OH}	5,0	–	–	ns
Output delay time	t_{OD}	–	–	23,5	ns
Output invalid after address change	t_{AH}	0	–	–	μs
Address valid after address change (note 3)	t_{AD}	–	–	7 clock pulses + 1	μs
Recirculation set-up time (note 4)	t_{MRNSU}	0	–	1	μs
Input select set-up time (note 5)	t_{MISSU}	0	–	1 clock pulse + 1	μs

Notes to the characteristics

1. The maximum recirculation time must never be exceeded by any combination of low frequency gating and/or waiting time.
2. Every 1300 μs at least three blocks of 1080 bits must be transferred to the output. This means that immediately after a wait of 1100 μs three blocks must be shifted out.
3. A change in delay will cause invalid data at the output for the time t_{AD}.
4. After a change of MRN, the signal recirculation path is not switched before t_{MRNSU}.
5. After a change of MIS, data at the input is invalid for t_{MISSU}.

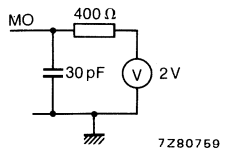


Fig. 6 Output load.

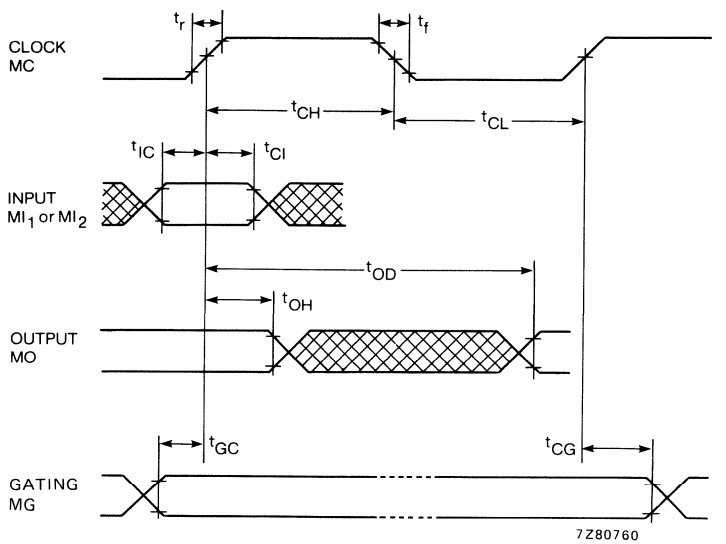


Fig. 7 Timing waveforms for gating and I/O.

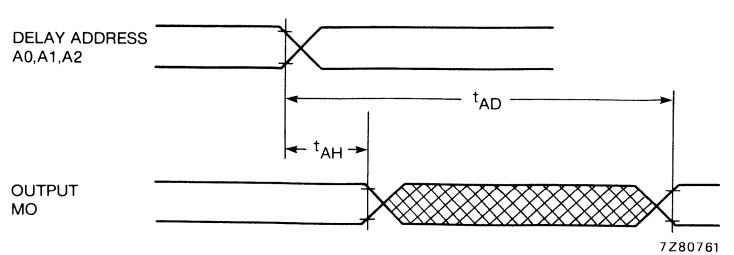


Fig. 8 Timing waveforms for address set-up and hold.

PICTURE ENHANCEMENT PROCESSOR

GENERAL DESCRIPTION

The SAA9010 picture enhancement processor (PEP), a 40-pin CMOS integrated circuit, is for application in memory-based feature tv receivers. It is part of the tv field memory system and provides picture quality enhancement by either cross-colour or noise reduction.

Additional features possible with the PEP, in conjunction with the field memory and controller SAA9020, are picture store/recall and still picture. It also forms part of a system that reduces teletext waiting time.

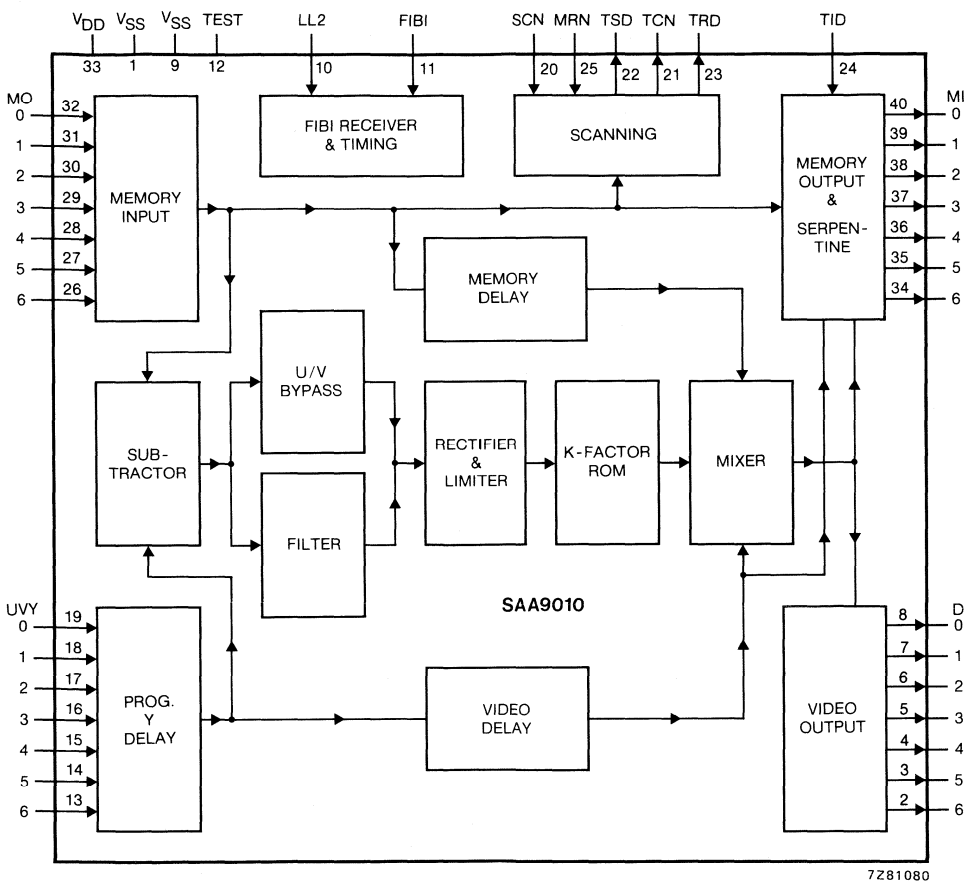


Fig. 1 Block diagram.

PACKAGE OUTLINE

40-lead DIL; plastic (SOT-129).

PINNING

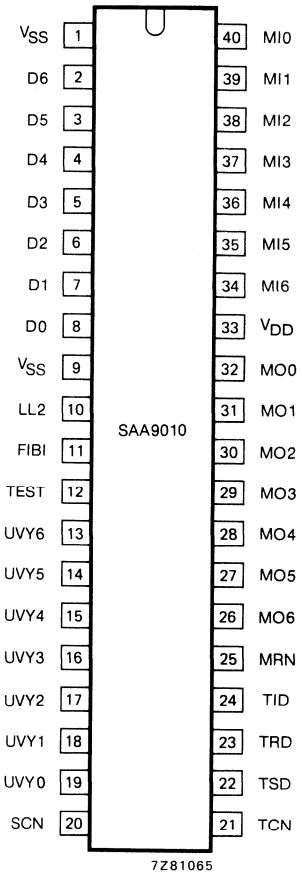


Fig. 2 Pinning diagram.

1,9	V_{SS}	negative supply voltage (0 V). Both pins must be connected to a common ground plane
8 to 2	D0 to D6	video data outputs to display. D6 is msb
10	LL2	20,25 MHz clock input
11	FIBI	format identification, blanking and instruction control input
12	TEST	test input. Connected to V_{SS} for normal operation
19 to 13	UVY0 to UVY6	video data input at 20,25 MHz bit rate in the order U V Y Y Y Y, U V Y Y Y Y, repeating. The magnitude of the Y samples is 7 bits with UVY6 as the msb. The U and V samples are two's complement, have a 6-bit magnitude, bit UVY5 is msb and UVY6 is the sign bit
20	SCN	scanning counter preset input. A rising edge of MRN during SCN = LOW presets the counter to MO0

21	TCN	terminal count output to indicate the end of a scan cycle. TCN = LOW when the scanning is on MO6
22	TSD	teletext scanned data output. Scanning is from MO0 to MO6 delayed by 2 LL2 cycles
23	TRD	teletext return data. Output data from the last memory (MO0) delayed by 2 LL2 cycles
24	TID	teletext input data for text mode. During text mode, data from TID delayed by 2 LL2 cycles is output on MI6
25	MRN	memory recirculate, valid LOW. Clock input to text scanning counter
32 to 26	MO0 to MO6	data inputs from memory. Format same as for UVY inputs
33	V_{DD}	positive supply voltage (+ 5 V). Must be decoupled to V_{SS}
40 to 34	MI0 to MI6	data outputs to memory

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Introduction (Fig. 3)

Video data is received into the PEP via the UVY inputs in a time-multiplexed data stream, the separate components of the data stream being identified by their time-relationship with FIBI. In order to adjust the relative positions of Y and U/V samples a programmable Y delay is provided. This can delay the Y samples from 0 to 31 Y-sample positions relative to a U/V sample to a maximum of 2,3 μs (31 x 1½ LL2 clock periods).

This video data is then subtracted from data entering via the MOn inputs to produce a difference signal. The Y components of the difference signal are filtered to reduce the residual subcarrier components. The difference signal is rectified and limited to provide part of the address to the K-factor ROM. The other components of the ROM address are mode control bits which can select fixed output values of 0, ½ or 1, or two different control ranges for noise reduction.

The K-factor ROM provides the control (K) input to a digital mixing unit which mixes the UVY and MO inputs to provide new data for the MI and D outputs. The transfer function of the mixer is:

$$(D) = (MI) = [K \times (UVY)] + [(1-K) \times MO)]$$

When the memories connected to MO and MI are being used for the storage of text data, the PEP provides routing to allow connection into serpentine mode in which new data enters the memories via TID and last data is returned via TRD.

The memory outputs can also be scanned one at a time using a built-in counter and multiplexer. The counter is under the control of SCN and MRN and data is output via TSD. TCN indicates the completion of a scan.

Control of the PEP is via a 15-bit data word inserted in the FIBI signal. FIBI, generated in the field memory controller (SAA9020), is also used to identify the positioning of the U/V and Y signals within the data streams.

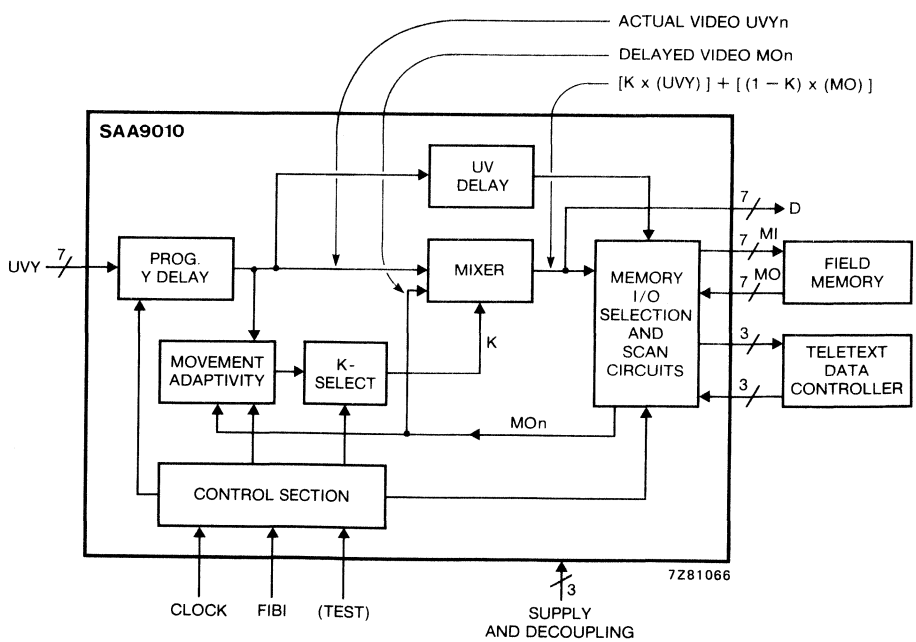


Fig. 3 Functional diagram.

DEVELOPMENT DATA

Noise reduction (Fig. 4)

In the noise reduction mode the field memory is connected in a feedback loop from the output to the input of the mixer, forming an integrating recursive filter. The effect of this is to combine each pixel with spatially corresponding pixels from the previous field. The field memory controller (SAA9020) alternates the length of the delay introduced by the memory so that it averages one field period. For standard signals the delay alternates between 312 and 313 or 262 and 263 lines, depending on the standard.

One of the four filters in the movement adaptivity circuit is selected to govern high-frequency noise behaviour. The different filters are optimized for the 5 MHz bandwidth of 625-line systems, the 4 MHz bandwidth of 525-line systems and the 3 MHz bandwidth of video recorders (see FIBI description and Fig. 9a).

The processed movement information is applied to a ROM which, via a transform curve, delivers the movement-adapted K-factor to the mixer. Either of two transform curves can be selected, one optimized for high noise levels and the other for low as shown in Fig. 9b.

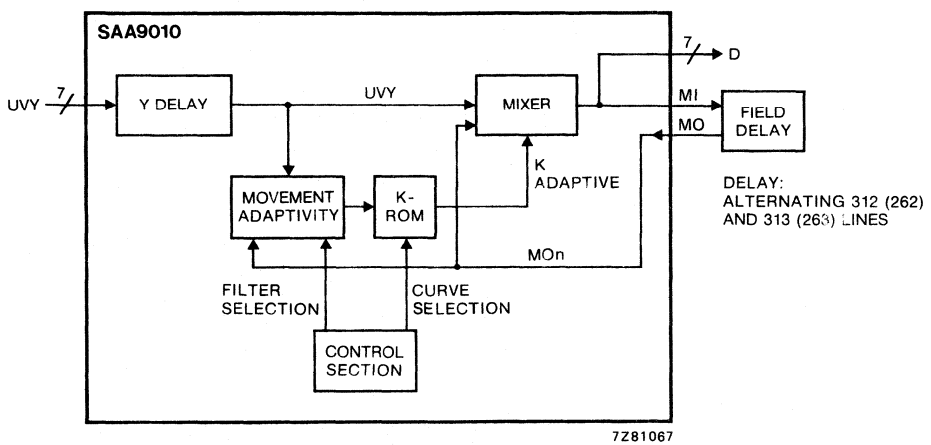


Fig. 4 Main signal flow during noise reduction.

Cross-colour reduction (Fig. 5)

During cross-colour reduction the UVY input signals go direct to the memory and the mixer output is directed to the data output D. In the mixer the factor K is set to 1 for the Y signal and to 0,5 for the UV signals. Therefore, the Y signal is unaffected and the UV signals at the mixer output represent the pixel-averages for two fields (transversal filtering).

The field memory controller (SAA9020) sets the field memory delay to an even number of lines for PAL or to an odd number of lines for NTSC. PAL or NTSC mode for cross-colour reduction can be selected independently of the number of lines per field.

Cross-colour reduction (continued)

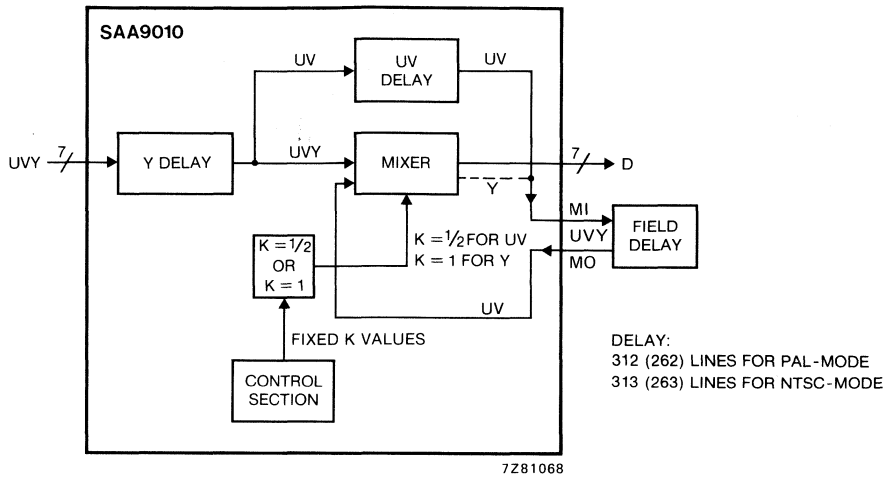


Fig. 5 Main signal flow for cross-colour reduction.

Stored picture mode (Fig. 6)

With one complete field of processed data loaded in the memory, the factor K is set to 1 causing the actual video to be bypassed to both D and MI outputs and the memory contents are retained by re-circulation. As long as the memory is kept in this mode, its output remains accessible and may also be used for obtaining hard copy of the stored data via a printer.

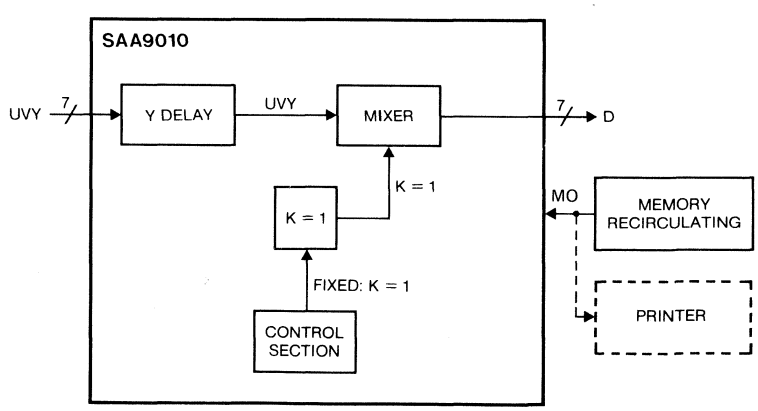


Fig. 6 Main signal flow during stored picture.

Still picture mode (Fig. 7)

When a stored picture is to be displayed, the factor K is set to 0 and the contents of the field memory are recirculated via the mixer. The field memory controller (SAA9020) sets the field period of the displayed picture to standard length in either interlaced or non-interlaced scan.

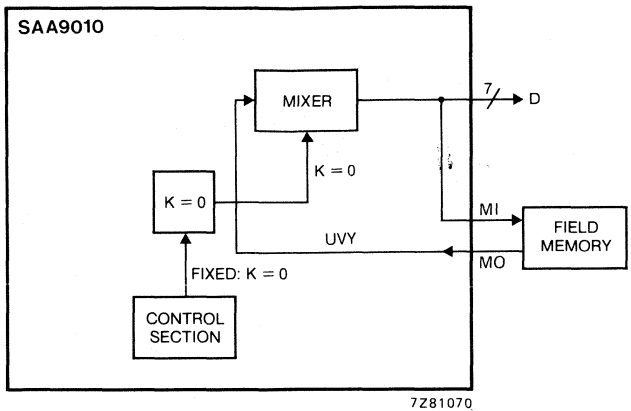


Fig. 7 Main signal flow during still picture.

Teletext mode (Fig. 8)

The factor K is set to 1 to bypass the actual video. The seven CCDs of the field memory, normally connected in parallel for video storage, are now connected in series (serpentine) by the memory I/O selection circuit.

After a page request by the user, the scanning circuit is activated by the background memory controller (SAA9030) which now also controls the memory gating and recirculation for this mode of operation.

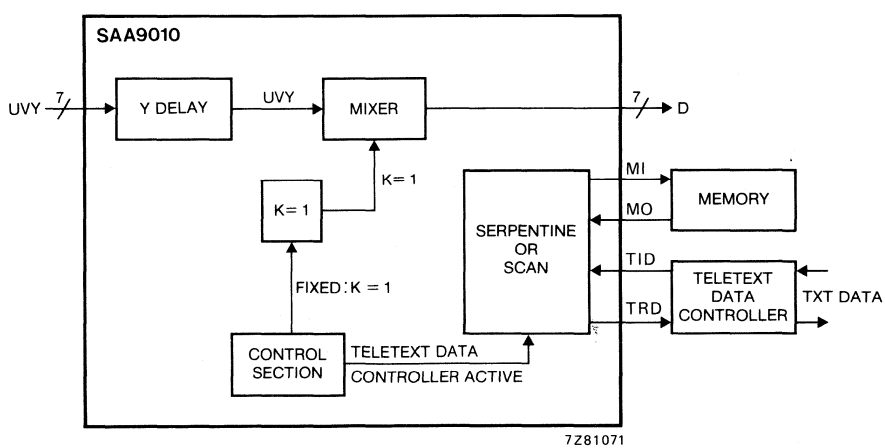


Fig. 8 Main signal flow during teletext mode.

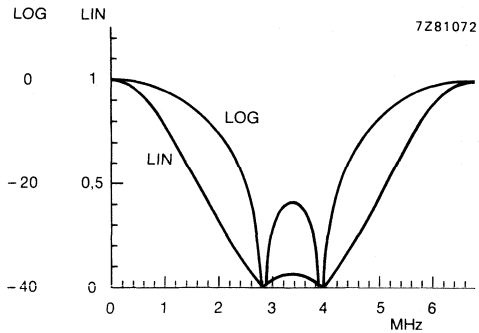
FIBI format and content

The format identification, blanking and instruction (FIBI) signal, obtained from the field memory controller (SAA9020), is used to indicate the positions of samples in the video data stream (Fig. 10a). It is also used as a means of controlling the functions of the PEP (Fig. 10b). Data is transmitted in the HIGH time of FIBI and each data bit is followed by its inverse. If the check on the data and $\overline{\text{data}}$ fails for any bit in a message the whole message is rejected. Each message must have the correct address (FA = 0) and length to be accepted. Only one message may be sent in each FIBI HIGH time. Data contained in the message is acted on at the next rising edge of FIBI after the minimum LOW time.

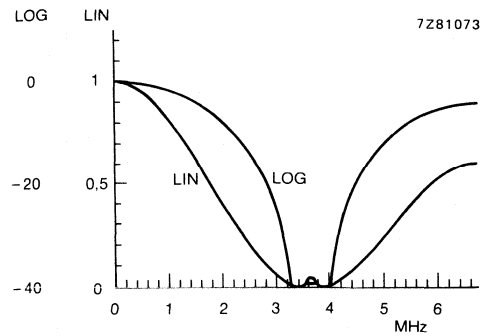
FIBI format and content (continued)

FIBI data	description
start bit	"0" sent at the beginning of each message
FA	address bit, PEP address is "0"
MBL	memory blank bit. MBL = "1" sets MI0 to MI6 to zero
F1, F0	luminance-difference filter control bits. Used to adjust the filter characteristics as follows (Fig. 9a): F1 F0 0 0 low bandwidth, low gain (filter 0) 0 1 suppression between 3 and 4 MHz (filter 1) 1 0 moderate filtering (filter 2) 1 1 good high-frequency suppression (filter 3)
M3	text bit. M3 = "1" allows text routing to be enabled
M2, M1, M0	status bits. Determine the mixer K factor as follows (Fig. 9b): M2 M1 M0 0 0 X K = 1. Direct video from UVY is passed to both MI and D outputs 0 1 X K = 0. Data from MO is passed to MI and D outputs 1 0 0 K = ½ and 1. Luminance data "Y" is passed directly from UVY to both MI and D outputs Chrominance data "U/V" is passed directly to MI but is processed with K = ½ before passing to D 1 0 1 K = ½ and 1. Luminance data "Y" is passed directly from UVY to both MI and D outputs Chrominance data "U/V" is processed with K = ½ before passing to outputs MI and D 1 1 0 low noise reduction. K is dependent on the difference between MO and UVY 1 1 1 high noise reduction. K is dependent on the difference between MO and UVY but with a different range
Y4 to Y0	delay to be given to Y-samples. The Y-delay has a range of 0 to 31 Y-sample positions relative to a U and V sample. Y4 is msb
TST	test mode bit. "0" for normal operation

X = don't care.

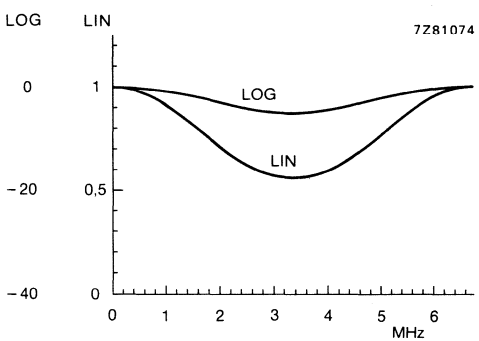


Filter 0: F1 = "0"; F0 = "0"
(low bandwidth, low gain).

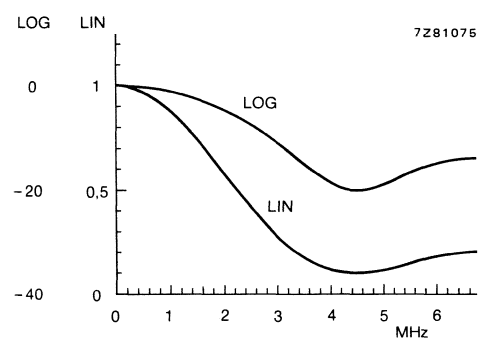


Filter 1: F1 = "0"; F0 = "1"
(3 to 4 MHz suppression).

DEVELOPMENT DATA

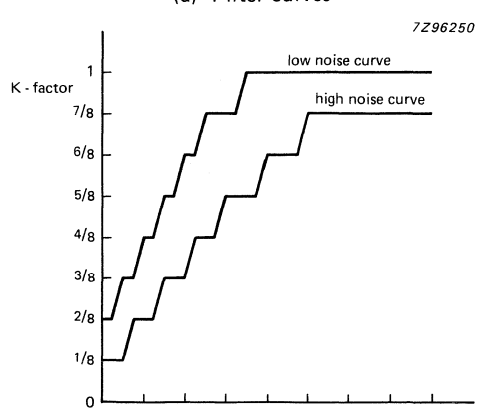


Filter 2: F1 = "1"; F0 = "0"
(moderate filtering).



Filter 3: F1 = "1"; F0 = "1"
(good high-frequency suppression).

(a) Filter curves



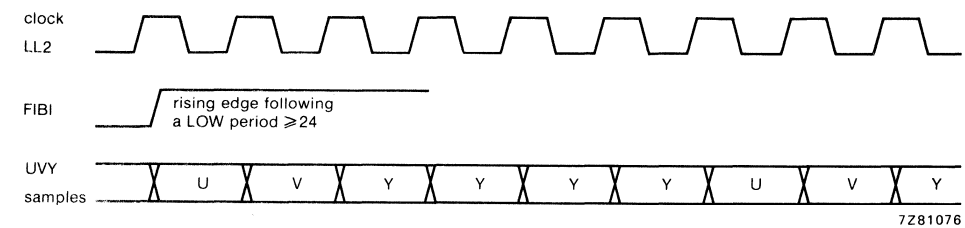
(b) K-factor curves

Fig. 9 Graphs showing filter and K-factor curves.

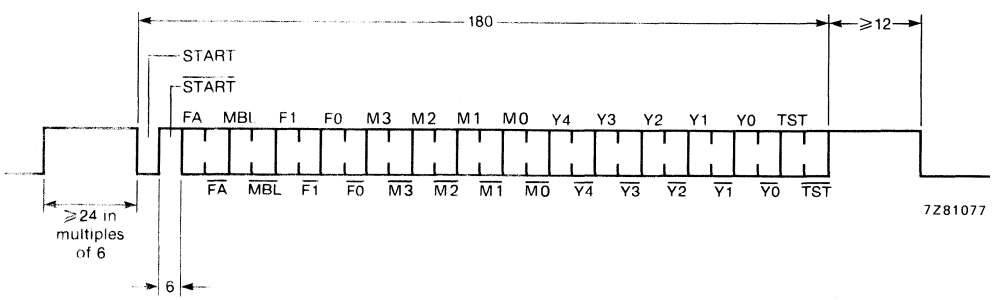
FIBI timing (Figs 10 and 11)

Data may be inserted during the HIGH period of FIBI after a minimum FIBI = HIGH time of 6n LL2 cycles ($n \geqslant 4$). To accommodate the data, the duration of the FIBI = HIGH period can be extended in multiples of 6 LL2 cycles. Each data bit (or its complement) is sent for a period of 6 LL2 cycles. After completion of a data message a FIBI = HIGH time of at least 12 LL2 cycles is required for the data to be accepted. The next rising edge of FIBI to load this data will be recognized only after a minimum FIBI = LOW time of 24 LL2 cycles.

After the FIBI = LOW time, the LL2 cycle corresponding to the FIBI rising edge is a U-sample position at the UVY inputs (Fig. 10a). The first valid sample cannot be less than 8 LL2 cycles after a rising edge of FIBI if the previous rising edge of FIBI was not a multiple of 6 LL2 cycles earlier.



(a) positioning of UVY samples relative to the rising edge of FIBI



(b) FIBI data format

Fig. 10 FIBI timing and data format (all numbers indicate LL2 clock cycles).

DEVELOPMENT DATA

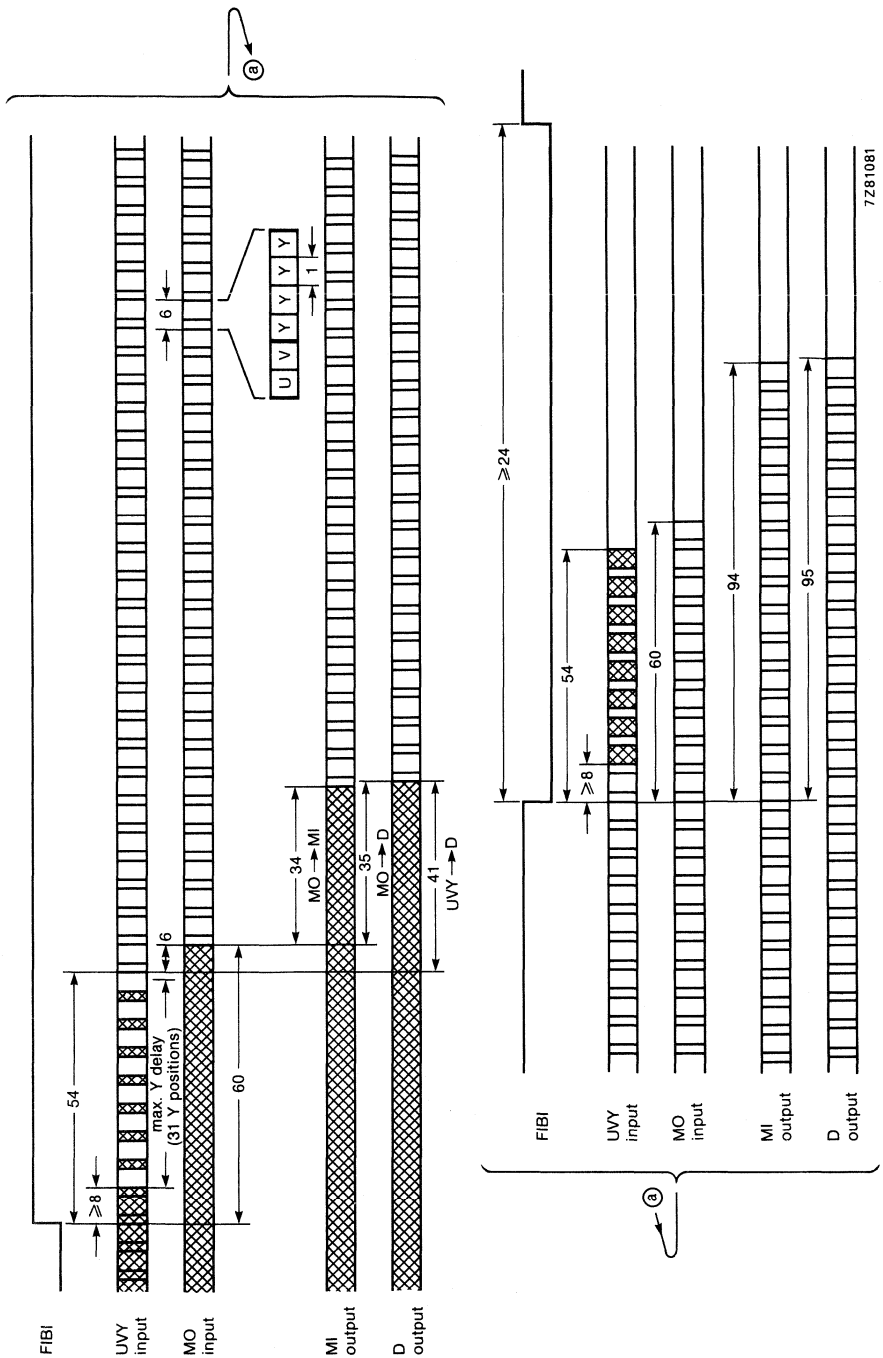
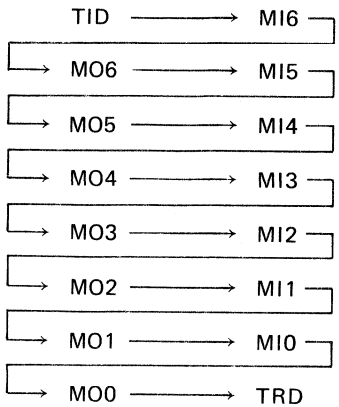


Fig. 11 Input and output timing relationships to FIBI rise and fall times (all numbers indicate LL2 clock cycles).

Non-video (text) routing

When the status bit M3 is set to "1" it is assumed that the memories are to be used only for text storage and the internal routing of the PEP is reconfigured accordingly. During each MRN = HIGH interval a serpentine mode is established to give the following signal path:



The set-up timing (5 LL2 cycles) for teletext mode is shown in Fig. 12. The delay time for teletext data to pass through the PEP in the serpentine and/or scanning modes is 2 LL2 cycles.

In the scanning mode the PEP scans the inputs from the memories MO0 to MO6 and is controlled by the inputs MRN and SCN (Fig. 13). The input selected to send data to the output TSD is reset to MO0 on a rising edge of MRN when SCN = LOW, and steps in the sequence MO0, MO1, MO2, etc. on rising edges of MRN when SCN = HIGH. The signal TCN = LOW indicates that the scanning is on MO6.

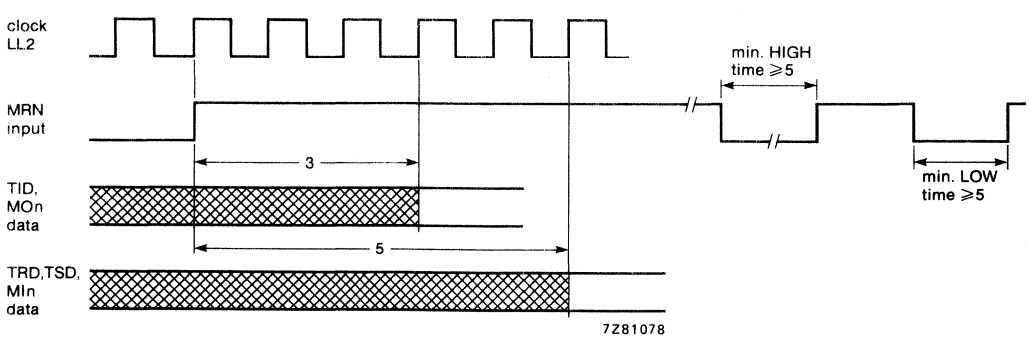


Fig. 12 Set-up timing for teletext mode (all numbers indicate LL2 cycles).

DEVELOPMENT DATA

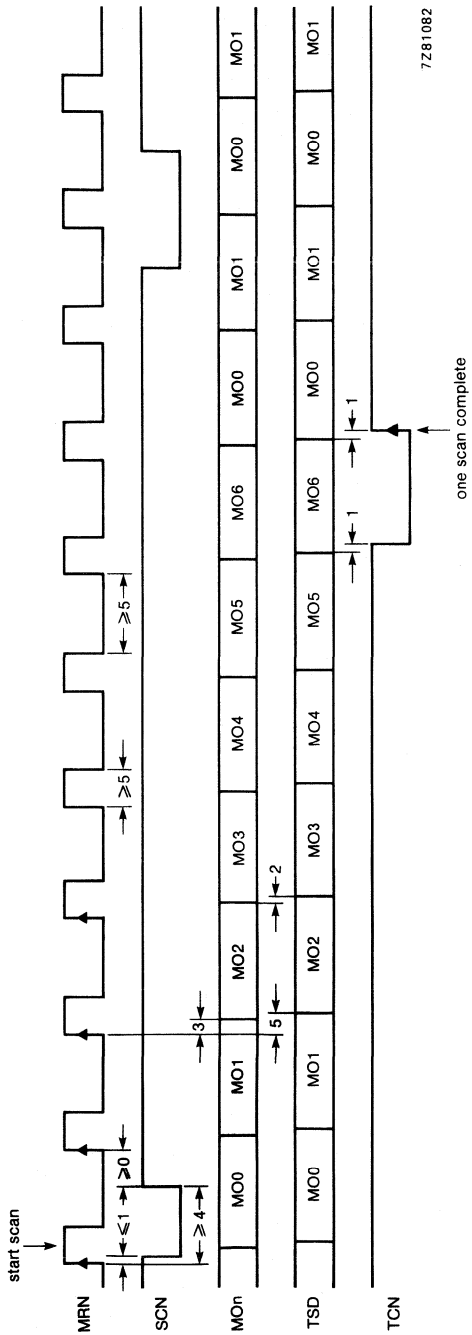


Fig. 13 Scanning mode timing (all numbers indicate LL2 cycles).

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to 6,5 V
D.C. input diode current		
at $V_I < V_{SS}$	$-I_{IK}$	20 mA
at $V_I > V_{DD}$	I_{IK}	20 mA
D.C. input voltage range	V_I	−0,5 to V_{DD}+ 0,5 V
D.C. output diode current		
at $V_O < V_{SS}$	$-I_{OK}$	20 mA
at $V_O > V_{DD}$	I_{OK}	20 mA
D.C. output voltage range	V_O	−0,5 to V_{DD}+ 0,5 V
D.C. output source or sink current per output pin	I_O, $-I_O$	25 mA
D.C. current V_{DD} or V_{SS}	I_{DD}, I_{SS}	200 mA
Storage temperature range	T_{stg}	−65 to 150 °C

RECOMMENDED OPERATING CONDITIONS

Supply voltage range	V_{DD}	4,75 to 5,25 V
Input voltage range	V_I	−0,5 to V_{DD}+ 0,5 V
Output voltage range	V_O	−0,5 to V_{DD}+ 0,5 V
Operating ambient temperature range	T_{amb}	0 to + 70 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{DD} = 4,75 to 5,25 V; V_{SS} = 0 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range (pin 33) with respect to V_{SS}	V_{DD}	4,75	5,0	5,25	V
Supply current range (pin 33)	I_{DD}	*	40	*	mA
Inputs					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}+ 0,5	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input capacitance (except LL2)	C_I	–	–	5	pF
Input capacitance (LL2)	C_I	–	–	20	pF

* Values under investigation.

parameter	symbol	min.	typ.	max.	unit
Outputs					
Output voltage HIGH at $-I_O$ = 2,0 mA	V_{OH}	2,2	–	V_{DD}+ 0,5	V
Output voltage LOW at I_O = 2,0 mA	V_{OL}	0	–	0,6	V
Timing (Fig. 14)					
LL2 cycle time	t_C	47	–	52	ns
LL2 HIGH time	t_{CH}	20	–	–	ns
LL2 LOW time	t_{CL}	20	–	–	ns
LL2 rise/fall time	t_r, t_f	–	–	3	ns
Input set-up time	t_{SU}	12	–	–	ns
Input hold time	t_{IH}	3,0	–	–	ns
Output hold time	t_{OH}	3,0	–	–	ns
Output delay time	t_{OD}	–	–	33	ns
Load capacitance	C_L	15	–	25	pF

DEVELOPMENT DATA

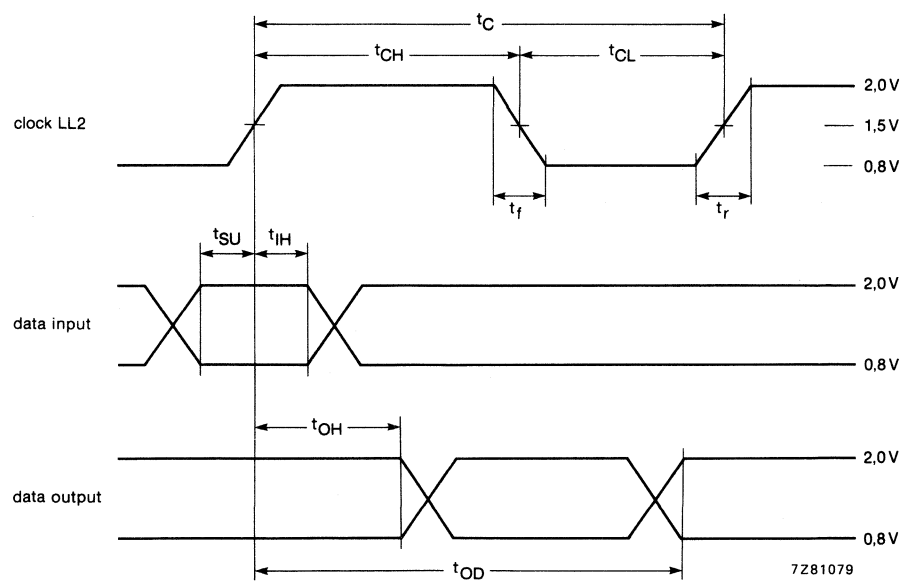


Fig. 14 Timing waveforms.

FIELD MEMORY CONTROLLER

The SAA9020 field memory controller (FMC), a 24-pin CMOS integrated circuit, is for application in memory-based feature tv receivers. It is part of the field memory system for providing picture quality enhancement. The SAA9020 provides the system I^2C bus interface and is used to control the picture enhancement processor (SAA9010) and the system field memory.

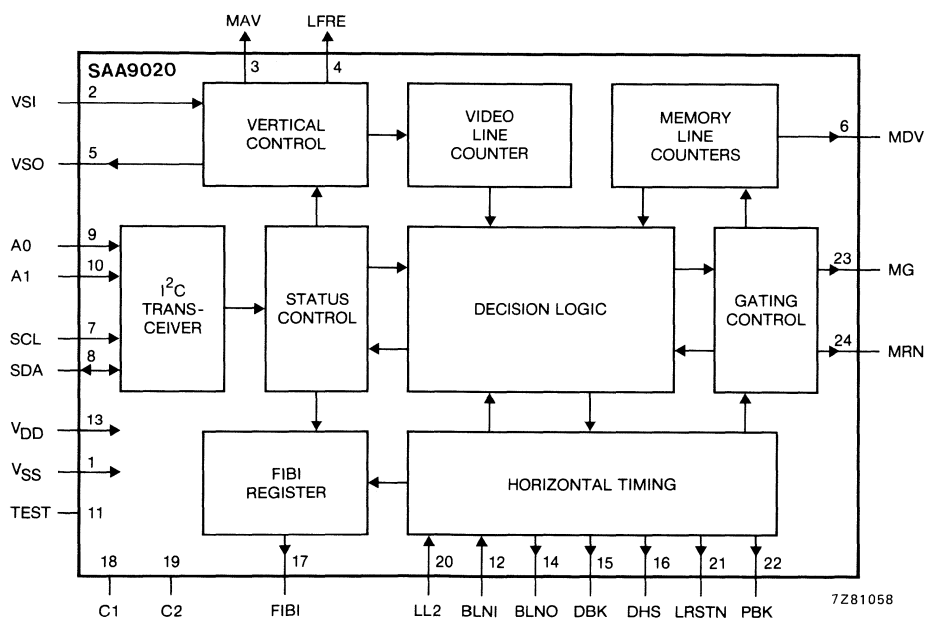


Fig. 1 Block diagram.

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

PINNING

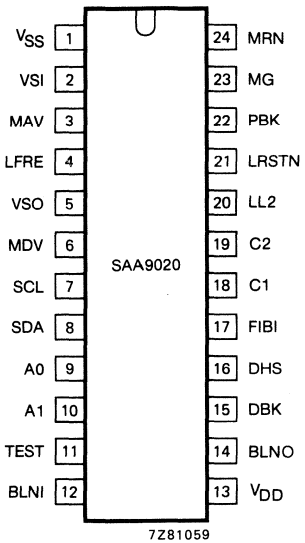


Fig. 2 Pinning diagram.

1	V_{SS}	negative supply voltage (0 V)
2	VSI	vertical synchronization input pulse
3	MAV	memory above video output signal that indicates the memory contents being processed were spatially above the incoming video
4	LFRE	line flicker reduction enable. This output signal indicates that a standard field length has been received
5	VSO	vertical synchronizing output. This is a delayed vertical synchronizing pulse that is HIGH for 14 to 15 line-periods and is derived from VSI or internal memory counters, depending on the mode of operation
6	MDV	memory data valid output. This is HIGH during the period when the outputs from the memories are known to be valid, i.e. during store/recall and still picture
7	SCL	serial clock input for the I^2C bus transceiver
8	SDA	serial data input/output and acknowledge output for I^2C bus transceiver
9, 10	A0, A1	address inputs for the I^2C bus transceiver. Normally hard-wired to a fixed address
11	TEST	connected to V_{SS} for normal operation
12	BLNI	blanking input. A rising edge of this input resets the horizontal timing of the FMC
13	V_{DD}	positive supply voltage (+ 5 V). Requires external decoupling to V_{SS}
14	BLNO	blanking output. This signal is LOW during vertical and horizontal flyback periods and when undefined data is expected from the picture enhancement processor (SAA9010

15	DBK	delayed burst key output. To correct signal processing delays the position of DBK can be adjusted by the programmable output delay with respect to BLNO
16	DHS	delayed horizontal synchronization pulse output. To correct signal processing delays the position of DHS can be adjusted by the programmable output delay with respect to BLNO
17	FIBI	format identification, blanking and instruction output. Indicates the format (order) of the video samples and carries instructions to control the picture enhancement processor (SAA9010)
18, 19	C1, C2	pins for connecting an external decoupling capacitor (low-inductance type), C1 = V_{DD} and C2 = V_{SS}
20	LL2	20,25 MHz line-locked clock input
21	LRSTN	line reset output pulse
22	PBK	phase-reference burst key output. The duty factor of this output is typically 50% and the timing of the rising edge can be adjusted by the programmable input delay
23	MG	memory gating output to the field memories to control data input, output and line shifting. This output is set to float when the background memory function is requested and by power-on-reset
24	MRN	memory refresh control output to the field memories. This output is set to float when a background memory function is requested and by power-on-reset

FUNCTIONAL DESCRIPTION

Operation

The main task of the FMC is to control the synchronism between incoming video, memory data and the display. During store/recall picture and still picture, where a field of video has been stored in the memories, the memories are not synchronized to the incoming video; when the memory contents are displayed the display synchronism is controlled by the memory counters and not by the incoming video.

The FMC communicates with the PEP via the FIBI signal and controls the memories via the MG and MRN signals. Communication with the FMC is made via the I^2C transceiver which is also used to set up certain FIBI data.

Other functions of the field memory controller are:

- to execute commands for changes of system operating modes by controlling the internal status of the PEP and the drive signals of the field memories;
- to divide the clock frequency (LL2) to the applicable line frequency;
- to pass the vertical sync pulse to the deflection circuits or, if necessary, to generate its own vertical sync pulse (e.g. for stored picture display);
- to delay the horizontal drive and the clamp pulse for the RGB processing and compensate for delays to the video signal in the PEP;
- to provide the means of making the system independent of tv standards (an important aspect of this function is its control of the virtual memory length).

There are six modes of operation, one of which releases control of the memories for other uses such as background text storage. The remaining five modes are direct video, store/recall picture, still picture, cross-colour reduction and noise reduction.

FUNCTIONAL DESCRIPTION (continued)

Operation (continued)

In the direct video mode no processing of memory data is performed and the PEP is instructed to pass unprocessed video data direct. The memories are controlled in such a way that they are reloaded with each new field of video.

Store/recall and still picture modes hold a field of video in the memories. If noise or cross-colour reduction was previously active then a processed picture will be stored. Once a picture has been fully stored the PEP is instructed to pass direct unprocessed video. The stored picture will be brought into view on the command 'recall picture', this is a toggle function and may be used to 'restore' this picture and display direct video or to display the stored picture. Freeze picture is the combined operation of store and recall.

The cross-colour reduction mode causes the PEP and memories to be controlled as a transversal filter for the U and V samples of the video. The mode can be for PAL or NTSC in that the memory data is either compared with the video line spatially above or spatially below. It is only active for standard length fields.

In the noise reduction mode recursive filtering is established for all video samples. The option for high-level or low-level noise reduction has no influence on the functioning of the FMC. Noise reduction is only active for the number of active video lines stored in memory, otherwise direct video is passed through.

In the cross-colour and noise reduction modes the memories have to be synchronized with the incoming video to ensure the correct processing and display of the data.

The FMC ensures that during any change of operating mode the correct synchronism is obtained before instructing the PEP to change mode. The mode change will be forced in extreme cases where synchronism cannot be obtained within 32 fields.

I^2C write mode

The I^2C message to the FMC comprises three or more bytes. The first contains the FMC address (0 0 1 0 1 A1 A0, where A1 and A0 are hard-wired externally). This byte is always acknowledged when the correct address is received. The second byte addresses one of three data registers, receipt of the correct address is acknowledged unless the FMC is busy with a status change. The third and subsequent bytes are data bytes which, if received, will only be acknowledged and loaded if the FMC is not busy with a requested status change initiated via bits S3 to S0.

The first data byte is loaded into the addressed register. The address is incremented for each data byte received until the third register is loaded, then the address remains at the third register until a new address is specified at the start of a new transmission.

FMC register address	contents msb							lsb	status after power-on-reset
0 0 0 0 0 0 0 0	TVL	VW	B2	B1	B0	H2	H1	H0	0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 1	Y4	Y3	Y2	Y1	Y0	TST	INT	FTST	0 0 0 0 1 0 0 0
0 0 0 0 0 0 1 0	FA	MBL	F1	F0	S3	S2	S1	S0	0 0 0 0 1 0 0 0

New data for TVL and VW will only be acted upon on the rising edge of VSO. The bits Y4 to Y0, TST, FA, MBL, F1 and F0 are copied into the FIBI message. The FMC responds to the other bits as follows:

bit	FMC response
TVL	set to "1" for 625-lines per frame set to "0" for 525-lines per frame
VW	vertical sync acceptance window limits are set as follows: VW = "0", TVL = "0" window is from video line 25 to 289; VW = "0", TVL = "1" window is from video line 25 to 342; VW = "1", TVL = "0" window is from video line 240 to 289; VW = "1", TVL = "1" window is from video line 281 to 342.
B2 to B0	set the programmable input delay (PID). B2 is the msb. The delay can be incremented to make the rising edge of PBK earlier in 7 steps of 6 LL2 cycles.
H2 to H0	set the programmable output delay (POD). H2 is the msb. The delay can be incremented to make the falling edge of DHS later in 7 steps of 6 LL2 cycles. DHS and DBK remain in a fixed relationship to each other (all edges move with the POD).
INT	selects mode of display of memory picture: INT = "1" = interlaced; INT = "0" = non-interlaced.
S3 to S0	status control bits. Used as follows: S3 S2 S1 S0 0 0 0 0 direct video – no memory processing 0 0 0 1 store picture in memory and display direct video 0 0 1 0 recall picture from store and view, or re-store the displayed memory picture 0 0 1 1 freeze picture by storing and displaying 0 1 0 0 cross-colour reduction (PAL mode) 0 1 0 1 cross-colour reduction (NTSC mode) 0 1 1 0 noise reduction (low level) 0 1 1 1 noise reduction (high level) 1 0 0 0 background memory active No other codes are permitted.
FTST	test bit, normally set to "0". When set to "1" causes the FIBI output to float.

FUNCTIONAL DESCRIPTION (continued)

I²C read mode

If the correct FMC address is received and the R/$\overline{W}$ bit is set to "1" then the following status byte is returned:

msb							lsb
PUD	BUSY	CM3	CM2	CM1	CM0	M25L	V25L

The bits of the status byte have the following meanings:

bit	meaning
PUD	power-up detection. This bit is set to "1" when a power-up has been detected since this register was last read. The bit is reset to "0" when the register is read
BUSY	"1" indicates that the FMC is busy with a change of status
CM3 to CM0	presents the contents of the current-mode latch and are normally the same as bits S3 to S0, exceptions are after power-on and in background memory mode when the contents are equal to 1 0 0 1
M25L	goes to "1" when the memory line counter is in 'position 0' through to 'position 24'
V25L	goes to "1" when the video line counter is in 'position 0' through to 'position 24'

FIBI (Fig. 3)

The FIBI signal indicates the positions of samples in the video data streams and carries commands to the PEP. Data is transmitted in the normally-HIGH time of FIBI whenever the video counter is reset or, in certain modes, when the last valid memory line is reached. Each transmission is repeated for two lines and each data bit of the message is followed by its inverse. Data sent is acted upon at the next rising edge of FIBI.

FIBI data	description
start bit	"0" sent at the beginning of each message
FA	copied from I²C bit FA
MBL	copied from I²C bit MBL
F1, F0	copied from I²C bits F1, F0
M3 to M0	mode control bits. Normally a copy of the I²C bits S3 to S0. Modified so that direct video is passed through during mode changes and in those cases where the requested mode is not possible
Y4 to Y0	copied from I²C bits Y4 to Y0
TST	copied from I²C bit TST, set internally to "0" at power-on

Data is inserted into the HIGH-period of FIBI 24 LL2 cycles after the rising edge. Each data bit (or its complement) is sent for a period of 6 LL2 cycles. For the description of the timing relative to other outputs see 'signal timing'.

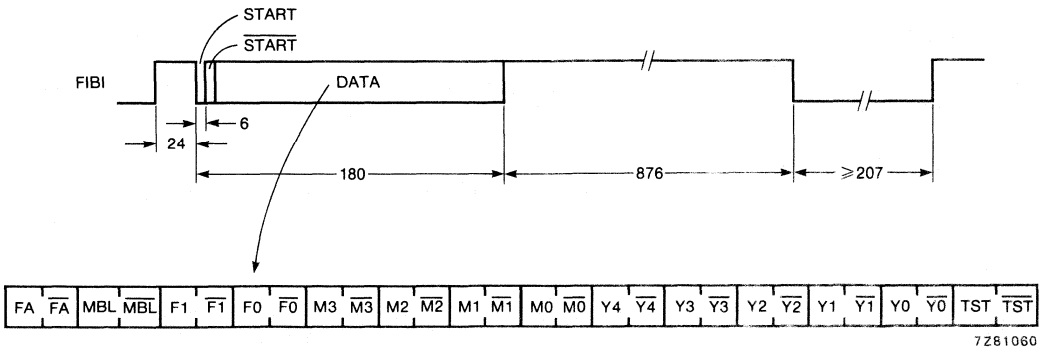


Fig. 3 FIBI timing and order of data (all numbers indicate LL2 cycles).

Signal timing

VSI

This is accepted only during the specified vertical acceptance window if it has an integrated HIGH time $\geqslant 16\ \mu s$ (342 LL2 cycles). When accepted, the VSI pulse resets the video line counter to video line 1. After acceptance at least 324 LL2 clock cycles must elapse before another VSI pulse can be accepted. If a VSI pulse is not accepted an internal vertical synchronizing pulse will be generated at the end of the vertical window.

VSO

In modes where VSO is derived from the incoming video (VSI) the rising edge of VSO follows 344 LL2 cycles after the rising edge of VSI. When VSO is derived from the internal memory counters the timing of VSO depends on the line system in use and the internal bit INT.

line system	line number in which VSO rising edge occurs	number of LL2 cycles from rising edge of FIBI to start of VSO rise
625 non-interlace	313	292
	312	292
625 interlace	312	940
	313	292
525 non-interlace	263	292
	262	292
525 interlace	262	940
	263	292

In all cases VSO will remain HIGH until at least 172 (163) LL2 cycles after the 14th FIBI (non-data) falling edge to occur in the current VSO = HIGH time as shown in Fig. 7.

MRN, MDV

These signals switch during the LOW time of MG, remain valid for at least 4 LL2 cycles after the MG falling edge and are valid at least one LL2 cycle before MG rising edge.

Signal timing (continued)

LFRE, MAV

When these signals are active they will start to change no sooner than 172 (163) LL2 cycles after the first FIBI falling edge in the VSO = HIGH time (see Fig. 7).

BLNO, DBK, DHS, FIBI, LRSTN, PBK

The relationships between these signals are shown in Fig. 4 in which all horizontal timings are shown in relation to one line of active video.

MG

This signal has four modes of operation; normal, refresh, slow and fast gating. The timing in normal and refresh modes is shown in Fig. 4. In the slow gating mode, MG may remain LOW for as many as 16 line periods and then be active for at least 3 line periods. In the fast gating mode the edges of this signal are not synchronized with the other line-rate signals, MG then has a nominal LOW time of 40 LL2 cycles and a nominal HIGH time of 362 LL2 cycles (either time may be extended once by 3 LL2 cycles during the FIBI LOW time in 525-line mode).

BLNI

A rising edge of this signal resets the horizontal timing of the FMC, which results in a falling edge of FIBI 1026 LL2 cycles later. When BLNI is held LOW or HIGH the horizontal timing will run free with a period of 1296 LL2 cycles (625-line working), or 1287 LL2 cycles (525-line working).

Note

In analogue environments the horizontal synchronization is achieved by phase comparison between the phase-reference and analogue burst keys (PBK and ABK, see Fig. 4)and the result is used to control the frequency of a VCO.

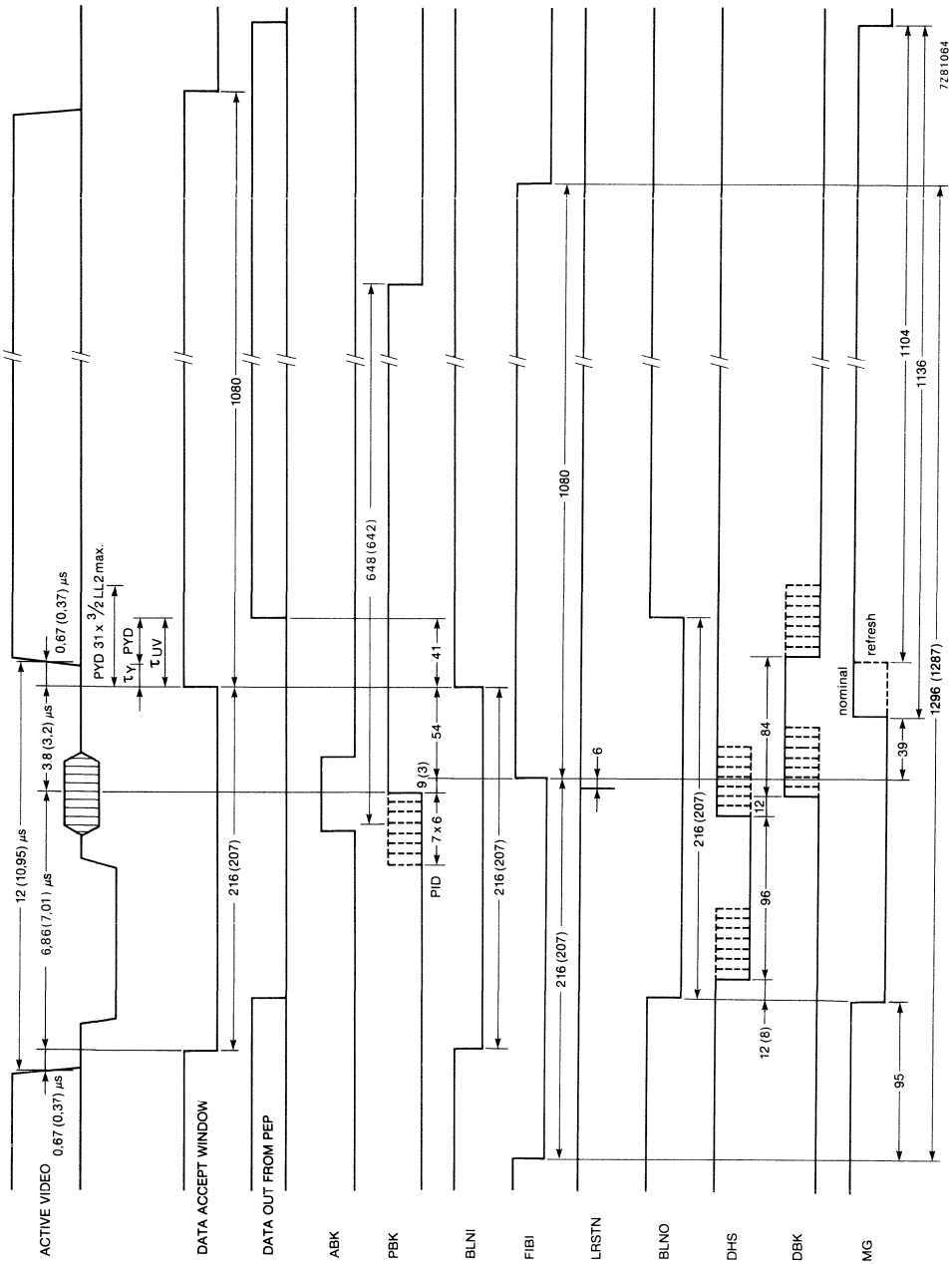


Fig. 4 Horizontal timing signals (all numbers indicate LL2 clock cycles unless otherwise specified, numbers in parentheses are for 525-line systems).

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to 6,5	V
D.C. input diode current			
at $V_I < V_{SS}$	$-I_{IK}$	20	mA
at $V_I > V_{DD}$	I_{IK}	20	mA
D.C. input voltage range	V_I	−0,5 to V_{DD}+ 0,5	V
D.C. output diode current			
at $V_O < V_{SS}$	$-I_{OK}$	20	mA
at $V_O > V_{DD}$	I_{OK}	20	mA
D.C. output voltage range	V_O	−0,5 to V_{DD}+ 0,5	V
D.C. output source or sink current per output pin	I_O, $-I_O$	25	mA
D.C. current V_{DD} or V_{SS}	I_{DD}, I_{SS}	50	mA
Storage temperature range	T_{stg}	−65 to 150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RECOMMENDED OPERATING CONDITIONS

Supply voltage range	V_{DD}	4,5 to 5,5	V
Input voltage range	V_I	−0,5 to V_{DD}+ 0,5	V
Output voltage range	V_O	−0,5 to V_{DD}+ 0,5	V
Operating ambient temperature range	T_{amb}	0 to + 70	°C

CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; V_{SS} = 0 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	*	7,0	*	mA
Inputs (except SDA, SCL)					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}+ 0,5	V
Input voltage LOW	V_{IL}	0,0	–	0,8	V
Input capacitance:					
LL2 (pin 20)	C_I	–	–	15	pF
all other inputs	C_I	–	–	5	pF
Inputs SDA, SCL					
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}+ 0,5	V
Input voltage LOW	V_{IL}	0,0	–	1,5	V
Input capacitance	C_I	–	–	5	pF
Outputs (except SDA)					
Output voltage HIGH at $-I_O$ = 2,0 mA	V_{OH}	2,2	–	V_{DD}+ 0,5	V
Output voltage LOW at I_O = 2,0 mA	V_{OL}	0,0	–	0,6	V
Output SDA					
Output voltage LOW at I_O = 3,0 mA	V_{OL}	0,0	–	0,4	V
Clock LL2 timing (Fig. 5)					
Cycle time	t_C	47	–	52	ns
HIGH time	t_{CH}	20	–	–	ns
LOW time	t_{CL}	20	–	–	ns
Rise/fall time	t_r, t_f	–	–	3,0	ns
Input BLNI timing (Fig. 5)					
Input set-up time	t_{SU}	12	–	–	ns
Input hold time	t_{HD}	3,0	–	–	ns

* Values under investigation.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Outputs BLNO, DBK, DHS, FIBI, LRSTN, MG, PBK timing (Fig. 5)					
Output hold time	t_{OH}	3,0	–	–	ns
Output delay time	t_{OD}	–	–	33	ns
Load capacitance	C_L	15	–	25	pF
Output MRN timing (Fig. 6)					
Output hold time	t_{OH}	0,0	–	–	ns
Output delay time	t_{OD}	–	–	600	ns
Load capacitance	C_L	10	–	100	pF
Outputs VSO, LFRE, MAV, MDV (Figs 6 and 7)					
Output hold time	t_{OH}	0,0	–	–	ns
Output delay time	t_{OD}	–	–	300	ns
Load capacitance	C_L	15	–	50	pF
I^2C bus timing (Fig. 8)					
SCL frequency	f_{SCL}	0	–	100	kHz
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise times	t_R	–	–	1	μs
SCL and SDA fall times	t_F	–	–	300	ns
Time the bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Start condition hold time (after this period the first clock pulse may be generated)	$t_{HD;STA}$	4,0	–	–	μs
Start condition set-up time (repeated start condition only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0,0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

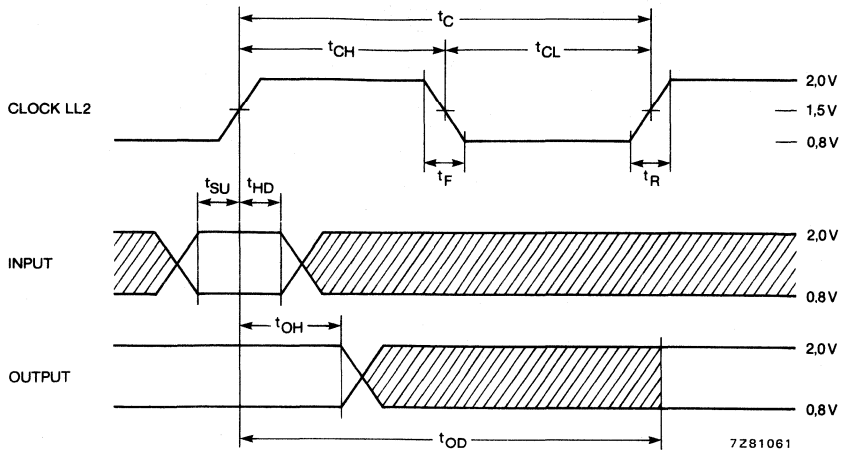


Fig. 5 Clock LL2 timing.

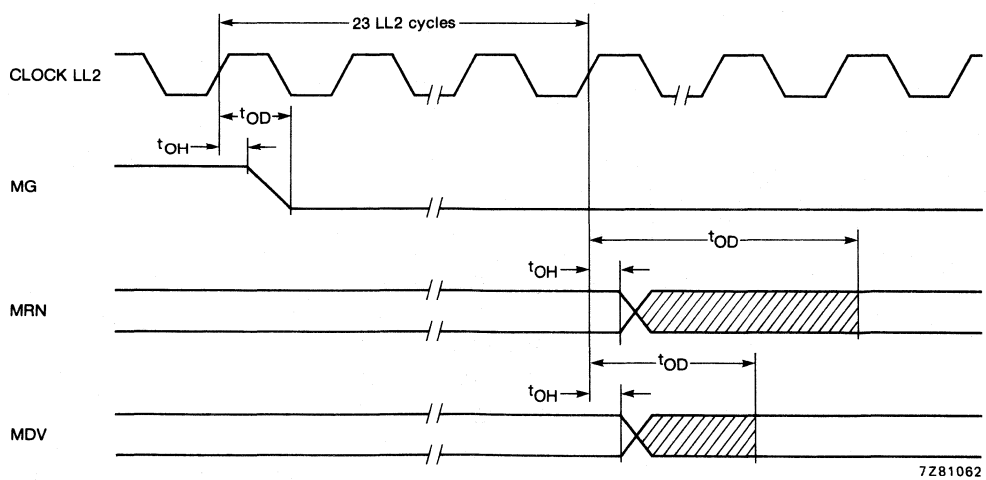


Fig. 6 MG, MRN, and MDV timing.

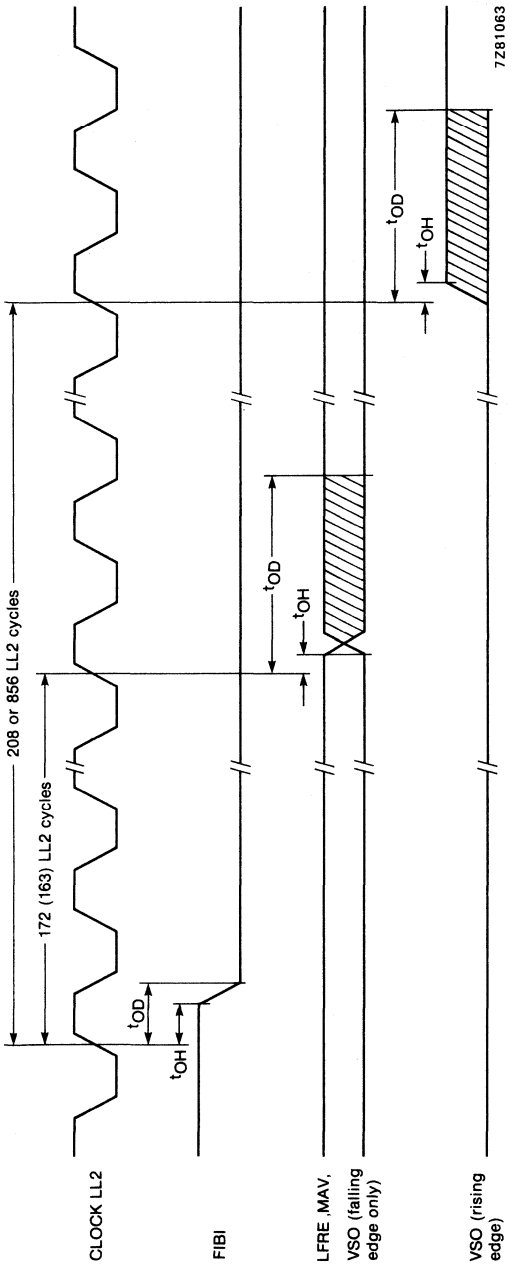


Fig. 7 FIBI, LFRE, MAV, VSO timing (numbers in parentheses are for 525-line working).

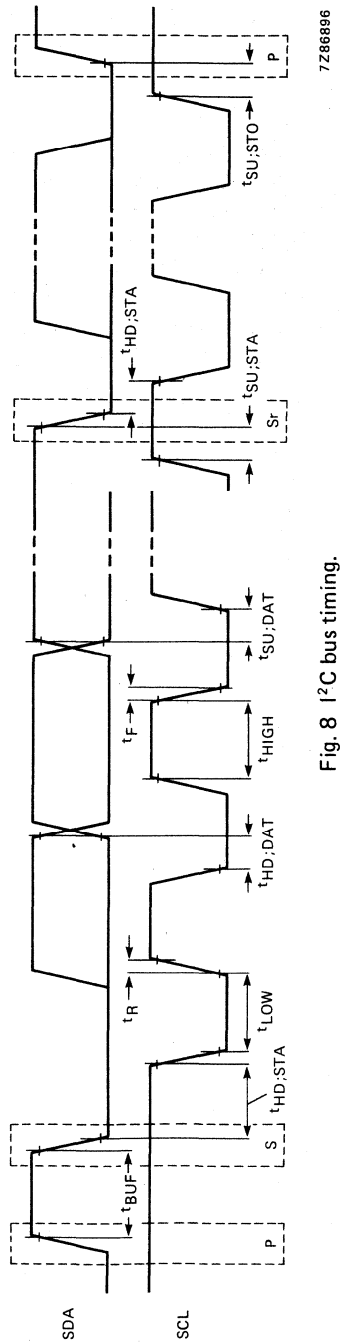


Fig. 8 I²C bus timing.

BACKGROUND MEMORY CONTROLLER

GENERAL DESCRIPTION

The SAA9030 background memory controller (BMC) is for application in memory-based feature tv receivers. It directs teletext data from the teletext video processor to a FIFO-organized CCD memory, refreshes the CCD memory arrays and, when in teletext mode, supplies the teletext data to a computer-controlled teletext decoder after a page request.

The background memory controller, together with the computer-controlled teletext extension (CCTE, SAA9040) can be used in a 'stand-alone' system or with a picture enhancement processor (PEP, SAA9010) in feature television applications. Inputs and outputs excepting F_6, TTDI and TTCI are TTL-compatible.

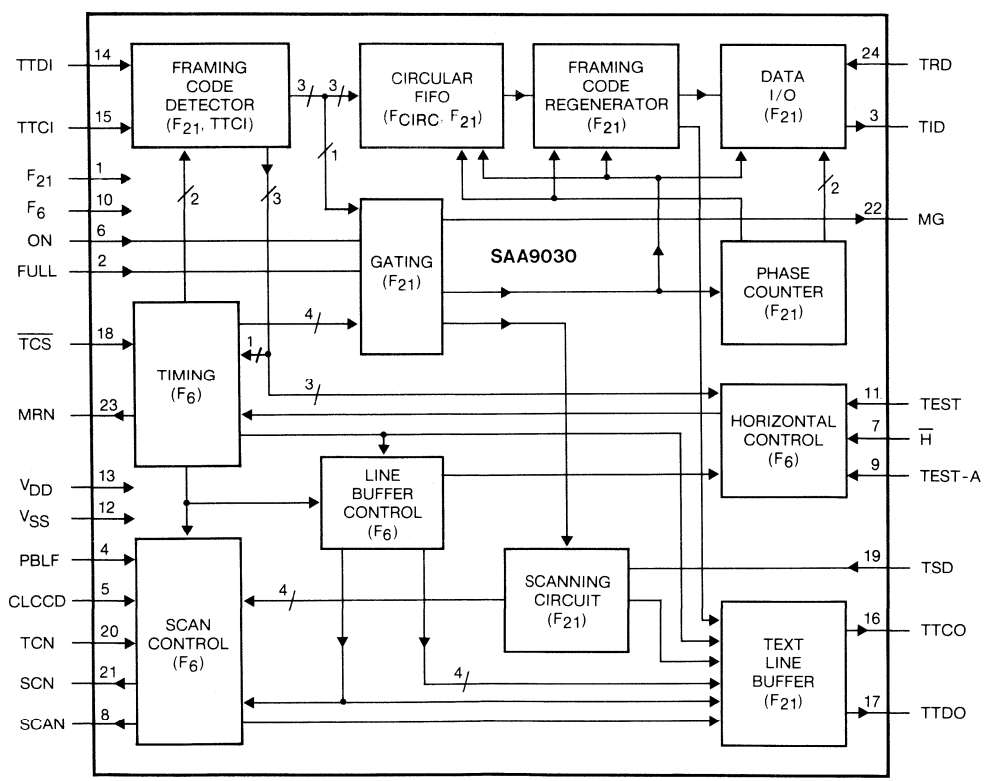


Fig. 1 Block diagram.

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101B).

PINNING

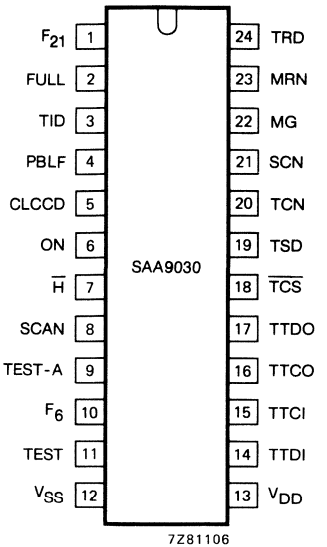


Fig. 2 Pinning diagram.

1	F_{21}	master clock input. 20,25 MHz line-locked in feature tv applications; 20,8 MHz (approx.) free-running in stand-alone applications
2	FULL	full channel mode select input. When HIGH, the BMC is in full channel mode
3	TID	teletext data to CCD memory. Bit rate of serial data stream is defined by F_{21}
4	PBLF	page-being-looked-for, command input
5	CLCCD	clear CCD, command input
6	ON	activate-BMC, command input. When LOW, MRN and MG are floating, and TTDI is resynchronized to $\overline{TCS}$ and routed to TTDO
7	$\overline{H}$	horizontal timing input at tv line frequency (from CCTE)
8	SCAN	output to indicate that memory scanning is in progress
9	TEST-A	test input. LOW for normal operation
10	F_6	6 MHz clock input. Internal a.c. coupling
11	TEST	test input. LOW for normal operation
12	V_{SS}	negative supply voltage (ground)
13	V_{DD}	positive supply voltage
14	TTDI	teletext data input. Serial bit stream from video input processor during active teletext lines in data entry window. Bit rate is defined by TTCI. External a.c. coupling, internal clamping
15	TTCI	teletext clock input. 6,9375 MHz. Internal a.c. coupling
16	TTCO	teletext clock output. Frequency = $^1/_3 F_{21}$; typical duty factor = 50%
17	TTDO	teletext data output. Serial bit stream active during CCD scanning and DEW (data entry window). Bit rate is defined by TTCO
18	$\overline{TCS}$	teletext composite sync. Defines BMC timing

19	TSD	teletext scanned memory data. Serial bit stream from one of the CCDs via the picture enhancement processor or multiplexer. Bit rate defined by F_{21}
20	TCN	terminal count input. Command from picture enhancement processor or external counter to start the second or third scan of the CCDs, or that a third scan is complete. Active LOW
21	SCN	start count output. Active LOW
22	MG	memory gating. Three-state output controlled by "ON" input. Active, if enabled, during reception of teletext data packets, and during memory recirculation
23	MRN	memory recirculate. Three-state output enabled by "ON" input. When enabled gives a HIGH during tv lines 7 to 22 and 320 to 335. Also used as scan clock for picture enhancement processor or external counter
24	TRD	teletext recirculated data. Serial bit stream from last CCD. Bit rate defined by F_{21}

FUNCTIONAL DESCRIPTION

Generation of MG and MRN signals

The background memory controller generates the memory gating (MG) and memory recirculate (MRN) signals required by the CCD memory arrays. These signals are available only when the "ON" input from the CCTE is HIGH (when "ON" is LOW, MG and MRN are in the high-impedance OFF-state).

Data storage during the vertical blanking interval

Teletext data packets (one data packet per tv line) are supplied from the video input processor at a bit rate of 6,9375 Mbits/s to pin TTDI. The incoming data is temporarily stored in a circular FIFO register from the start of the incoming line until the first bit can be stored in the CCD memory.

A valid data line carries a framing code that is recognized by the BMC. Detection of the framing code is performed during the Data Entry Window (DEW) which is a gate derived from the negative edge of the Text Composite Sync ($\overline{TCS}$) signal and is active during lines 7 to 22 and 320 to 335 of a tv picture. The time slot for detection (frame code window) is active from 12 to 15 μs in a tv line and this timing is derived from the horizontal timing pulse ($\overline{H}$). The framing code is regenerated within the BMC.

When valid teletext data is recognized, it is synchronized to one-third of the master clock frequency (F_{21}). As a line of teletext data is being shifted out via pin TID to the CCD memory input, it is interleaved with teletext recirculated data received at pin TRD from the last of the CCD memory stages. Interleaving is performed in three phases on a bit-by-bit basis.

During the data entry window all CCDs are set to the 'serpentine mode' in which a line of data leaving pin TID is written into the first CCD as the output data from the first CCD is written into the second CCD. This repeats through all the CCDs and results in a one-line shift of data through the whole memory, the last line becoming available at the TRD input.

When the 'full channel mode' is activated (FULL = HIGH):

- the BMC is forced to an internal OFF-state and incoming data lines are redirected to the computer-controlled teletext decoder (CCT, SAA5240), the data is not stored in the CCDs and no scan is made after a page request;
- the framing code can be recognized in all tv lines and not only during the data entry window.

FUNCTIONAL DESCRIPTION (continued)

Data scanning after a page request

The page-being-looked-for (PBLF) input from the CCTE originates in the CCT and indicates that the latter is searching for a requested page. As the PBLF input goes HIGH, the BMC activates the start scan output (SCN = LOW) and this presets an external counter and multiplexer (picture enhancement processor or TTL circuits). The preset value takes the multiplexer to the last CCD and therefore depends on the number of CCDs connected.

The multiplexer selects one CCD output at a time, starting with the last CCD (oldest information) and finishing with the first CCD (newest information). Three scans of the CCDs are required before all stored information is retrieved due to the three-phase interleaving (a memory with "n" CCDs will require a scanning period of 3n tv fields). Stepping of the counter/multiplexer occurs with the rising edge of MRN (at field flyback), and after each scan of all CCD outputs the external counter generates a terminal count signal TCN to initiate the next scan.

As each CCD is selected, the data is shifted from the memory by the clock F_{21} and supplied via the multiplexer to the teletext scan data pin TSD. A scanning circuit in the BMC selects one of the three phases from the CCD line for output, reducing the output bit-rate to one-third of F_{21}. The resulting bit stream is then synchronized to the CCT line-timing and fed to the CCT decoder that operates in the full-channel mode. The data packets retrieved by the scanning circuit are supplied at one packet per tv line via the output pin TTDO to the CCT decoder.

After the third scan of the CCDs, the BMC returns to the 'direct mode' in which it directs all incoming data lines to the CCT decoder and to the CCDs. This is necessary for updating a displayed page, or when a requested page was not found during the scan.

Repositioning of data

The BMC incorporates a variable length shift register in the output circuit supplying data TTDO. This accommodates a complete data line and introduces a delay that allows synchronization of the data to the CCT line-timing. The length of the delay depends on the position of the data in the tv line and on the RGB delay value that is programmed into the CCTE. In the BMC, the length of the delay is controlled automatically from the timing of $\overline{TCS}$ compared with the start of incoming data.

Refreshing CCD memories

CCD refreshing is required to maintain valid data and is done outside of the vertical blanking interval. At this time the 'serpentine mode' of the memory is broken and each CCD recirculates its contents once. To do this, the BMC supplies a sequence of 294 MG pulses (the number of memory lines per CCD) to all CCDs with recirculate activated (MRN = LOW). The MG signal is synchronized to the tv line frequency (one MG cycle per tv line) so that at the end of each tv field all data in the CCD arrays are returned to their original positions.

Clearing CCD memories

When a LOW-to-HIGH transition is detected at the CLCCD input, the scanning circuit is activated as follows:

- the memory recirculate control MRN is held HIGH except during the first line of the data entry window DEW (normally, MRN HIGH period is equal to DEW). This maintains the CCD serpentine mode during the recirculation time. The LOW on MRN during the first line of DEW acts as a clock input to the counter/multiplexer;
- the data output to the first CCD from pin TID is held LOW so that all CCDs are filled with zeros;
- the BMC is forced into the 'direct mode' so that no incoming teletext lines are missed during the CCD-clearing time.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage range (pin 13)	V_{DD}	−0,5 to + 7,0	V
Maximum supply current (pin 13)	I_{DD}	max. ▲	mA
Maximum supply current (pin 12)	I_{SS}	max. ▲	mA
Input voltage range (not F_6, TTCI)	V_I	−0,5 to (V_{DD}+ 0,5)*	V
Input voltage range (F_6, TTCI)	V_I	−0,5 to + 12	V
Maximum input current	$\pm I_I$	max. 10	mA
Maximum output current	$\pm I_O$	max. 10	mA
Operating ambient temperature range	T_{amb}	−25 to + 85	°C
Maximum power dissipation per output	P_O	▲	mW
Maximum power dissipation per package	P_{tot}	▲	W
Storage temperature range	T_{stg}	−55 to + 150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

D.C. CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range	V_{DD}	4,5	–	5,5	V
Quiescent supply current at T_{amb} = 25 °C; all inputs at V_{DD} or V_{SS}; TEST and TEST-A at 4,6 V; I_O = 0 mA	I_{DD}	–	–	100	μA
Inputs					
F_6 clock (a.c. coupled)					
D.C. input voltage	V_I	4,0	–	8,0	V
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	3,0	V
Leakage current	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	6	pF

▲ Values under investigation.

* V_{DD}+ 0,5 V not to exceed 8,0 V.

D.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Inputs (continued)					
TTCI data clock (a.c. coupled)					
D.C. input voltage	V_I	4,0	–	8,0	V
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	3,0	V
Leakage current	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	6	pF
F_{21}, TRD, TSD, $\overline{H}$, PBLF, CLCCD, ON, $\overline{TCS}$, TCN, TEST, TEST-A					
Input voltage LOW	V_{IL}	–	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	–	V
Leakage current at V_{IL}	I_{LI}	–	–	10	μA
Leakage current at V_{IH}	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	5	pF
Outputs TTDO, TTCO, TID, SCAN, SCN					
Output voltage LOW at I_{OL} = 2,0 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH at I_{OH} = 100 μA	V_{OH}	2,4	–	–	V
3-state outputs MRN, MG					
Output voltage LOW at I_{OL} = 2,0 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH at I_{OH} = 0,5 mA	V_{OH}	2,4	–	–	V
Leakage current at V_{OL}	I_{LO}	–	–	10	μA
Leakage current at V_{OH}	I_{LO}	–	–	10	μA
Input/output TTDI (input incorporates an active clamping circuit)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2,4	–	4,0	V
Input leakage current	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	6	pF
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V
External coupling capacitor	C_{ext}	–	10	–	nF

DEVELOPMENT DATA

A.C. CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Clocks F_6, TTCI (Fig. 3)					
F_6 frequency	f	–	6,0	–	MHz
F_6 rise and fall times (between 10% and 90% levels)	t_r, t_f	10	–	66	ns
TTCI frequency	f	–	6,9375	–	MHz
TTCI rise and fall times (between 10% and 90% levels)	t_r, t_f	10	–	57	ns
F_6, TTCI duty factor at d.c. level		30	50	70	%
Clock F_{21} (Fig. 4)					
Frequency	f	20,2	–	20,9	MHz
HIGH time	t_{CH}	17	–	–	ns
LOW time	t_{CL}	17	–	–	ns
Rise and fall times (between 0,8 and 2,0 V levels)	t_r, t_f	–	–	3	ns
Video processor interface (Fig. 3)					
Set-up time input to TTCI	t_{SU}	40	–	–	ns
Hold time TTCI to input	t_{IH}	40	–	–	ns
CCT decoder interface (Figs 3 and 5)					
TTCO clock output					
Frequency	f	–	$^1/_3 F_{21}$	–	MHz
Duty factor		40	–	60	%
Rise and fall times (between 10% and 90% levels)	t_r, t_f	–	–	40	ns
Load capacitance	C_L	–	–	50	pF
TTDO output, $\overline{TCS}$ input					
Set-up time $\overline{TCS}$ to F_6	t_{SU}	40	–	–	ns
Hold time F_6 to $\overline{TCS}$	t_{IH}	40	–	–	ns
Relative delay TTDO to TTCO	t_{RD1}	40	–	–	ns
Relative delay TTCO to TTDO	t_{RD2}	40	–	–	ns

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
CCTE interface (Fig. 3)					
Inputs $\overline{H}$, PBLF, CLCCD, ON; output SCAN					
Set-up time input to F_6	t_{SU}	40	–	–	ns
Hold time F_6 to input	t_{IH}	40	–	–	ns
Output delay F_6 to output	t_{OD}	–	–	40	ns
Load capacitance	C_L	–	–	50	pF
PEP, TTL, CCD interface (Figs 3 and 4)					
Inputs TRD, TSD; outputs TID, MG					
Set-up time input to F_{21}	t_{SU}	8	–	–	ns
Hold time F_{21} to input	t_{IH}	0	–	–	ns
Output delay F_{21} to output	t_{OD}	6	–	33	ns
TID load capacitance	C_L	–	–	25	pF
MG load capacitance	C_L	–	–	60	pF
Input TCN; outputs SCN, MRN					
Set-up time input to F_6	t_{SU}	40	–	–	ns
Hold time F_6 to input	t_{IH}	40	–	–	ns
Output delay F_6 to output	t_{OD}	–	–	40	ns
MRN load capacitance	C_L	–	–	70	pF
SC load capacitance	C_L	–	–	50	pF

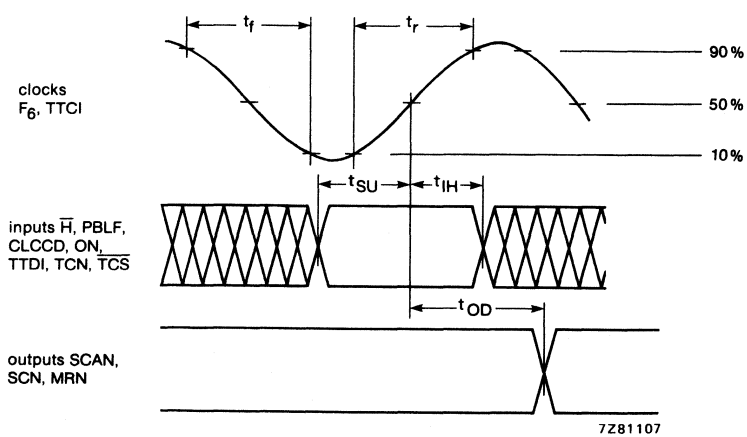


Fig. 3 Timing with respect to clocks F_6 and TTCI.

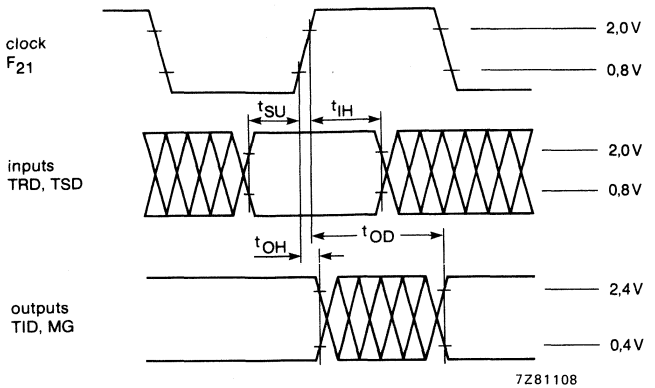


Fig. 4 Timing with respect to clock F_{21}.

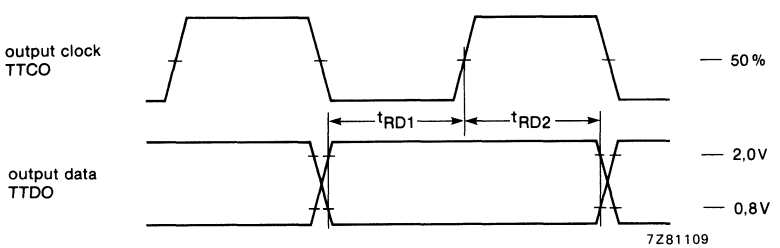


Fig. 5 Timing with respect to clock TTCO.

COMPUTER-CONTROLLED TELETEXT EXTENSION

GENERAL DESCRIPTION

The SAA9040 computer-controlled teletext extension (CCTE) for memory-based feature tv receivers is used together with a background memory controller (BMC, SAA9030) to organize the storage of teletext data in a field memory before processing by a CCT decoder (CCT, SAA5240). The CCTE shares the address and data buses of the CCT and a single-page display RAM and transfers commands indirectly from the I^2C bus to the BMC; it blanks the display for non-transmitted rows and provides the required delays for video/teletext operation.

The CCTE, together with the BMC, can be used in a 'stand-alone' system or with a picture enhancement processor (PEP, SAA9010) in feature television applications.

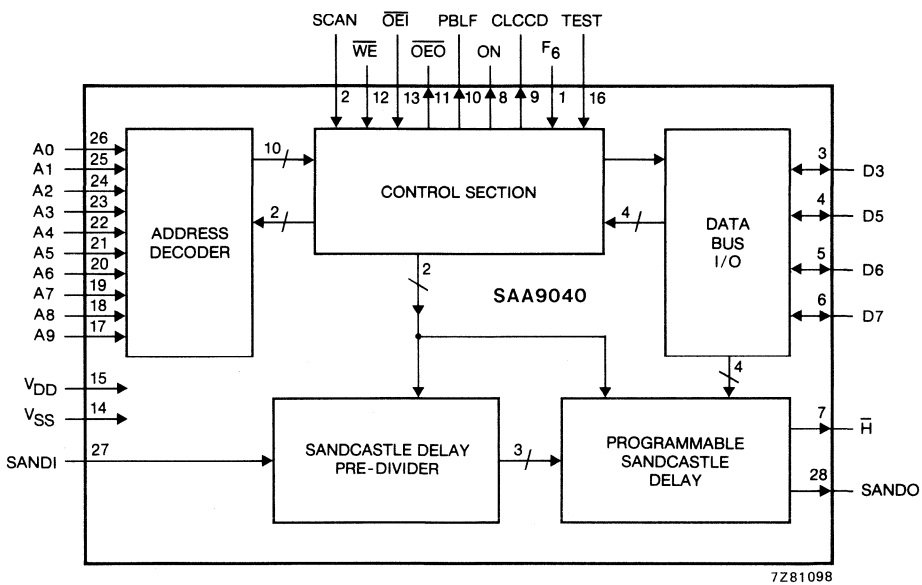


Fig. 1 Block diagram.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

PINNING

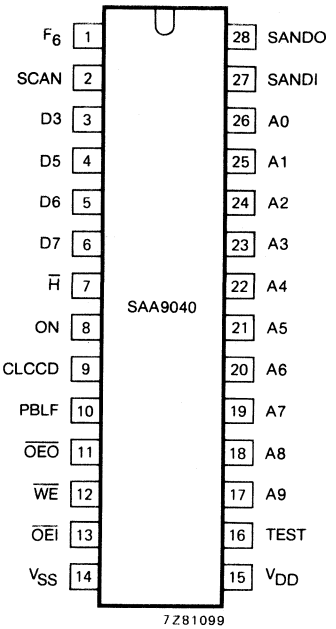


Fig. 2 Pinning diagram.

1	F_6	6 MHz clock input from the video input processor. Internal a.c. coupling
2	SCAN	input from BMC indicating that memory scanning is in progress
3 4 5 6	D3 D5 D6 D7	I/O data bus. Input used for commands into CCTE. Output if RAM address indicates rows not received from the page display RAM, D3, D5, D6 and D7 then force character codes on the data to effect an empty row
7	$\overline{H}$	horizontal timing output at tv line frequency. Derived from sandcastle pulse SANDO
8	ON	command output to activate BMC/CCD interface. Controlled initially by I^2C command. LOW after power-on
9	CLCCD	clear CCD command, output to BMC. Controlled initially by I^2C command
10	PBLF	page-being-looked-for, command output to BMC. This signal is a copy of the PBLF bit written into the page display RAM by the CCT
11	$\overline{OEO}$	output enable to page display RAM. Disables the RAM output if a row is not allowed for display
12	$\overline{WE}$	write enable input. Indicates that the CCT writes into the page display RAM. Is used in the control section of the CCTE to access the row-found register during acquisition and command transfer
13	$\overline{OEI}$	output enable input. Indicates that the CCT reads from the page display RAM. Is used in the control section of the CCTE to access the row-found flag register during display
14	V_{SS}	negative supply voltage (ground)

15	V_{DD}	positive supply voltage
16	TEST	test input. HIGH for normal operation
17	A9	address bus from the CCT to the page display RAM and CCTE. Decoding is performed in the CCTE control section to address the row-found flag and command registers
18	A8	
19	A7	
20	A6	
21	A5	
22	A4	
23	A3	
24	A2	
25	A1	
26	A0	
27	SANDI	sandcastle pulse input. A three-level signal from the CCT decoder giving phase lock and colour burst blanking information
28	SANDO	sandcastle pulse output to the teletext video processor. This pulse is a copy of SANDI delayed according to commands on the I^2C bus and is used to adjust the timing of the RGB signal.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

General

The CCTE shares data and address buses with the CCT and page display RAM. This allows indirect transfer of I^2C commands for system control, the I^2C commands being written to the RAM by the CCT and read from the RAM by the CCTE.

The following information is written to/read from the page display RAM:

information	*RAM location*	
received page	rows 0 to 23	
status row	row 24	
page-being-looked-for	row 25, col. 9, D5	additional page-related data
clear page bit from page header	row 25, col. 3, D3	additional page-related data
RGB delay	row 25, col. 11, D3, D5, D6, D7	data written to/read from RAM via CCT I^2C bus
CLCCD (clear CCDs)	row 25, col. 12, D5	data written to/read from RAM via CCT I^2C bus
ON (activate BMC)	row 25, col. 12, D3	data written to/read from RAM via CCT I^2C bus

Row-found flags

In the full channel acquisition mode, the CCT does not clear the page display RAM after it receives a requested page and does not respond to the page clear bit (C4) in page headers. These functions are performed by the CCTE which has 23 row-found flags (RFFs) for this purpose, one for each of the page display RAM rows 1 to 23. All RFFs are cleared on the rising edge of PBLF and on detection by CCTE of the page clear bit (C4 = 1) in the header of the requested page. An RFF is set when the CCT writes a character into the corresponding row of the RAM. During display, the CCT reads the row's contents sequentially from the RAM. Normally the RAM output enable ($\overline{OEO}$) is a copy of the output enable of the CCT ($\overline{OEI}$).

If a row is read and the corresponding RFF is not set, the output enable $\overline{OEO}$ is suppressed and the data bits D3, D5, D6 and D7 are forced LOW giving the effect of a row of spaces on the screen.

RGB delay

To compensate for delays in the video signal path, the CCTE regenerates the incoming sandcastle pulse with a delay that matches the timing of the CCT to that of the delayed (processed) video. The delay must be programmed into the page display RAM in the format shown in Table 1. The programmable values are in steps of 1 μs. For the combination CCTE + BMC only delays between 0 and 9 μs are applicable.

Table 1 RGB delay programming

address	row 25, column 11							
data bus	D7	D6	D5	D4	D3	D2	D1	D0
delay value (μs)	+ 8	+ 4	+ 2	–	+ 1	–	–	–

ON and CLCCD outputs

These signals are generated in the CCTE and fed to the BMC. When ON is LOW, the BMC/CCD memory interface is in its high impedance OFF-state. When CLCCD is HIGH, this instructs the BMC to clear the CCD memories. Both signals are initiated by the CCT software control with instructions sent via the I^2C bus and the CCT. The instructions are written into specific locations in the page display RAM which are accessed by the CCTE. The page display RAM locations are shown in Table 2.

Table 2 ON and CLCCD locations

address	row 25, column 12							
data bus	D7	D6	D5	D4	D3	D2	D1	D0
bit contents	–	–	CLCCD	–	ON	–	–	–

SCAN

This signal originates in the BMC. When HIGH, SCAN suppresses the output enable ($\overline{OEO}$) to the page display RAM causing the display to be blanked during a scan of the BMC. SCAN acts upon a complete page (excluding the status row and the page header) in the same way as an RFF acts upon a single row.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage range (pin 15)	V_{DD}	−0,5 to + 7,0	V
Maximum supply current (pin 15)	I_{DD}	max. ▲	mA
Maximum supply current (pin 14)	I_{SS}	max. ▲	mA
Input voltage range (not F_6)	V_I	−0,5 to (V_{DD} + 0,5)*	V
Input voltage range (F_6)	V_I	−0,5 to + 12	V
Maximum input current	$\pm I_I$	max. 10	mA
Maximum output current	$\pm I_O$	max. 10	mA
Operating ambient temperature range	T_{amb}	−25 to + 85	°C
Maximum power dissipation per output	P_O	▲	mW
Maximum power dissipation per package	P_{tot}	▲	W
Storage temperature range	T_{stg}	−55 to + 150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range	V_{DD}	4,5	–	5,5	V
Quiescent supply current at T_{amb} = 25 °C; all inputs at V_{DD} or V_{SS}; TEST and $\overline{OEI}$ at V_{DD}; I_O = 0 mA	I_{DD}	–	–	100	μA
Inputs					
F_6 clock (a.c. coupled)					
D.C. input voltage	V_I	4,0	–	8,0	V
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	3,0	V
Leakage current	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	6	pF

▲ Value under investigation.

* V_{DD} + 0,5 V not to exceed 8,0 V.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
$\overline{OEI}$, $\overline{WE}$, A0 to A9, SCAN					
Input voltage LOW	V_{IL}	–	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	–	V
Leakage current at V_{IL}	I_{LI}	–	–	10	μA
Leakage current at V_{IH}	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	5	pF
SANDI (multilevel signal, see Fig. 3)					
LOW tripping level (colour burst blanking)					
Input voltage LOW	V_{IL}	–	–	0,5	V
Input voltage HIGH	V_{IH}	1,0	–	–	V
HIGH tripping level (phase-lock)					
Input voltage LOW	V_{IL}	–	–	3,0	V
Input voltage HIGH	V_{IH}	3,9	–	–	V
Leakage current LOW	I_{LI}	–	–	10	μA
Leakage current INTERMEDIATE	I_{LI}	–	–	10	μA
Leakage current HIGH	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	5	pF
TEST					
Input voltage HIGH	V_{IH}	V_{DD}	–	–	V
Input current HIGH	I_{IH}	–	–	100	μA
Outputs					
$\overline{H}$, PBLF, ON, $\overline{OEO}$, CLCCD					
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH at I_{OH} = 100 μA	V_{OH}	2,4	–	–	V
SANDO (multilevel signal, see Fig. 3)					
Output voltage LOW at I_{OL} = 0,5 mA	V_{OL}	–	–	0,2	V
Output voltage INTERMEDIATE at $I_{OI} = \pm 30$ μA	V_{OI}	0,4 V_{DD} −0,5	0,4 V_{DD}	0,4 V_{DD} +0,5	V
Output voltage HIGH at I_{OH} = 30 μA	V_{OH}	V_{DD}−0,3	V_{DD}−0,15	V_{DD}	V
Inputs/outputs D3, D5, D6, D7					
Input voltage LOW	V_{IL}	–	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	–	V
Input leakage current at V_{IL}	I_{LI}	–	–	10	μA
Input leakage current at V_{IH}	I_{LI}	–	–	10	μA
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V

A.C. CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
ADDRESS and DATA to $\overline{WE}$ (Fig. 4)					
Set-up time from address change to start $\overline{WE}$	t_{SA}	50	–	–	ns
Hold time from end $\overline{WE}$ to address change	t_{HA}	0	–	–	ns
Set-up time from data stable to end $\overline{WE}$	t_{SD}	50	–	–	ns
Hold time from end $\overline{WE}$ to data change	t_{HD}	0	–	–	ns
$\overline{OEO}$ to ADDRESS and $\overline{OEI}$ (Figs 5 and 6)					
Delay from address change to negative edge of $\overline{OEO}$	t_{AOL}	–	–	50	ns
Delay from $\overline{OEI}$ to negative edge of $\overline{OEO}$	t_{IOL}	–	–	50	ns
Delay from address change to positive edge of $\overline{OEO}$	t_{AOH}	–	–	50	ns
Delay from $\overline{OEI}$ to positive edge of $\overline{OEO}$	t_{IOH}	–	–	50	ns
DATA to ADDRESS (Fig. 6)					
Address change to data valid	t_{OD}	50	–	–	ns
Hold time data to address change	t_{IZ}	0	–	–	ns
INPUTS and OUTPUTS to F_6 (Fig. 7)					
Set-up time input to F_6	t_{SU}	50	–	–	ns
Hold time input to F_6	t_{IH}	0	–	–	ns
Delay F_6 to output	t_{DO}	–	–	50	ns
Rise and fall times					
Inputs (except SANDI) reference levels 0,8 and 2,0 V	t_r, t_f	–	–	45	ns
Outputs (except SANDO) reference levels 0,4 and 2,4 V	t_r, t_f	–	–	25	ns
SANDI, SANDO (Fig. 3)					
rise time V_{OL} to V_{OI} reference levels 0,4 and 1,4 V	t_r	–	–	250	ns
rise time V_{OI} to V_{OH} reference levels 2,8 and 4,0 V	t_r	–	–	100	ns
fall time V_{OH} to V_{OL} reference levels 4,0 and 0,4 V	t_f	–	–	25	ns
Clock F_6					
Frequency	f	–	6,0	–	MHz

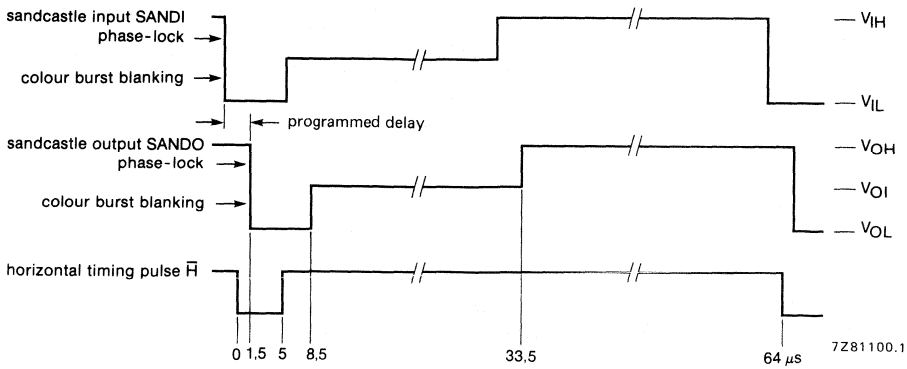


Fig. 3 Timing of sandcastle pulses.

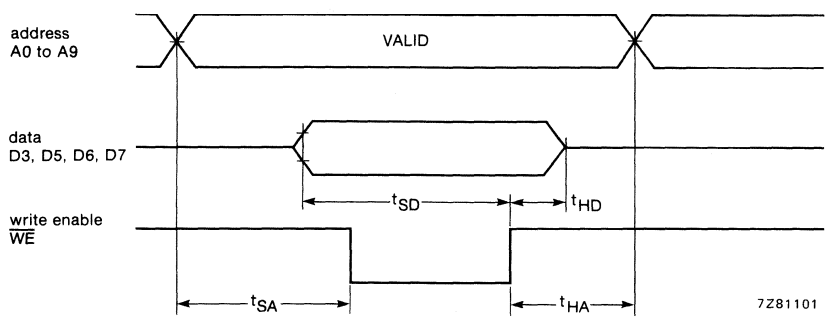


Fig. 4 Address/write enable/data timing.

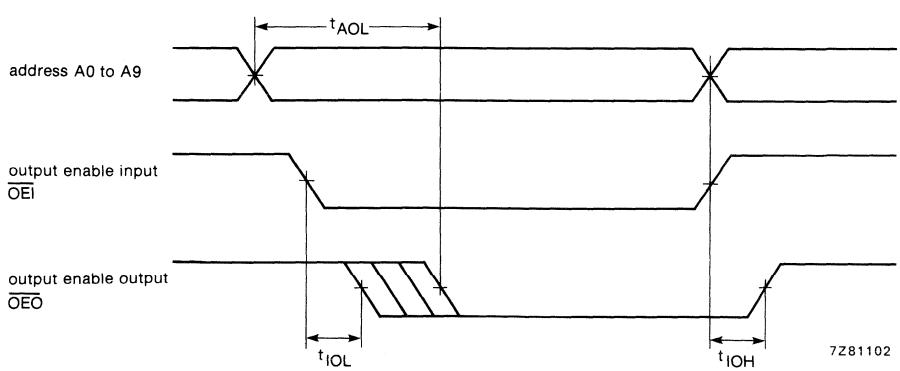


Fig. 5 Address/output enable timing.

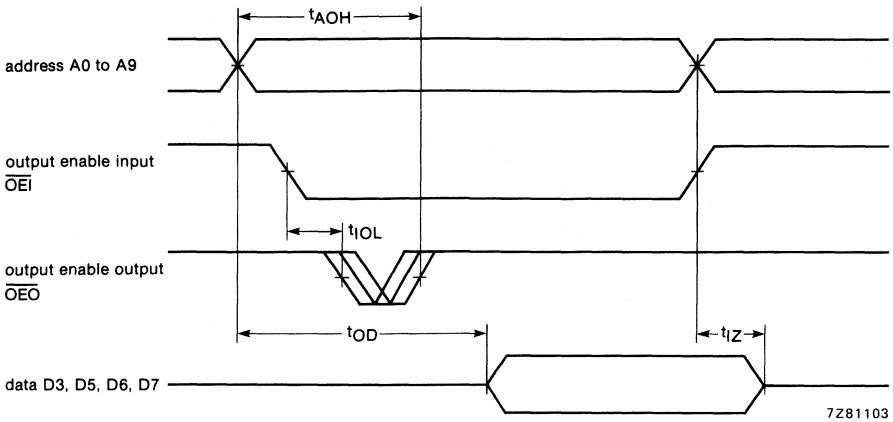


Fig. 6 Address/output enable/data timing.

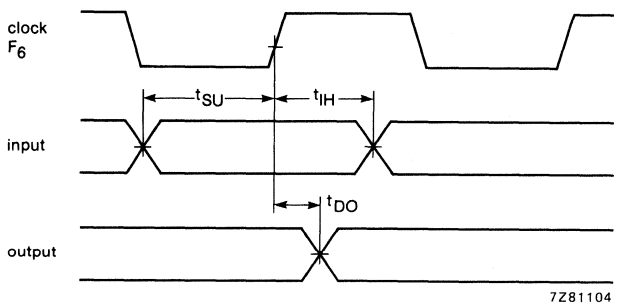


Fig. 7 Timing of inputs and outputs to F_6 clock.

DIGITAL MULTISTANDARD TV DECODER

GENERAL DESCRIPTION

The SAA9050 digital multistandard decoder (DMSD) performs demodulation and decoding of all quadrature modulated colour tv standards, and contains luminance and part-synchronization processing for all tv standards.

Features

- Luminance signal processing for all tv standards (PAL, NTSC, SECAM, B/W)
- Horizontal and vertical sync detection for all standards (525/625 lines)
- Chrominance signal processing for all quadrature amplitude modulated colour-carrier signals (PAL-B, G, H, I, M, N; NTSC-M, N)
- Requires only one crystal (24,576 MHz), which may also be used for audio processing
- Functions, settings and adjustments programmable under software control via the I^2C bus
- User-programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Multiplexed output format selectable (U, V, Y, Y, Y, Y)
- Parallel (nibble) output format selectable (Y/U6, U5, V6, V5; U4, U3, V4, V3; U2, U1, V2, V1; U0, CS, V0, PORS)
- SECAM interface
- Cross-colour reduction by chrominance comb-filtering (NTSC)
- Comb-filters adapt automatically to line frequency
- Internal overflow protection
- Selectable chrominance amplitude control protection for non-standard signals
- Programmable horizontal position of the active video signal in each line
- Indirect I^2C control capability to select input from one of four video sources
- Indirect I^2C control capability for automatic flesh-tone correction
- Wide range hue control
- Internal coincidence detection

PACKAGE OUTLINE

40-lead DIL; plastic with internal heat spreader (SOT-129).

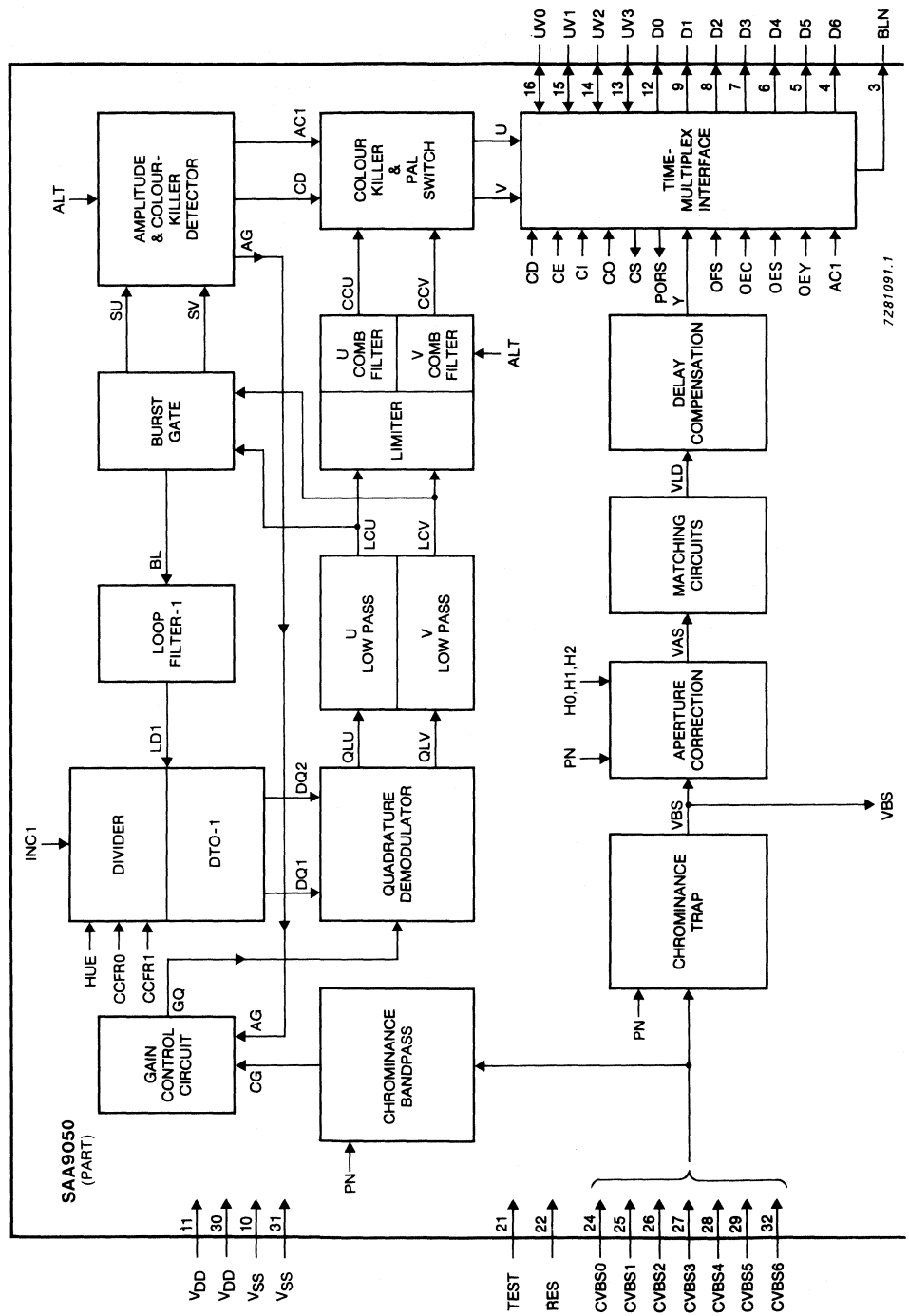


Fig. 1a Block diagram; continued in Fig. 1b.

DEVELOPMENT DATA

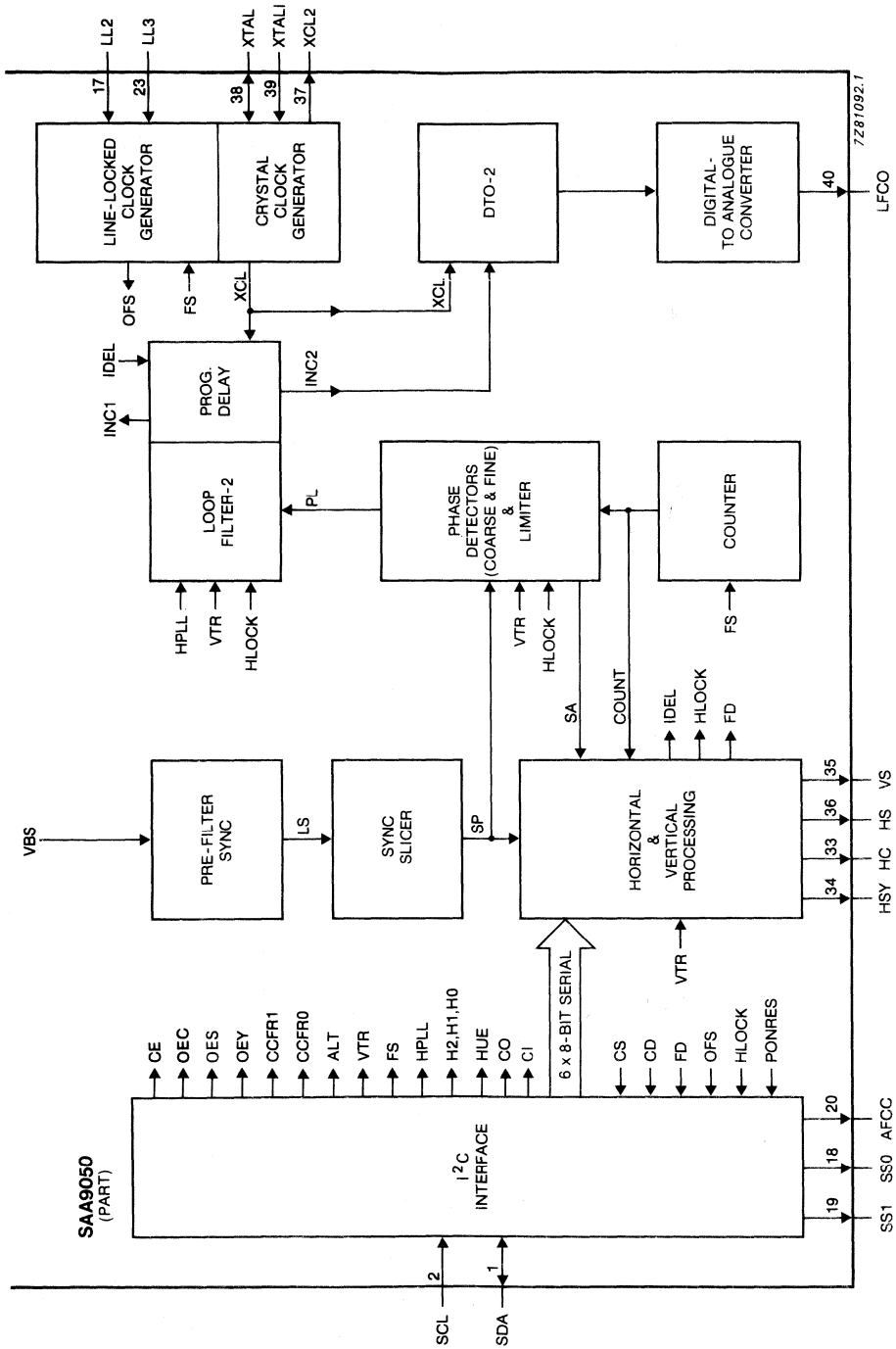


Fig. 1b Block diagram; from Fig. 1a.

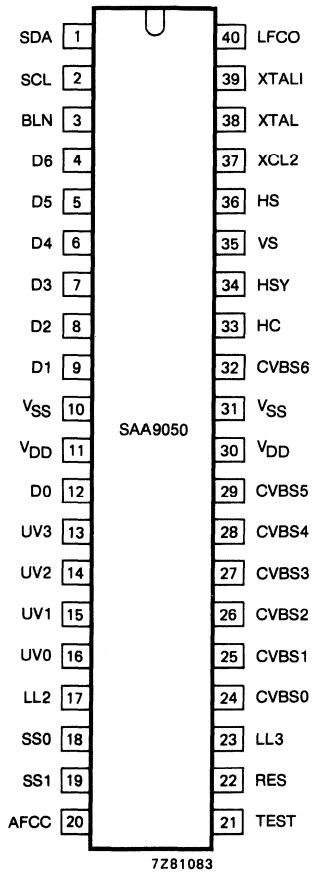


Fig. 2 Pinning diagram.

1	SDA	I^2C bus serial data input/output
2	SCL	I^2C bus serial clock input
3	BLN	Blanking output to indicate the active video and line blanking periods. Active LOW
4	D6(msb)	Colour difference outputs (U, V) with positive polarity plus luminance (Y)
5	D5	outputs, transmitted in a 20,25 MHz data stream with U, V, Y, Y, Y, Y serial
6	D4	format. The chrominance data is in two's complement and luminance is unipolar.
7	D3	The transmission is synchronized externally by BLN. The delay from CVBS
8	D2	input to D0-D6 output is 58 LL3 + 2 LL2 clocks in multiplexed format, and
9	D1	58 LL3 clocks in semi-parallel format. Luminance only is transmitted when
12	D0(lsb)	LL2 = LL3 = 13,5 MHz
10	V_{SS}	Ground (0 V)
11	V_{DD}	Positive supply voltage (+ 5 V)

DEVELOPMENT DATA

13 14 15 16	UV3 UV2 UV1 UV0	SECAM colour difference signal input/PAL or NTSC colour difference signal output. In the input mode, SECAM U, V, CS (colour-SECAM) and PORS (power-on-reset-SECAM) signals are received from the SECAM decoder. The output mode occurs when LL2 = LL3, then U and V signals are transmitted at 13,5 MHz. Input and output data formats are two's complement with positive polarity
17	LL2	20,25 MHz line-locked clock input used for multiplexed UVY-format. LL2 frequency is 13,5 MHz for semi-parallel format
18 19	SS0 SS1	Source-select output signals, set via the I^2C bus to control the input switch (e.g. TDA9045)
20	AFCC	Automatic flesh-tone correction control activated via the I^2C bus to control the colour-track circuit of NTSC systems
21	TEST	Test input, when HIGH enables the scan-test mode
22	RES	Reset input, active LOW, causes control registers 1 and 2 to be reset during the reset phase. The minimum LOW period of RES is 120 LL3 clocks
23	LL3	13,5 MHz line-locked system clock
24 25 26 27 28 29 32	CVBS0(lsb) CVBS1 CVBS2 CVBS3 CVBS4 CVBS5 CVBS6(msb)	Digitized composite video, blanking and synchronization signal containing luminance, chrominance and all synchronization information. Two's complement format
33	HC	Horizontal clamping signal that indicates the black-level position before analogue-to-digital conversion. The start and stop time is programmable via the I^2C bus in the range of −9,4 to + 9,5 μs in steps of 74 ns
34	HSY	Horizontal synchronization signal that indicates the sync pulse position before analogue-to-digital conversion. The start and stop time is programmable via the I^2C bus in the range of −14,2 to + 4,7 μs in steps of 74 ns
35	VS	Vertical synchronization output that indicates the vertical position of the picture for 50 or 60 Hz line frequency
36	HS	Horizontal synchronization pulse output. Duration = 16 LL3 clocks. Synchronizes the horizontal position of the active video signal in each line and is programmable via the I^2C bus in the range of −32 to + 32 μs in steps of 300 ns
37	XCL2	Clock output at half the crystal clock frequency (12,288 MHz). In phase with XTAL (pin 38)
38	XTAL	Crystal input/output. Input to the internal clock generator (from an external oscillator, when used), or output of the inverting amplifier to an external crystal (24,576 MHz)
39	XTALI	Input to the inverting amplifier from the external crystal (24,576 MHz); connected to ground when an external oscillator is used
40	LFCO	Line frequency control. Analogue output representing a multiple of the line frequency (6,75 MHz) with a 4-bit resolution, the phase of which is compared with the system clock by the clock generator circuit (SAA9057)

FUNCTIONAL DESCRIPTION (Fig. 1)

The DMSD performs demodulation and decoding for PAL-B, G, H, I, M, N, NTSC-M, N tv standards and contains luminance and parts of the synchronization processing for all PAL, NTSC and SECAM tv standards. All of the controllable functions of the DMSD, user controls as well as factory adjustments, are accessed via the two-line, bidirectional I^2C bus, so enhancing the adaptability of the digital tv concept.

Operation is based on a line-locked sampling frequency of 13,5 MHz, making the system fully adaptable to all line frequencies and requiring only one crystal for all tv standards.

Output formats (Fig. 3)

There are two output formats available via the time-multiplex interface that are controlled by the LL2 and LL3 clocks. The interface can also be used to incorporate an optional SECAM decoder.

LL2 = 20,25 MHz LL3 = 13,5 MHz	A multiplexed output data stream in the format U, V, Y, Y, Y, Y is transmitted from D0-D6 at a sample rate of 20,25 MHz, giving full compatibility with memory-based feature tv concepts.
LL2 = LL3 = 13,5 MHz	The Y and U, V signals are transmitted separately, the Y signals in a data stream of 13,5 MHz from D0-D6 and the U, V signals in a nibble format from UV0-UV3. The SECAM-decoder option also uses this clock mode.

Processing

The digital CVBS input is separated into its luminance (VBS) and chrominance (CG) parts by chrominance-trap and chrominance-bandpass circuits, both of which can be switched by the standard-identification signal (PN) according to the detected PN centre-frequency (3,58 or 4,43 MHz). The range of binary values for input/output signals are shown in Fig. 4.

The separated luminance signal (VBS) is passed to an aperture-correction circuit that has programmable horizontal peaking. The corrected signal (VAS) is then matched to the full-scale of the appropriate word-width and limited to prevent overflow. The signal (now VLD) undergoes delay compensation to equalize the delays of the luminance and chrominance channels. Differences of delay compensation requirements in PAL and NTSC modes are catered for when switching is performed by the standard-identification signal (PN).

In the chrominance channel, the amplitude of the chrominance signal (CG) is controlled to give a signal with constant burst amplitude (CQ). The control signal (AG) for gain-control is derived in the amplitude and colour-killer detection circuit. If there is a non-standard ratio between burst and chrominance amplitudes (−17% in the NTSC mode), an automatic colour-levelling circuit takes the function of amplitude detection to ensure correct chrominance amplitude and to avoid overflow and limiter defects.

Demodulation of the square-modulated chrominance signal (CQ) is performed by the quadrature demodulator which gives the baseband colour difference signals (LCU and LCV). The comb filter stage then separates remaining luminance components from these signals and (for PAL) corrects their phase to give the signals CCU and CCV. The number of delay elements required in the comb filter is minimized by the use of a reduced, blanked, line-locked clock. The comb filter structure is changeable under the control of the standard-identification signal (ALT).
The colour-killer, under the control of amplitude and colour-killer detection (AC1 and CD), removes incoming signals that do not comply with the chosen standard. The PAL switch restores the correct phasing of the V-signal when in PAL mode.

Regeneration of the colour carrier frequency is done by the phase-locked loop comprising quadrature modulator, lowpass filter, burst gate, loop filter-1 and discrete time oscillator (DTO-1). The latter is controlled by standard-identification signals (CCFR0, CCFR1) and a signal (HUE) that influences the demodulation phase of the chrominance signal.

In the synchronization circuit, pre-filter synchronization is implemented to normalize sync slopes. A sync-slicer provides the detected sync pulses (SP) to the H, V processing and phase detector stages.

The H and V processing comprises part of a PLL circuit for the regeneration of the horizontal synchronization (HS) and an adaptive filter for the detection of vertical sync (VS). The timing of VS is modified by the video recorder/tv time constant signal VTR (Fig. 5). The H, V processing also generates the coincidence signal (HLOCK) which controls the mute function, and a standard identification signal (FD) which identifies nominal 625 or 525 lines per picture.

The phase detectors that receive the SP signal, also part of the PLL, control the generation of the line-locked clock (PL). Loop filter-2, which has a changeable bandwidth controlled by the video recorder/tv time constant signal (VTR), generates two increment signals (INC1 and INC2) with different delays. INC2 is programmable via the increment-delay signal (IDEL). INC1 corrects the regenerated subcarrier frequency at DTO-1 and INC2 performs phase incrementing of DTO-2. The crystal clock generator provides a stable 24,576 MHz clock input to DTO-2 which in turn supplies the 4-bit DAC with a digital control signal of 432 or 429-times the line frequency. The analogue output (LFCO) from the DAC goes to the clock generator (SAA9057).

The output signals D0-D6 can be multiplexed under the control of an internal blanking and format signal. It is a time-multiplex-interface that also provides an external blanking and format signal (BLN).

For real-time inputs to the DMSD, the line-locked clocks LL2 and LL3 are required as well as the digital CVBS signal (CVBS0-CVBS6). As an option, a nibble-format colour difference input to UV0-UV3 can be used for interfacing a digital SECAM decoder. Under the control of the I^2C bus this interface can be switched into an output mode for outward transmission of colour difference signals U, V (LL2 = LL3 = 13,5 MHz).

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

I²C bus interface

The following control signals are received via the I²C bus (SDA and SCL) and the I²C bus interface:

- standard-identification signals (CCFR0, CCFR1, ALT, FS, CE)
- time constant VTR/TV (VTR)
- hue control (HUE)
- delay programming of the horizontal signals (HS, HC, HSY)
- increment delay (IDEL)
- aperture correction control (H0, H1, H2)
- fixed clock generation command (HPLL)
- internal colour ON/OFF (CO)
- internal colour forced-ON for test purposes (CI)
- sync output enable (OES)
- luminance output enable (OEY)
- chrominance output enable (OEC)
- source-select signal (SS0, SS1)
- automatic flesh-tone control (AFCC)

Signals transmitted from the DMSD via the I²C bus are:

- standard identification signals (FD, CS)
- colour killer status signal (CD)
- coincidence information (HLOCK)
- selected output format indicator (OFS)
- power-on-reset of DMSD (PONRES)

Time-multiplex interface (Fig. 6)

The UV0-UV3 signals from the SECAM decoder are received in a 13,5 MHz data stream in the following format:

input signal	sample 0	1	2	3	0	1	2	3
UV3	U6	U4	U2	U0	repeating			
UV2	U5	U3	U1	XU	repeating			
UV1	V6	V4	V2	V0	repeating			
UV0	V5	V3	V1	XV	repeating			

The signals XU and XV are information bits from the SECAM decoder, respectively CS and PORS:

CS = "0" indicates colour not detected in SECAM
CS = "1" indicates colour detected in SECAM
PORS = "0" after a complete initialization of all receiver bytes in the SECAM decoder
PORS = "1" after the first power-on-reset and after a severe power dip

These two bits are latched in the DMSD. The CS bit is transmitted to control circuits via the I²C bus. The PORS bit from the SECAM decoder is ORed with the internal power-on-reset signal to become PONRES.

Commands that control the outputs of the time-multiplex interface are OES, OEY, OEC, CO and CI which are received via the I^2C bus, and CD which is detected in the DMSD. The start condition of OES, OEY, OEC, CO and CI after initialization is always zero. The outputs are controlled as follows:

OES	OEY	OEC	outputs	output status
0 1	X X	X X	HS and VS	high impedance OFF-state active
X X	0 1	X X	D0-D6 and BLN	high impedance OFF-state active
X X	X X	0 1	UV0-UV3	high impedance OFF-state active

CO	CI	CD	outputs	output status
0	X	X	UV0-UV3 or UV samples of 'multiplexed output format (U, V, Y, Y, Y, Y)'	colour OFF (zero)
1 1	0 0	0 1		colour OFF } controlled colour ON } by CD
1	1	X		colour forced-ON

X = don't care.

FUNCTIONAL DESCRIPTION (continued)

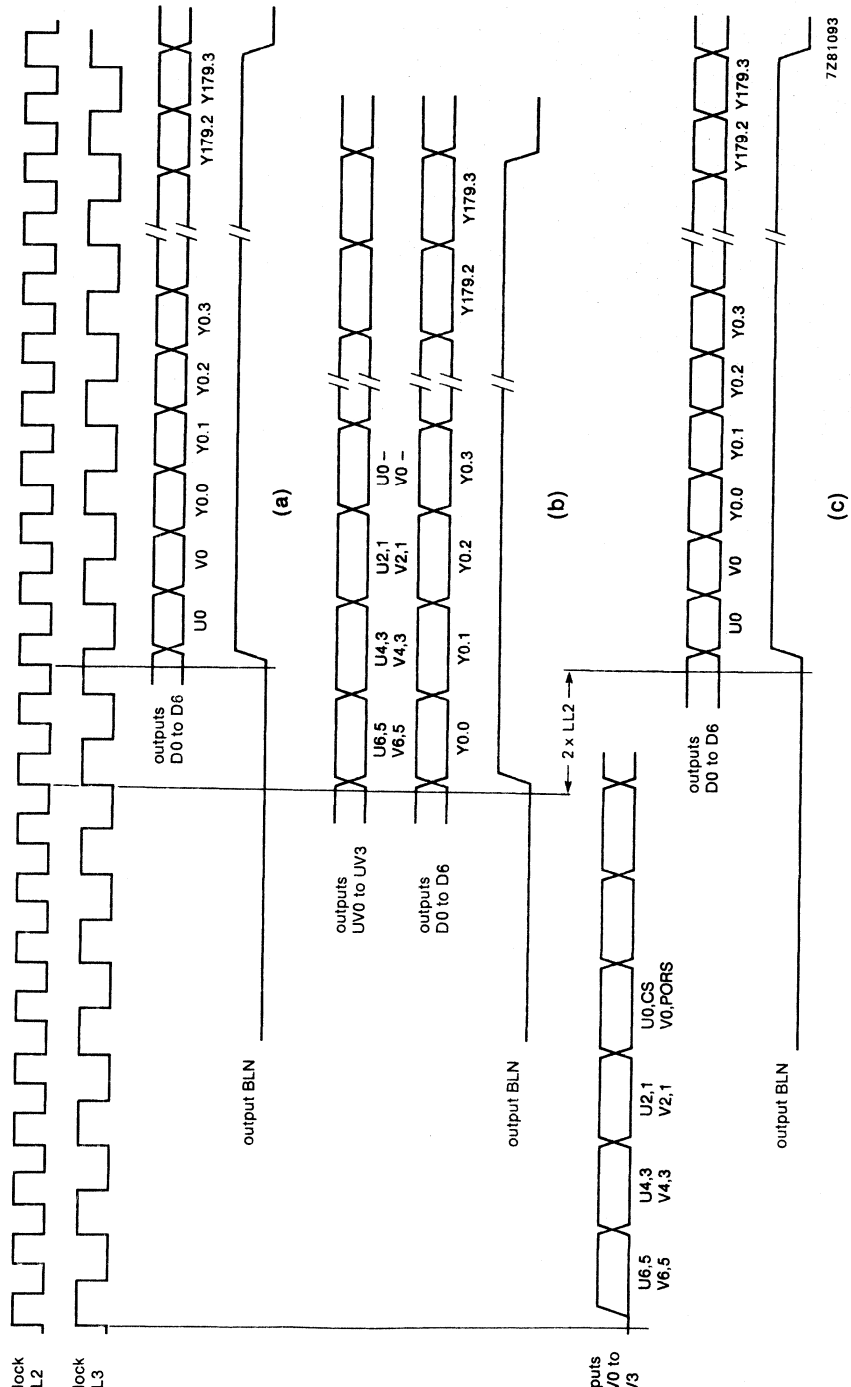
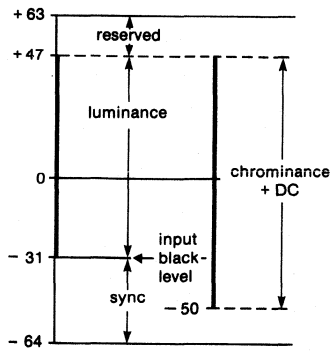
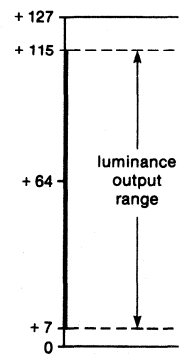


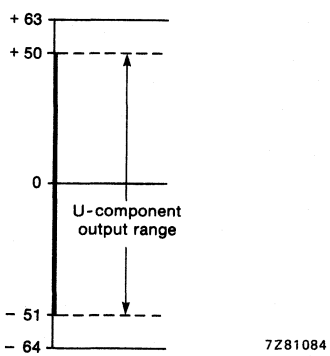
Fig. 3 Correlation of signals: (a) serial mode; (b) parallel (nibble) mode when LL2 = LL3 = 13,5 MHz; (c) serial mode in which SECAM chrominance signals (received via UV0-UV3 from a SECAM decoder) are combined with DMSD luminance signals.



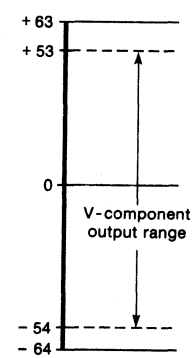
(a) CVBS0 to CVBS6 input range with 75% colour bar.



(b) Y output range.



(c) U output range (B–Y).



(d) V output range (R–Y).

Fig. 4 Diagram showing input/output range of the DMSD (levels are given in binary values).

FUNCTIONAL DESCRIPTION (continued)

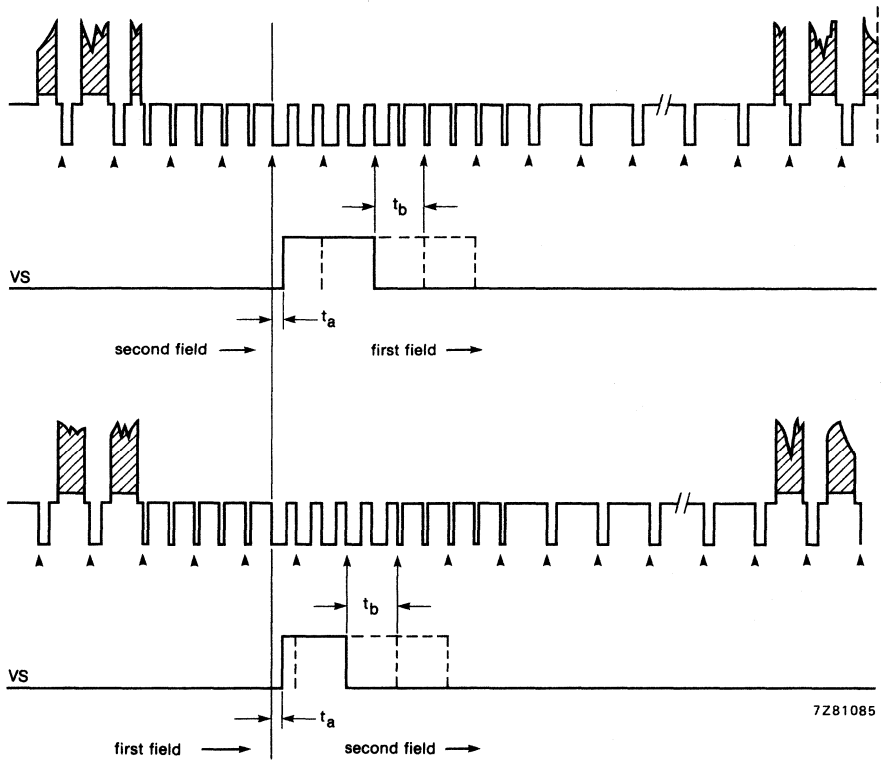


Fig. 5 Vertical sync (VS): time t_a is approximately 24 μs for tv signals and 10 μs for video recorder signals; time t_b = 64 μs (= the minimum vertical sync pulse length).

DEVELOPMENT DATA

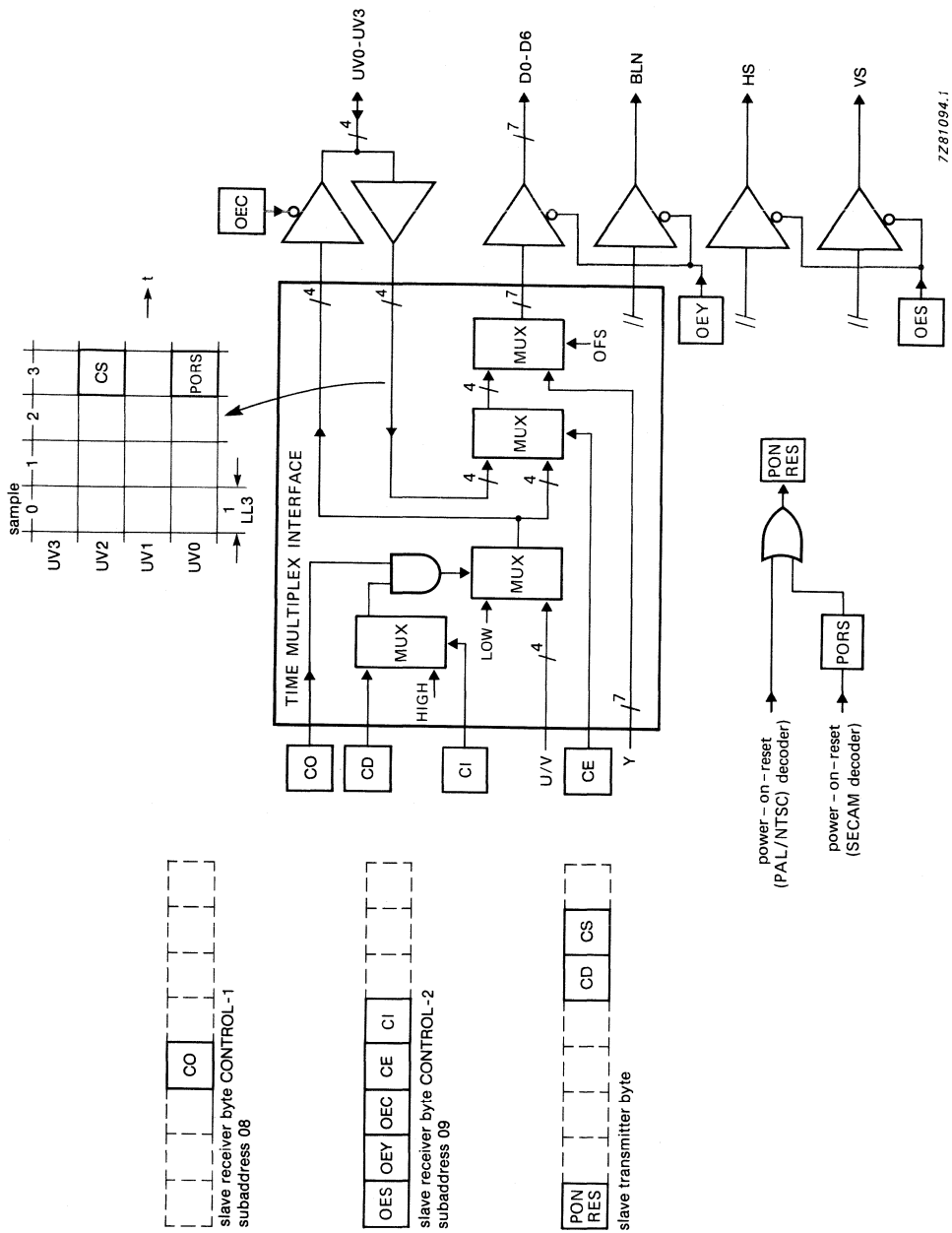


Fig. 6 Schematic diagram of control signals at the time-multiplex interface and output stages.

SLAVE RECEIVER ORGANIZATION

Slave address and receiver format

Slave address for the digital multistandard decoder is:

1	0	0	0	1	0	1

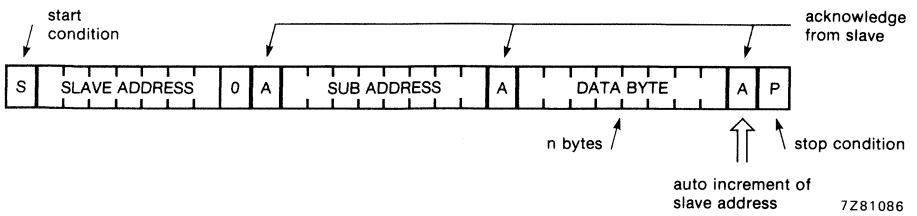


Fig. 7 Slave receiver format.

Subaddress byte and data byte formats

register function	sub address	data byte D7	D6	D5	D4	D3	D2	D1	D0
Increment delay IDEL	00	A07	A06	A05	A04	A03	A02	A01	A00
Horizontal sync									
HSY start time	01	A17	A16	A15	A14	A13	A12	A11	A10
HSY stop time	02	A27	A26	A25	A24	A23	A22	A21	A20
Horizontal clamp									
HC start time	03	A37	A36	A35	A34	A33	A32	A31	A30
HC stop time	04	A47	A46	A45	A44	A43	A42	A41	A40
Horiz. sync after PHI1									
HS start time	05	A57	A56	A55	A54	A53	A52	A51	A50
Horizontal peaking	06	X	X	X	X	X	H2	H1	H0
Hue control	07	A77	A76	A75	A74	A73	A72	A71	A70
Control 1	08	HPLL	FS	VTR	CO	ALT	CCFR2	CCFR1	CCFR0
Control 2	09	OES	OEY	OEC	CE	CI	AFCC	SS1	SS0
Reserved	0A to 0F	X	X	X	X	X	X	X	X

Notes

The subaddress is automatically incremented. This enables quick initialization by the I^2C bus controller within one transmission.

All eight bits of the subaddress have to be decoded by the device.

The subaddresses shown are acknowledged by the device. Subaddresses 10 to 1F (reserved for the SECAM decoder SAA9055) are not acknowledged. The subaddress counter wraps-around from 1F to 00. Subaddresses 20 to FF are not allowed.

X = don't care.

After power-on-reset the control registers 1 and 2 (subaddresses 08 and 09) are set to "0", all other registers are undefined.

The least significant bit of an analogue control or alignment register is defined as AX0.

DEVELOPMENT DATA

Increment delay control IDEL (application dependent)

decimal multiplier	delay time (step size = 2/13,5 MHz = 148 ns)	control bits* A07	A06	A05	A04	A03	A02	A01	A00
−1	−148 ns (min. value)	1	1	1	1	1	1	1	1
to									
−110	−16,3 μs (outside available range)	1	0	0	1	0	0	1	0
−111	−16,44 μs	1	0	0	1	0	0	0	1
to									
−214	−31,7 μs (max. value if FS = "1")	0	0	1	0	1	0	1	0
−215	−31,85 μs (outside central counter if FS = "1")**	0	0	1	0	1	0	0	1
−216	−32 μs (max. value if FS = 0)	0	0	1	0	1	0	0	0
−217	−32,148 μs (outside central counter if FS = "0")**	0	0	1	0	0	1	1	1
to									
−256	−37,9 μs (outside central counter)**	0	0	0	0	0	0	0	0

* A sign bit, designated A08 and internally set to HIGH, indicates values are always negative.

** The horizontal PLL does not function in this condition: the system clock frequency is set to a value fixed by the last update and is within ± 7,1% of the nominal frequency.

Horizontal sync HSY start time (application dependent)

decimal multiplier	delay time (step size = 1/13,5 MHz = 74 ns)	control bits A17	A16	A15	A14	A13	A12	A11	A10
+ 191	−14,2 μs (max. negative value)	1	0	1	1	1	1	1	1
to									
+ 1	−0,074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0,074 μs	1	1	1	1	1	1	1	1
to									
−64	+ 4,7 μs (max. positive value)	1	1	0	0	0	0	0	0

SLAVE RECEIVER ORGANIZATION (continued)

Horizontal sync HSY stop time (application dependent)

decimal multiplier	delay time (step size = 1/13,5 MHz = 74 ns)	control bits A27	A26	A25	A24	A23	A22	A21	A20
+ 191	−14,2 μs (max. negative value)	1	0	1	1	1	1	1	1
to									
+ 1	−0,074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0,074 μs	1	1	1	1	1	1	1	1
to									
−64	+ 4,7 μs (max. positive value)	1	1	0	0	0	0	0	0

Horizontal clamp HC start time (application dependent)

decimal multiplier	delay time (step size = 1/13,5 MHz = 74 ns)	control bits A37	A36	A35	A34	A33	A32	A31	A30
+ 127	−9,4 μs (max. negative value)	0	1	1	1	1	1	1	1
to									
+ 1	−0,074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0,074 μs	1	1	1	1	1	1	1	1
to									
−128	+ 9,5 μs (max. positive value)	1	0	0	0	0	0	0	0

Horizontal clamp HC stop time (application dependent)

decimal multiplier	delay time (step size = 1/13,5 MHz = 74 ns)	control bits A47	A46	A45	A44	A43	A42	A41	A40
+ 127	−9,4 μs (max. negative value)	0	1	1	1	1	1	1	1
to									
+ 1	−0,074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0,074 μs	1	1	1	1	1	1	1	1
to									
−128	+ 9,5 μs (max. positive value)	1	0	0	0	0	0	0	0

Horizontal sync after PHI1 HS start time (application dependent)

decimal multiplier	delay time (step size = 4/13,5 MHz = 296 ns)	control bits A57	A56	A55	A54	A53	A52	A51	A50
+ 127 to + 109	outside central counter range, no HS pulse detected	0	1	1	1	1	1	1	1
		0	1	1	0	1	1	0	1
+ 108	−32 μs (max. neg. value if FS = "0")	0	1	1	0	1	1	0	0
+ 107	outside central range if FS = "1"; −31,7 if FS= "0"	0	1	1	0	1	0	1	1
+ 106	−31,4 μs (max. neg. value if FS = "1")	0	1	1	0	1	0	1	0
to + 1	−0,296 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −107	+ 0,296 μs	1	1	1	1	1	1	1	1
	+ 32 μs (max. pos. value, FS = "0" or "1")	1	0	0	1	0	1	0	1
−108 to −128	outside central counter range, no HS impulse detected	1	0	0	1	0	1	0	0
		1	0	0	0	0	0	0	0

DEVELOPMENT DATA

SLAVE RECEIVER ORGANIZATION (continued)

Horizontal peaking H2, H1, H0, PN (user dependent) (see Fig. 13)

PN = "0" when all CCFRx flags are "0" (4,43 MHz); PN = "1" if any one CCFRx flag is not "0" (3,58 MHz).

aperture factor (af)	control bits H2	H1	H0	PN
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1	1	0	0
7	1	1	1	0
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1

Hue phase (user dependent)

hue phase	control bits A77	A76	A75	A74	A73	A72	A71	A70
+ 178,6 deg to	1	1	1	1	1	1	1	1
0 deg to	1	0	0	0	0	0	0	0
−180 deg	0	0	0	0	0	0	0	0

Step size per least-significant bit (A70) = 1,4 deg.

Reference point for positive colour difference signals = 0 deg.

The hue phase may be shifted ± 180 deg from the reference point using bit A77, the colour difference signals are then switched from normal positive to negative polarity.

Horizontal clock PLL (application dependent)

function	HPLL control bit
horizontal clock PLL open, horizontal frequency fixed	1
horizontal clock PLL closed	0

Field frequency select (system mode dependent)

function	FS control bit
60 Hz; 525-line mode	1
50 Hz; 625-line mode	0

VTR/TV mode select (system mode dependent)

function	VTR control bit
VTR mode	1
TV mode	0

DEVELOPMENT DATA

SLAVE RECEIVER ORGANIZATION (continued)

Colour-on control (system mode dependent)

function	CO control bit
colour-ON	1
colour-OFF (all colour output samples zero)	0

Alternate/non-alternate mode (system mode dependent)

function	ALT control bit
alternate mode (PAL)	1
non-alternate mode (NTSC)	0

Colour carrier frequency control (system mode dependent)

colour carrier frequency	control bits CCFR2	CCFR1	CCFR0
4 433 618,75 Hz (PAL-B, G, H, I; NTSC-4,43)	0	0	0
3 575 611,49 Hz (PAL-M)	0	0	1
3 582 056,25 Hz (PAL-N)	0	1	0
3 579 545 Hz (NTSC-M)	0	1	1

Colour decoding table

colour standard	control bits FS				ALT	CCFR2	CCFR1	CCFR0
PAL-B, G, H, I		0			1	0	0	0
NTSC-4,43		0			0	0	0	0
PAL-M	HPLL	1	VTR	CO	1	0	0	1
PAL-N		0			1	0	1	0
NTSC-M		1			0	0	1	1

Sync output enable (system mode dependent)

function	control bit OES
outputs HS and VS active	1
outputs HS and VS high-Z	0

Y-output enable (system mode dependent)

function	control bit OEY
outputs D0-D6 and BLN active	1
outputs D0-D6 and BLN high-Z	0

Chrominance output enable (system mode dependent)

function	control bit OEC
outputs UV0-UV3 active; chrominance signal when CD = "1"; zero signal when CD = "0"	1
outputs UV0-UV3 high-Z	0

External colour-select (system mode dependent)

function	control bit CE
select external colour channel; serial format via inputs UV0-UV3	1
select internal colour channel	0

Internal colour forced-ON/OFF (for test or service requirements only)

function	control bit CI
colour forced-ON if CO = '1' (CD = 'X') colour OFF if CO = '0' (CD = 'X')	1
colour OFF if CO = '0' (CD = 'X') colour controlled by CD if CO = '1'	0

X = don't care

Automatic fleshtone corrector (colour track) (user dependent)

function	AFCC control bit
colour track ON	1
colour track OFF	0

Source-select (system mode dependent)

function	control bits SS1	SS0
select input CVBS0	0	0
select input CVBS1*	0	1
select input CVBS2	1	0
select input CVBS3	1	1

* not allowed when working with TDA9045.

DEVELOPMENT DATA

SLAVE TRANSMITTER ORGANIZATION

Slave transmitter format

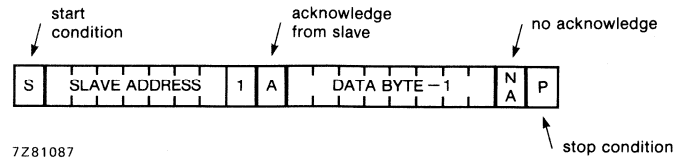


Fig. 8 Slave transmitter format (a general call address is not acknowledged).

The format of data byte-1 is:

PONRES	HLOCK	OFS	FD	0	CD	CS	0

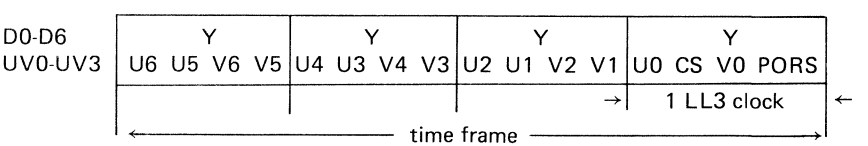
PONRES — Status bit for power-on-reset/power-failure:
"1" after the first power-on-reset and after a power failure. Also set to "1" after a severe voltage dip that may have disturbed slave receiver data in the PAL/NTSC decoder (SAA9050) or SECAM colour decoder (SAA9055). The PORS bit from the SECAM colour decoder is ORed with the internal power-on-reset signal to give the PONRES bit. PONRES sets all data bits of control registers 1 and 2 to zero.

"0" after a successful read of the PAL/NTSC decoder status byte and, if a SECAM decoder is included in the system, following the complete initialization of all SECAM decoder receiver bytes.

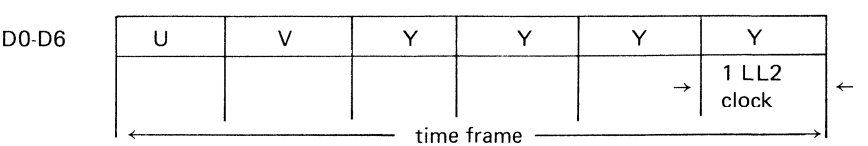
HLOCK — Status bit for horizontal frequency lock (transmitter identification, stop or mute bit):
"1" if horizontal frequency is not locked (no transmitter available);

"0" if horizontal frequency is locked (transmitter received).

OFS — Status bit for output format selection:
"1" when quasi-parallel format is selected:



"0" when serial output format is selected:



FD — Detected field frequency status bit:
"1" when received signal has 60 Hz sync pulses;
"0" when received signal has 50 Hz sync pulses.

CD — PAL/NTSC colour-detected status bit:
"1" when PAL/NTSC colour signal is detected;
"0" when no PAL/NTSC colour signal is detected.

CS — SECAM colour-detected status bit:
"1" when SECAM colour signal is detected;
"0" when no SECAM colour signal is detected.

PROGRAMMING IDEL, HSY, HC and HS

These variables are programmed via data words on the I^2C bus. In the following examples decreasing numbers correspond to increasing time.

IDEL (Fig. 9)

The IDEL data word compensates for time delays in data processing between loop filter-2 and the quadrature demodulator and includes internal and external (system) signal paths. The internal path from loop filter-2 takes INC1 to the divider and DTO-1. This delay (t_{REF}) corrects the relationship between the subcarrier frequency and the line frequency. The external path accounts for the following time delays:

t_{IDEL}	programmable delay time
t_a	processing time of DTO-2 and the D-A converter
t_b	chrominance bandpass and gain control stage delay times
t_{CGC}	clock generator circuit delay time
t_{ADC}	analogue-to-digital converter delay time
t_{SRC}	sample-rate converter delay time
t_{SECAM}	SECAM colour decoder delay time

As the delays t_a and t_b are known constants, t_{IDEL} is programmed as follows:

$t_{IDEL} = -115 - 0{,}5\,(99 - t_{CGC} - t_{ADC} - t_{SRC}{}^{*} - t_{SECAM}{}^{*})$

Programming range: −115 to −214/−216 μs.

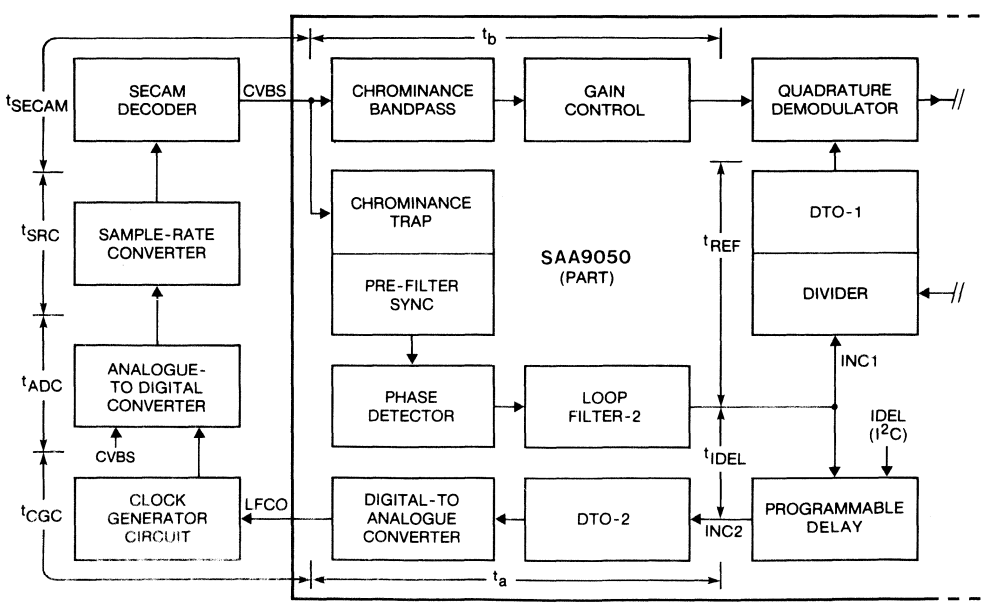


Fig. 9 Compensation of delay times by increment delay control IDEL.

* When included in the application.

PROGRAMMING IDEL, HSY, HC and HS (continued)

HSY (Fig. 10)

Referring to Fig. 10 points (1), (2) and periods 'a', 'b':

HSY start time $= T_{(1)\_(2)} + 42 - a$ LL3 clock periods

HSY stop time $= T_{(1)\_(2)} + 42 - b$ LL3 clock periods

Programming range of HSY start/stop time: + 191 to −64 LL3 clock periods.

HC (Fig. 10)

Referring to Fig. 10 points (1), (2) and periods 'c', 'd':

HC start time $= T_{(1)\_(2)} + 42 - c$ LL3 clock periods

HC stop time $= T_{(1)\_(2)} + 42 - d$ LL3 clock periods

Programming range of HC start/stop time: + 127 to −128 LL3 clock periods.

HS (Fig. 10)

The reference positions of HS in PAL and NTSC modes are shown in Fig. 10 at points (4) and (5) respectively. To move the HS pulse to the centre of blanking pulse BLN the following equation is used:

$$\text{HS (NTSC)} : \frac{-[\text{position of HS relative to point (3)} + 17\ \text{LL3}]}{4\ \text{LL3}}$$

$$\text{HS (PAL)} : \frac{-[\text{position of HS relative to point (3)} + 14\ \text{LL3}]}{4\ \text{LL3}}$$

In the example given in Fig. 10:

HS (NTSC) : $-[55 + 17]/4 = -18$ (decimal) = 1110 1110 (binary)

HS (PAL) : $-[62 + 14]/4 = -19$ (decimal) = 1110 1101 (binary)

DEVELOPMENT DATA

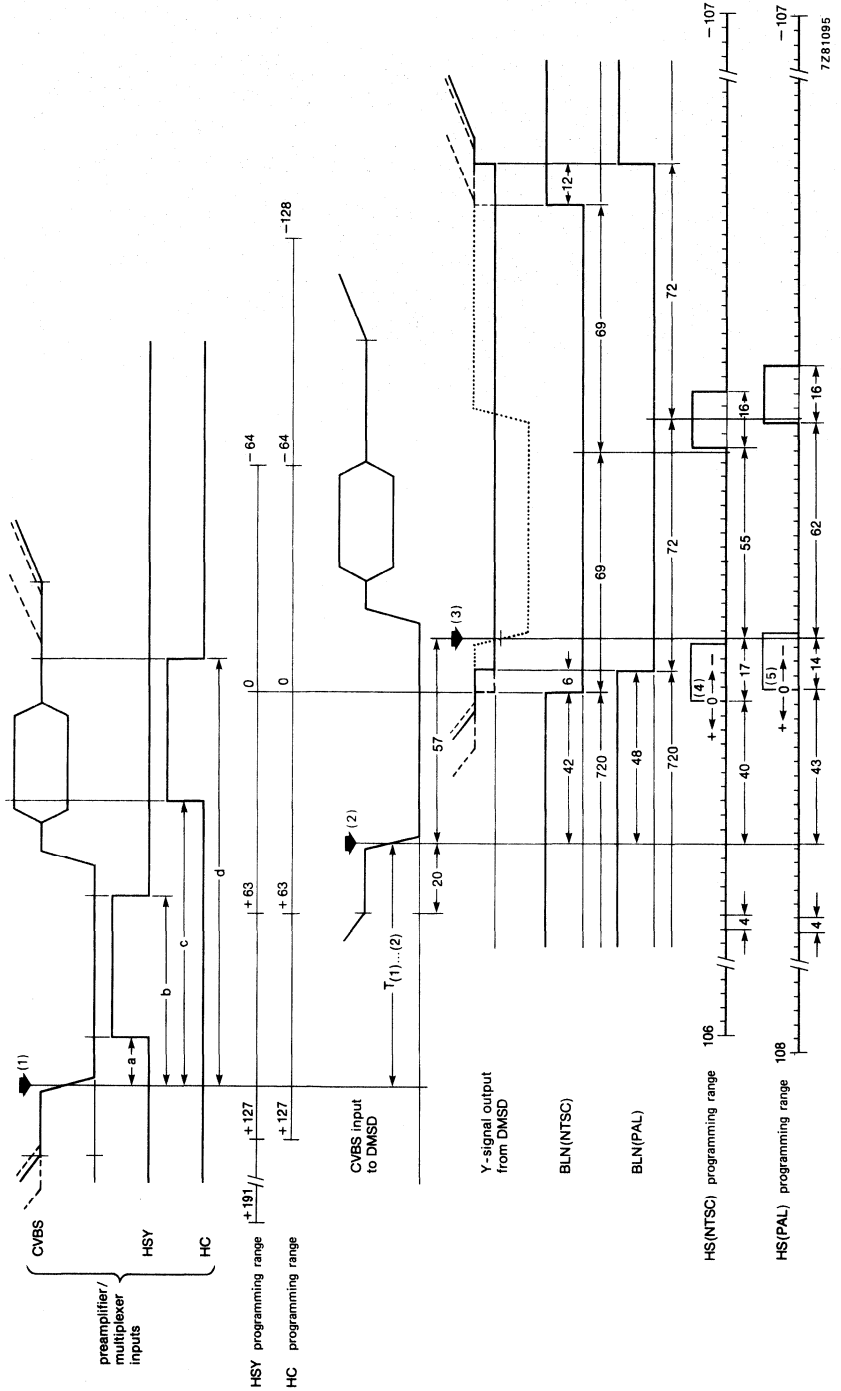


Fig. 10 Signal correlation (see notes on next page).

Notes to Fig. 10

——— represents PAL signals
– – – – represents NTSC signals (showing tolerance of active video)

HSY and HC inputs are referenced to the analogue input CVBS (1)

BLN and HS outputs are referenced to the digital input DCVBS (2) or to the DMSD output (3).

Waveform timing is indicated in numbers (n) of LL3 cycles ($n \times 1/f_{LL3}$), where n = 1 for HSY, HC, CVBS input to DMSD and BLN, and n = 4 for HS.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to + 7,0 V
Input voltage range	V_I	−0,5 to + 7,0 V
Output voltage range (max. output current $I_{O\,max}$ = 20 mA)	V_O	−0,5 to + 7,0 V
Maximum power dissipation per package	P_{tot}	tbf W
Operating ambient temperature range	T_{amb}	0 to + 70 °C
Storage temperature range	T_{stg}	−65 to + 150 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; T_{amb} = 0 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	300	tbf	mA
Inputs					
Input voltage LOW:					
pins 13 to 17, 21 to 29, 32 and 38	V_{IL}	−0,5	–	+ 0,8	V
pins 1 and 2	V_{IL}	−0,5	–	+ 1,5	V
Input voltage HIGH:					
pins 13 to 16, 21, 22, 24 to 29 and 32	V_{IH}	2,0	–	V_{DD}	V
pins 1, 2 and 38	V_{IH}	3	–	V_{DD}	V
pins 17 and 23	V_{IH}	2,4	–	V_{DD}	V
Input leakage current:					
pins 1, 2, 13 to 17, 21 to 29, 32 and 38	I_I	–	–	10	μA
Input capacitance:					
pins 17 and 23	C_I	–	–	10	pF
pins 13 to 16, 21, 22, 24 to 29, 32, 38 and 39	C_I	–	–	5	pF
Outputs					
Output capacitance pins 4 to 9 and 12	C_O		tbf		pF
Output voltage LOW:					
pins 3 to 9, 12 to 16, 18 to 20 and 33 to 37 at I_{OL} = 2,0 mA	V_{OL}	0	–	0,4	V
pin 1 at I_{OL} = 5 mA	V_{OL}	0	–	0,45	V

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Outputs (continued)					
Output voltage HIGH: pins 1, 3 to 9, 12 to 16, 18 to 20 and 33 to 37 at $I_{OH} = -0,5$ mA	V_{OH}	2,4	–	V_{DD}	V
LFCO output (pin 40, a.c. coupled) 4-bit triangular waveform clocked at 24,576 MHz (peak-to-peak value):					
$R_L \geqslant 10$ kΩ; $C_L < 15$ pF	$V_{O(p-p)}$	1	–	–	V
$R_L \geqslant 1$ kΩ; $C_L < 15$ pF	$V_{O(p-p)}$	0,5	–	–	V
Timing (Fig. 11)					
LL2 cycle time	t_{C2}	46*	49,4	60*	ns
LL2 HIGH time	t_{C2H}	20	–	–	ns
LL2 LOW time	t_{C2L}	20	–	–	ns
LL2 rise and fall times	t_r, t_f	–	–	3	ns
LL3 cycle time	t_{C3}	69*	74	80*	ns
LL3 HIGH time	t_{C3H}	30	–	–	ns
LL3 LOW time	t_{C3L}	30	–	–	ns
LL3 rise and fall times	t_r, t_f	–	–	3	ns
Skew time LL2/LL3	t_{skew}	−2	–	+ 2	ns
Input set-up time	t_{SU}	12	–	–	ns
Input hold time	t_{IH}	3	–	–	ns
Output hold time at C_L = 7,5 to 15 pF	t_{OH}	3	–	–	ns
Output delay time at C_L = 7,5 to 15 pF	t_{OD}	–	–	33	ns
Crystal oscillator (Fig. 12)					
Crystal frequency	f	–	24,576	–	MHz
Crystal frequency tolerance	Δf	–	–	± 2,4	kHz
Colour killer					
Switching levels at 75% PAL colour bar:					
Colour-OFF (PAL)		–	−34	–	dB
Colour-ON (PAL)		–	−31	–	dB
Colour-OFF (NTSC)		–	−30	–	dB
Colour-ON (NTSC)		–	−27	–	dB
Colour levelling					
Switching level against nominal burst		–	−1,3	–	dB
Control range of automatic gain control		–	30	–	dB
Capture range of subcarrier PLL (w.r.t. subcarrier nominal frequency)	Δf_{sc}	–	–	± 740	Hz
H-PLL frequency range					
Deviation about centre frequency:					
maximum static and dynamic deviation	Δf_o	–	–	± 7,1	%
maximum static deviation	Δf_o	–	–	± 5,8	%
Horizontal peaking		see Fig. 13			

* For min. and max. cycle times Δf = ± 7,1% of typical frequency value.

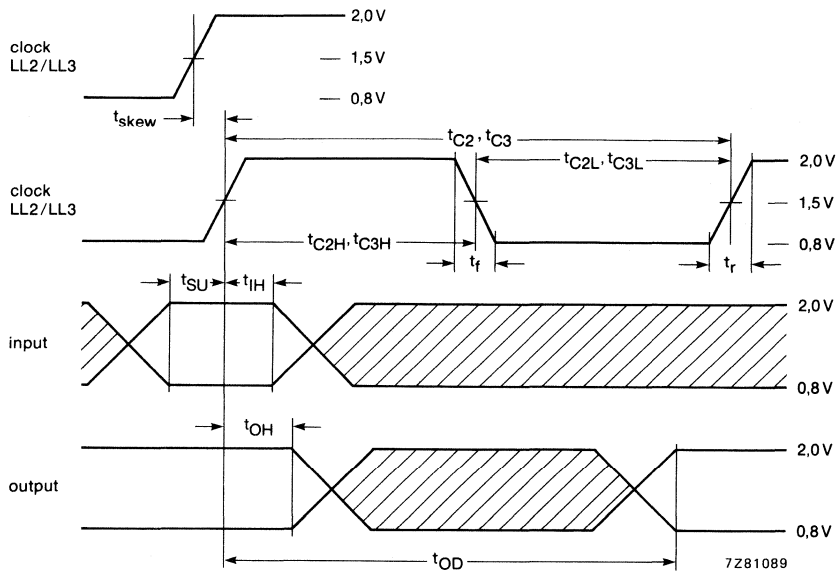


Fig. 11 Timing diagram.

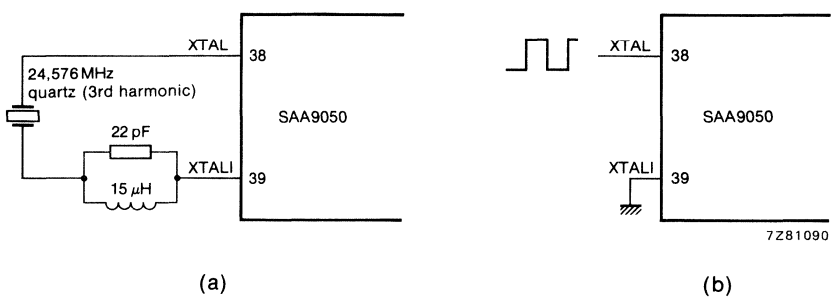
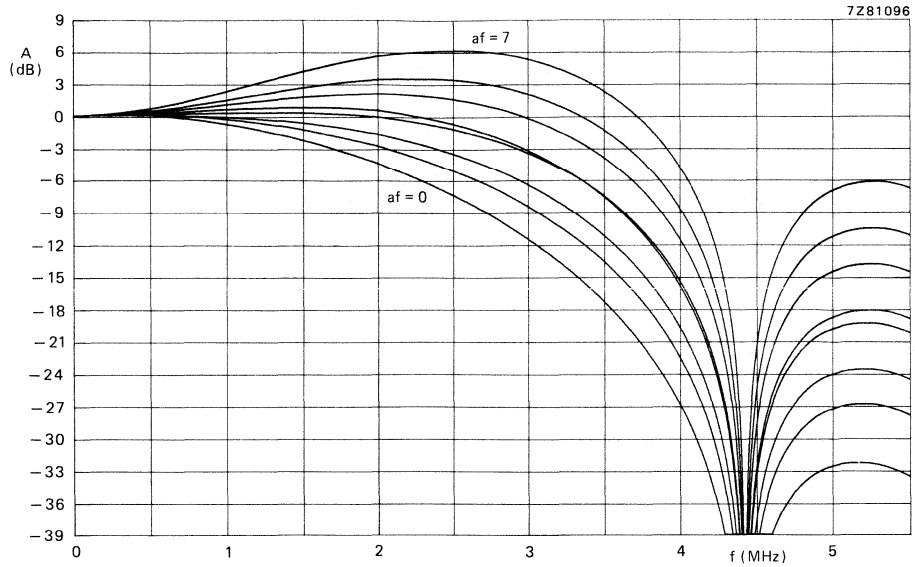


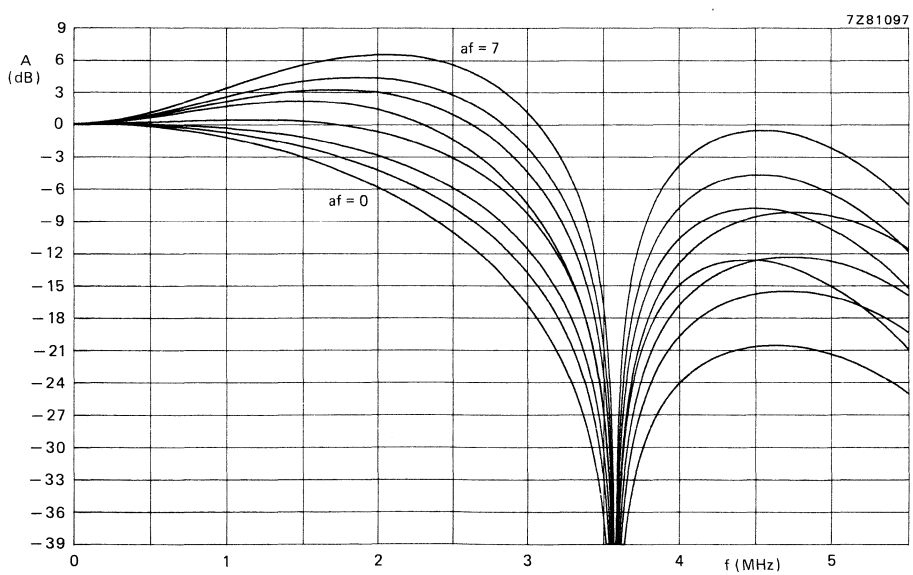
Fig. 12 Oscillator circuit requirements: (a) with quartz crystal; (b) with external clock.

DEVELOPMENT DATA

(a)



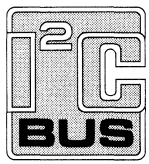
(b)



Aperture factor selection:

af	H2	H1	H0
0	0	0	0
– – – –	through to	– – – –	
7	1	1	1

Fig. 13 Horizontal peaking aperture factors (af): (a) PN = "0" (colour subcarrier = 4,43 MHz); (b) PN = "1" (colour subcarrier = 3,58 MHz).



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CLOCK GENERATOR CIRCUIT

GENERAL DESCRIPTION

The SAA9057 clock generator circuit is for application in memory-based feature tv receivers and in digital tv concepts with line-locked sampling. The circuit employs a PLL frequency multiplier to give three different line-locked clock output frequencies, a bypass switch for the PLL is provided. All clock outputs have high driving capability. Skew control and power-fail detection circuits are included.

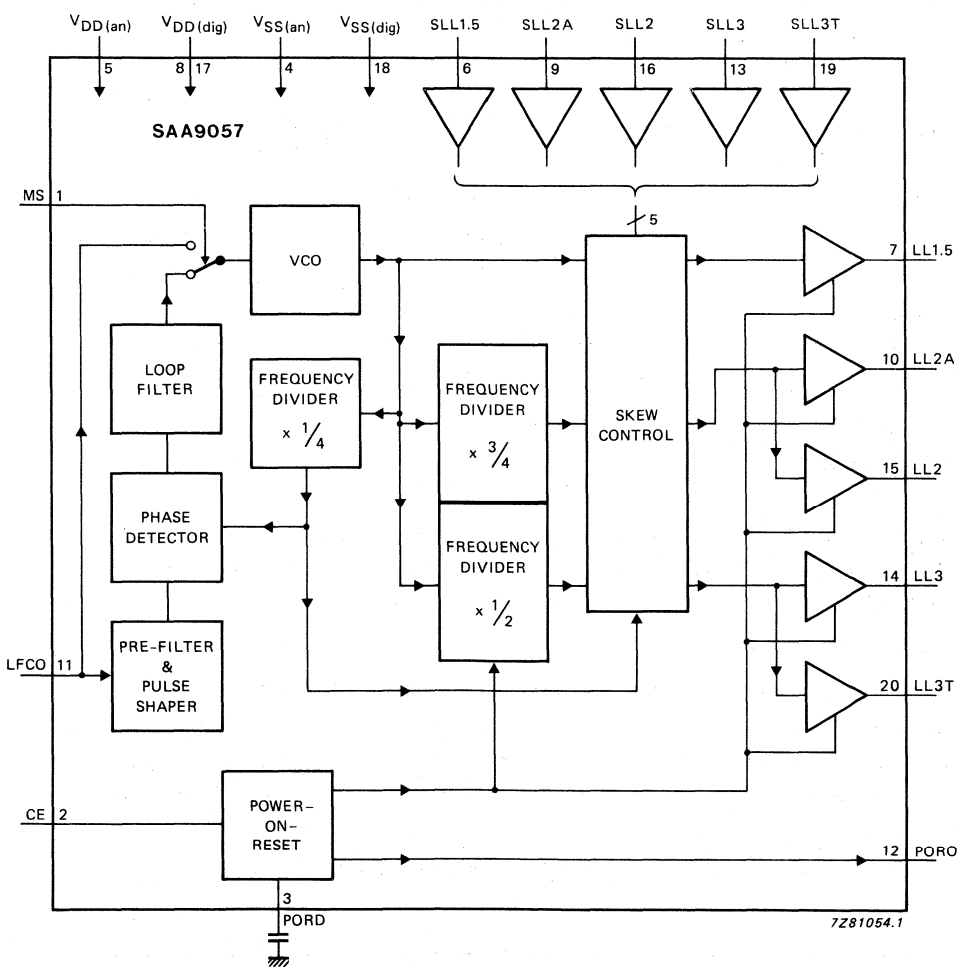


Fig. 1 Block diagram.

PACKAGE OUTLINE

20-lead DIL; plastic (SOT-146).

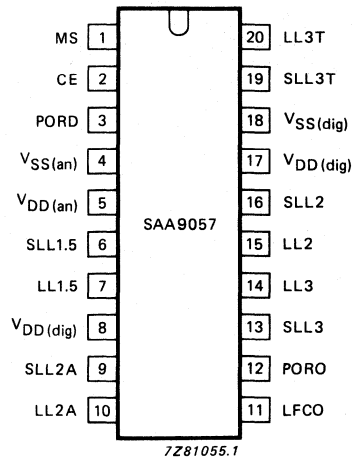


Fig. 2 Pinning diagram.

PINNING

1	MS	mode select input. MS = LOW for normal operation in which the CGC generates clocks with reference to LFCO MS = HIGH disables the PLL and connects the LFCO input to the control input of the VCO, providing VCO, frequency divider and buffer facilities only
2	CE	chip enable. CE = HIGH enables the VCO and the output buffers; CE = LOW sets the buffers to high impedance off-state and inhibits VCO oscillation
3	PORD	power-on-reset delay. Duration of delay is determined by an external capacitor at this pin
4	$V_{SS(an)}$	ground (0 V) for analogue circuits
5	$V_{DD(an)}$	positive supply voltage (+ 5 V) for analogue circuits
6	SLL1.5	sensing input for LL1.5 skew control. Pin 6 input amplifier can handle low-level sinusoidal clock waveforms. Strap to pin 7 when not using external clock drivers or low-level clocks
7	LL1.5	27 MHz line-locked clock. The waveform is rectangular and the duty factor is 50%
8	$V_{DD(dig)}$	positive supply voltage (+ 5 V) for digital circuits (no internal connection to pin 17)
9	SLL2A	sensing input for LL2A skew control. Pin 9 input amplifier can handle low-level sinusoidal clock waveforms. Strap to pin 10 when not using external clock drivers or low-level clocks
10	LL2A	20,25 MHz line-locked clock. The waveform is rectangular and the duty factor is 50%
11	LFCO	line frequency control input to which all internal clocks are referred. The waveform is triangular with 4-bit quantization and 24,576 MHz sample rate

12	PORO b	power-on-reset output. Goes LOW following power-on or power fail. Remains LOW for a period determined by external capacitor at pin 3. It is also activated by a slow or fast fall of supply voltage to below operating level. PORO can be used as a reset signal for the whole digital tv system.
13	SLL3	sensing input for LL3 skew control. Pin 13 input amplifier can handle low-level sinusoidal waveforms. Strap to pin 14 when not using external clock drivers or low-level clocks
14	LL3	13,5 MHz line-locked clock. The waveform is rectangular and the duty factor is 50%
15	LL2	20,25 MHz line-locked clock. The waveform is rectangular and the duty factor is 50%
16	SLL2	sensing input for LL2 skew control. Pin 16 input amplifier can handle low-level sinusoidal waveforms. Strap to pin 15 when not using external clock drivers or low-level clocks
17	$V_{DD(dig)}$	positive supply voltage (+ 5 V) for digital circuits
18	$V_{SS(dig)}$	ground (0 V) for digital circuits (no internal connection to pin 8)
19	SLL3T	sensing input for LL3T skew control. Pin 19 input amplifier can handle low-level sinusoidal waveforms. Strap to pin 20 when not using external clock drivers or low-level clocks
20	LL3T	13,5 MHz line-locked clock. The waveform is rectangular and the duty factor is 50%

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The SAA9057 provides all the clock waveforms required in a typical digital tv system. This can comprise an analogue-to-digital converter (ADC, PNA7509), a sample-rate converter (SRC, SAA9058), a digital multi-standard decoder (DMSD, SAA9050), a digital deflection controller (DDC, SAA9060) with single or double line-frequency, plus extensions to add to the features available in the system.

The frequency of the reference input LFCO (a 6,75 MHz triangular waveform from the DMSD) is multiplied to 27 MHz by the PLL. All clock outputs are derived from this by frequency dividers with ratios as shown in Figs 1 and 3.

Each clock output is skew-controlled so that a temperature and load-independent phase relationship is maintained between the clock outputs.

The LL1.5, LL2 and LL3 outputs are rectangular waveforms with a 50% duty factor.

The clock outputs are inhibited from power-on until the circuit has stabilized. The inhibit time is determined by the capacitor at pin 3. A power-fail detector is combined with the inhibit circuit so that the DDC is protected from unspecified clock frequencies that could occur in the event of a power failure. The PORO output (pin 12) indicates that the power supply is stable and can be used to drive other power-on-reset circuits.

The phase detector and loop filter are disabled by the mode select input at pin 1 which internally connects the VCO control input to the LFCO input at pin 11. The circuit now operates as an oscillator followed by stages of frequency division, uses for which may be found in analogue environments of feature tv applications.

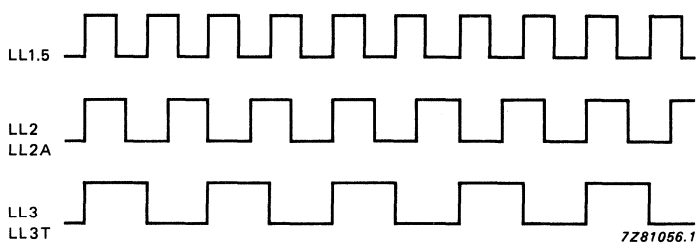


Fig. 3 Relationship between clock outputs.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage range	$V_{DD(dig)}$	−0,5 to + 0,7	V
	$V_{DD(an)}$	−0,5 to + 7,0	V
Input voltage at any pin with respect to ground	V_I	−0,5 to + 7,0	V
Input/output current	I_I, I_O	max. *	mA
Total power dissipation	P_{tot}	*	W
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Storage temperature range	T_{stg}	−65 to −150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	*	*	mA
Input LFCO (triangular waveform; resolution = 4 bits)					
Frequency	f_{LFCO}	6,0	6,75	7,4	MHz
Amplitude (peak-to-peak value)	$V_{LFCO(p-p)}$	1,0	2,0	V_{DD}	V
PLL					
Natural frequency	f_n	55	80	115	kHz
Damping coefficient	D	0,5	0,7	1,0	
Jitter		–	–	*	ns
Clock outputs					
Rise time (all clocks)	t_r	–	–	3	ns
Fall time (all clocks)	t_f	–	–	3	ns
Skew (all clocks)	t_{skew}	−2	–	+ 2	ns
Output voltage HIGH (except LL2A)	V_{OH}	2,8	–	V_{DD}	V
Output voltage HIGH (LL2A only)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (all clocks)	V_{OL}	0	–	0,4	V
Duty factor	δ	45	50	55	%

* Values not yet available.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Load capacitance:					
LL1.5	C_L	–	–	30	pF
LL2	C_L	–	–	50	pF
LL2A	C_L	–	–	20	pF
LL3T	C_L	–	–	20	pF
LL3	C_L	–	–	50	pF

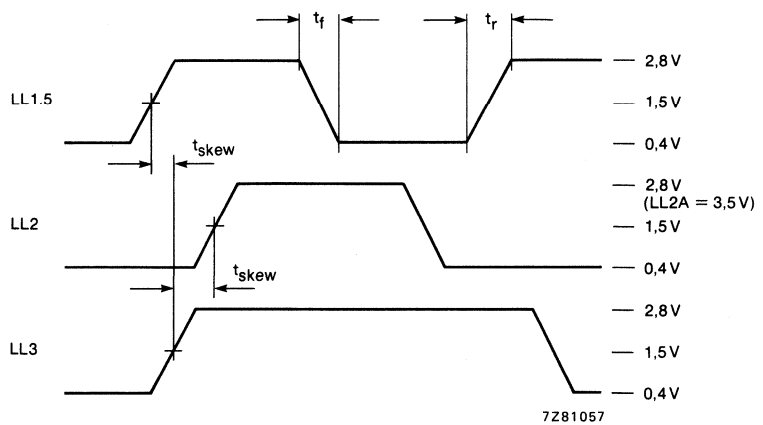


Fig. 4 Timing diagram.

SAMPLE-RATE CONVERTER

GENERAL DESCRIPTION

The SAA9058 sample-rate converter (SRC) is for use in digital tv receiver applications. It converts the sampling rate of digital signals by a factor of 2/3, e.g. from 20,25 to 13,5 MHz, using a phase-linear, finite impulse response (FIR) filter with time-varying coefficients. Only two clocks are required, the data format is two's complement and the word length at both input and output is seven bits.

The FIR filter creates a filter-algorithm to interpolate digitized composite video signals (DCVBS) into a slower sample rate that is suitable for video decoding. The circuit gives low attenuation of colour subcarrier, gives high rejection of aliasing components and has unity d.c. gain.

It is intended for use with the 7-bit digital-to-analogue converter PNA7507 or PNA7509 and the digital multistandard decoder SAA9050, with DCVBS in PAL, NTSC or SECAM. Other applications are digital anti-aliasing filtering, rejection of harmonics caused by analogue-to-digital conversion and data reduction.

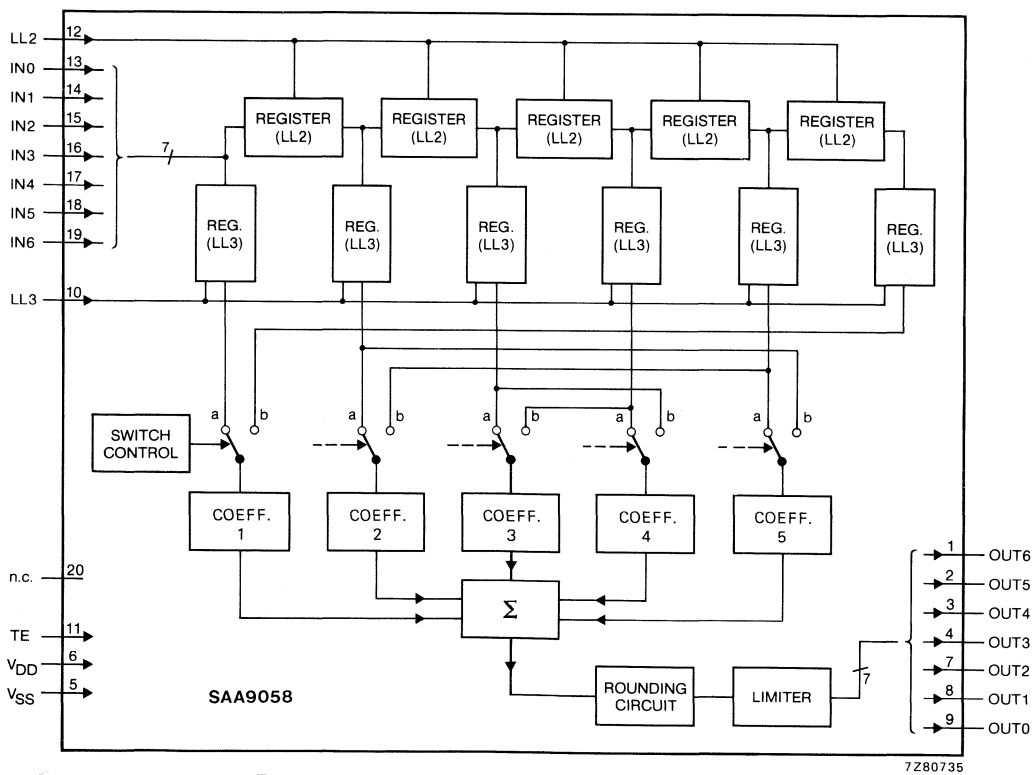


Fig. 1 Block diagram (see Fig. 3 for switch timing).

PACKAGE OUTLINE

20-lead DIL; plastic (SOT-146).

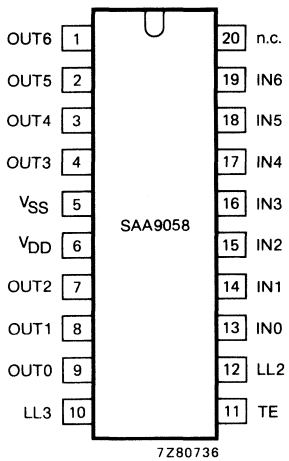


Fig. 2 Pinning diagram.

PINNING

1	OUT6	output data
2	OUT5	
3	OUT4	
4	OUT3	
5	V_{SS}	ground (0 V)
6	V_{DD}	positive supply voltage (+ 5 V)
7	OUT2	output data
8	OUT1	
9	OUT0	
10	LL3	output clock
11	TE	production test input; LOW for all applications
12	LL2	input clock
13	IN0	input data
14	IN1	
15	IN2	
16	IN3	
17	IN4	
18	IN5	
19	IN6	
20	n.c.	not connected

OPERATION

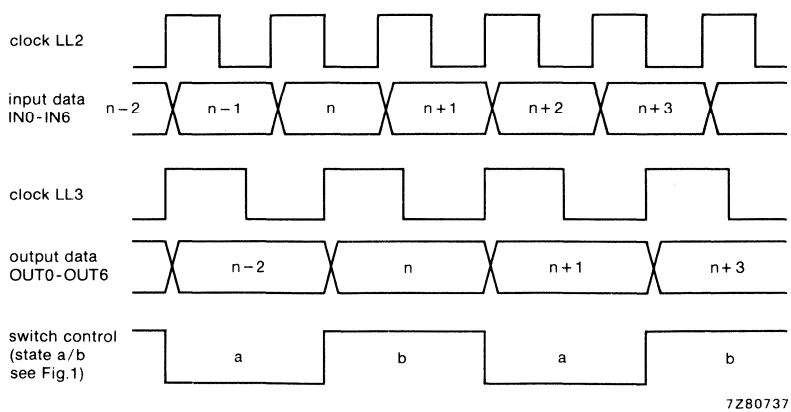


Fig. 3 Relationship of inputs to outputs.

Frequency response

The virtual frequency response in the 2 x LL2 (40,5 MHz) domain is interpreted as the characteristic of the interpolation filter directly before conversion to the LL3 (13,5 MHz) sample rate and the spectral components beyond LL3/2 are aliased into the baseband.

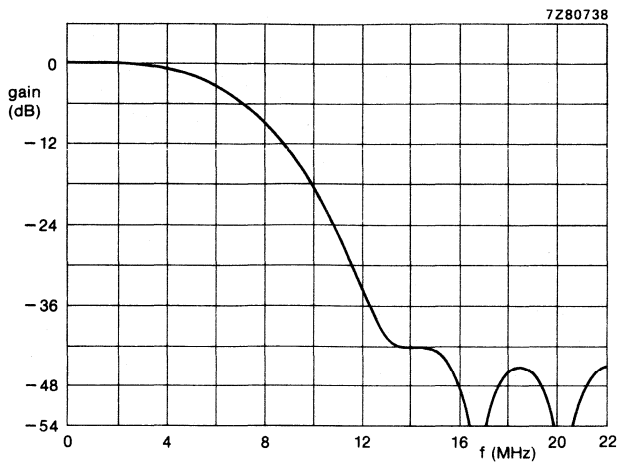


Fig. 4 Frequency response.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to + 7 V
Input voltage range	V_I	−0,5 to + 7 V
Output voltage range to $I_{O\,max}$ = 20 mA	V_O	−0,5 to + 7 V
Maximum power dissipation	P_{tot}	0,5 W
Operating ambient temperature range	T_{amb}	0 to + 70 °C
Storage temperature range	T_{stg}	−65 to + 150 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range	V_{DD}	4,5	5,0	5,5	V
Supply current at V_{DD} = 5 V; f_{LL2} = 20,25 MHz; f_{LL3} = 13,5 MHz	I_{DD}	–	50	–	mA
Inputs					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH (except LL2, LL3)	V_{IH}	2,0	–	V_{DD}	V
Input voltage HIGH (LL2, LL3)	V_{IH}	2,4	–	V_{DD}	V
Input leakage current	I_I	–	–	10	μA
Input capacitance (LL2)	C_I	–	–	10	pF
Input capacitance (LL3)	C_I	–	–	10	pF
Input capacitance (IN0 to IN6)	C_I	–	–	5	pF
Outputs					
Output voltage HIGH at I_{OH} = −0,5 mA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 2,0 mA	V_{OL}	0	–	0,4	V
Timing (Fig. 5)					
LL2 cycle time	t_{C2}	47	–	60	ns
LL2 HIGH time	t_{C2H}	20	–	–	ns
LL2 LOW time	t_{C2L}	20	–	–	ns
LL2 rise and fall time	t_r, t_f	–	–	3	ns
LL3 cycle time	t_{C3}	69	–	80	ns
LL3 HIGH time	t_{C3H}	30	–	–	ns
LL3 LOW time	t_{C3L}	30	–	–	ns
LL3 rise and fall time	t_r, t_f	–	–	3	ns
Skew time	t_{skew}	−2	–	+ 2	ns
Input data set-up time	t_{SU}	12	–	–	ns
Input data hold time	t_{HD}	3	–	–	ns
Output data load capacitance	C_L	7,5	–	15	pF
Output data hold time	t_{OH}	3	–	–	ns
Output data delay time	t_{OD}	–	–	33	ns

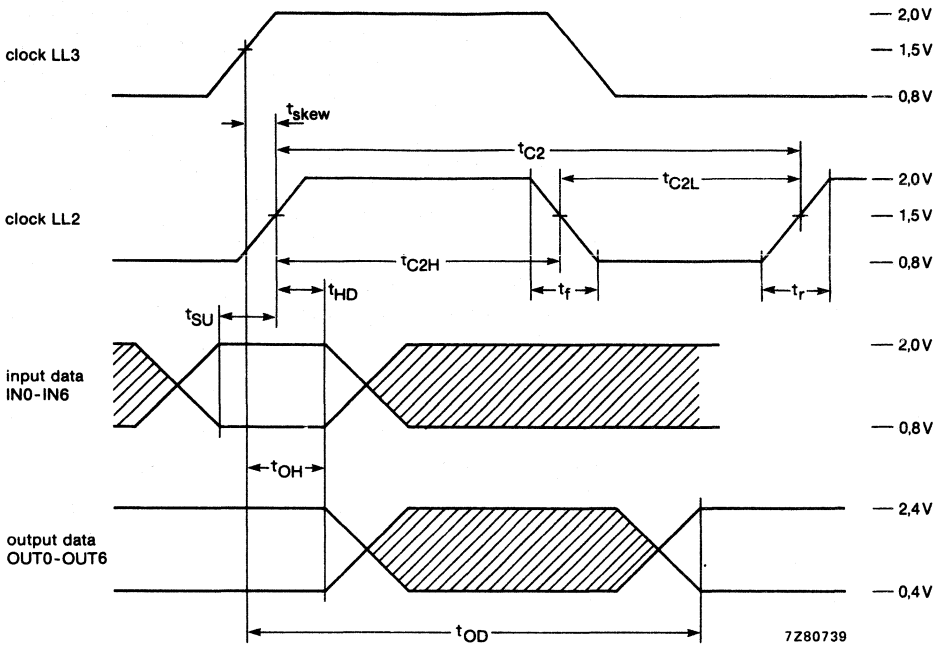


Fig. 5 Timing diagram.

DEVELOPMENT DATA

SENSITIVE 1 GHz DIVIDER-BY-64

This silicon monolithic integrated circuit is a prescaler in current-mode logic. It contains an amplifier, a divide-by-64 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a television tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C. It features a high sensitivity and low harmonic contents of the output signal. The difference between SAB1164 and SAB1165 is the output resistance (see Fig. 7)

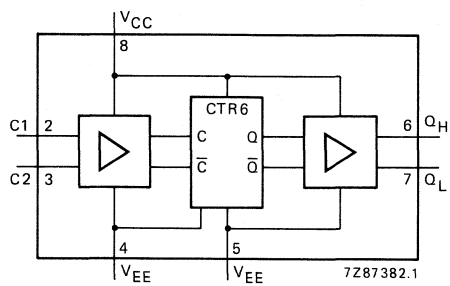


Fig. 1 Block diagram. CTR6 = 6 binary dividers = (÷ 64).

QUICK REFERENCE DATA

Supply voltage (pin 8)	V_{CC}	5 ± 10%	V
Input frequency range (pins 2 and 3)	f_i	70 to 1000	MHz
Output voltage swing (pins 6 and 7)	$V_{o(p-p)}$	typ. 1	V
Supply current; unloaded (pin 8)	I_{CC}	typ. 42	mA
Operating ambient temperature	T_{amb}	0 to + 70	°C

PACKAGE OUTLINES

SAB1164P: 8-lead DIL; plastic (SOT-97A).
SAB1165P: 8-lead DIL; plastic (SOT-97A).

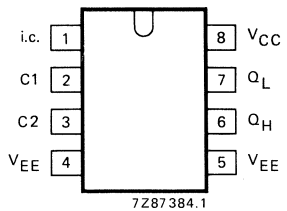


Fig. 2 Pinning diagram.

PINNING

V_{CC}	positive supply
V_{EE}	0 V; ground
C_1, C_2	differential inputs
Q_H, Q_L	complementary outputs
i.c.	internally connected

FUNCTIONAL DESCRIPTION

The circuit contains an amplifier, a divide-by-64 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a TV tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C.

The inputs are differential and are internally biased to permit capacitive coupling. For asymmetrical drive the unused input should be connected to ground via a capacitor.

The first divider stage will oscillate in the absence of an input signal; an input signal within the specified range will suppress this oscillation.

The output differential stage has two complementary outputs. The output voltage edges are slowed down internally to reduce the harmonic contents of the signal.

Wide, low-impedance ground connections and a short capacitive bypass from the V_{CC} pin to ground are recommended.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	7 V
Input voltage	V_i		0 to V_{CC} V
Storage temperature	T_{stg}		−55 to + 125 °C
Junction temperature	T_j	max.	125 °C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c\text{-}a}$	=	120 K/W

D.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V; T_{amb} = 25 °C unless otherwise specified.

The circuit has been designed to meet the d.c. specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

Output voltage				
HIGH level	V_{OH}	max.	V_{CC}	V
LOW level	V_{OL}	max.	V_{CC}−0,8	V
Supply current	I_{CC}	typ.	42	mA
		max.	50	mA

A.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V ± 10%; T_{amb} = 0 to + 70 °C.

		min.	typ.	max.	unit
Input voltage r.m.s. value (see Fig. 4)					
input frequency 70 MHz	$V_{i(rms)}$	–	9	17,5	mV
150 MHz		–	4	10	mV
300 MHz		–	3	10	mV
500 MHz		–	3	10	mV
900 MHz		–	2	10	mV
1 GHz		–	3	17,5	mV
Input overload voltage r.m.s. value					
input frequency range 70 MHz up to 1 GHz	$V_{i(rms)}$	–	–	200	mV
Output voltage swing	$V_{o(p-p)}$	0,8	1	–	V
Output resistance					
SAB1164	R_o	–	1	–	kΩ
SAB1165	R_o	–	0,5	–	kΩ
Output unbalance	ΔV_o	–	–	0,1	V
Output rise time*					
f_i = 1 GHz	t_{TLH}	–	25	–	ns
Output fall time*					
f_i = 1 GHz	t_{THL}	–	25	–	ns

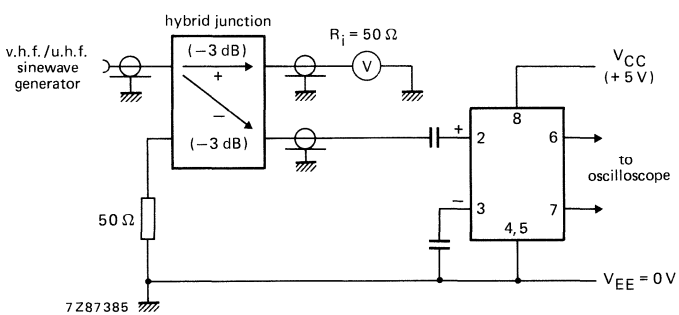


Fig. 3 Test circuit for defining input voltage.

– Cables must be 50 Ω coaxial.
– The capacitors are leadless ceramic (multilayer capacitors) of 10 nF.
– All connections to the device and to the meter must be kept short and of approximately equal lengths.
– Hybrid junction is ANZAC H-183-4 or similar.

* Between 10% and 90% of observed waveform.

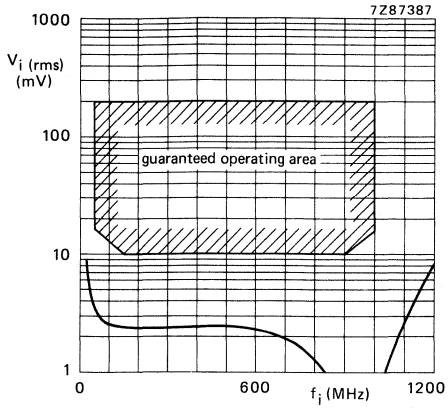


Fig. 4 Typical sensitivity curve under nominal conditions.

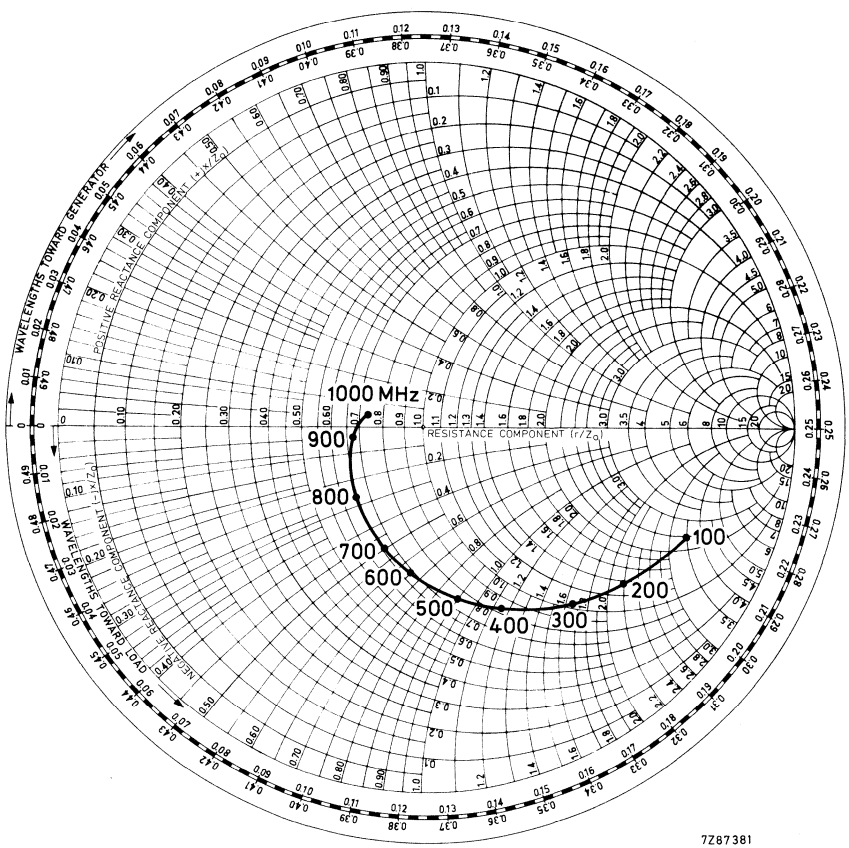


Fig. 5 Smith chart of typical input impedance.
$V_{i(rms)}$ = 25 mV; V_{CC} = 5 V; reference value = 50 Ω.

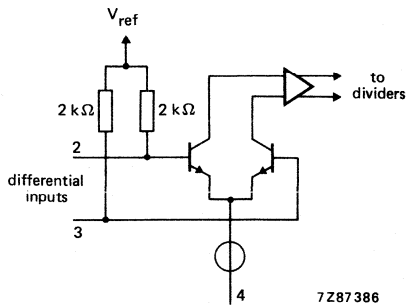


Fig. 6 Input stage.

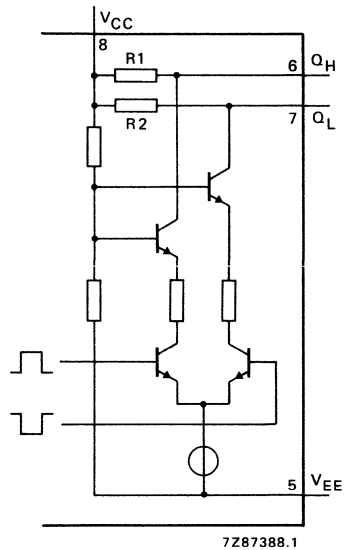


Fig. 7 Output stage. V_{CC} = 5 V.
SAB1164: R1 = R2 = 1 kΩ; I = 1 mA
SAB1165: R1 = R2 = 0,5 kΩ; I = 2 mA.

APPLICATION INFORMATION

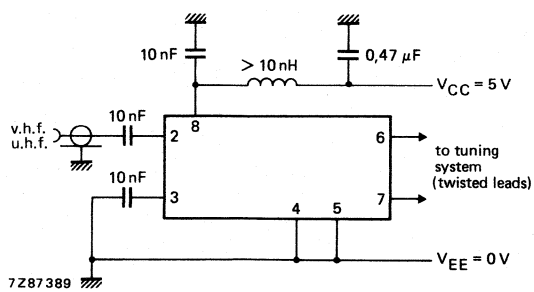


Fig. 8 Circuit diagram. Application in a television tuning system.
The output peak-to-peak voltage is about 1 V.

SENSITIVE 1 GHz DIVIDER-BY-256

This silicon monolithic integrated circuit is a prescaler in current-mode logic. It contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a television tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C. It features a high sensitivity and low harmonic contents of the output signal.

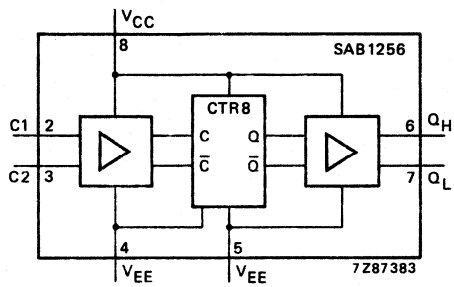


Fig. 1 Block diagram. CTR8 = 8 binary dividers = (÷ 256).

QUICK REFERENCE DATA

Supply voltage (pin 8)	V_{CC}	5 ± 10%	V
Input frequency range (pins 2 and 3)	f_i	70 to 1000	MHz
Output voltage swing (pins 6 and 7)	$V_{o(p-p)}$	typ. 1	V
Supply current, unloaded (pin 8)	I_{CC}	typ. 47	mA
Operating ambient temperature	T_{amb}	0 to + 70	°C

PACKAGE OUTLINE

SAB1256P: 8-lead DIL; plastic (SOT-97A).

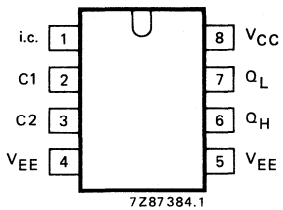


Fig. 2 Pinning diagram.

PINNING

V_{CC}	positive supply
V_{EE}	0 V; ground
C_1, C_2	differential inputs
Q_H, Q_L	complementary outputs
i.c.	internally connected

FUNCTIONAL DESCRIPTION

The circuit contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a TV tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C.

The inputs are differential and are internally biased to permit capacitive coupling. For asymmetrical drive the unused input should be connected to ground via a capacitor.

The first divider stage will oscillate in the absence of an input signal; an input signal within the specified range will suppress this oscillation.

The output differential stage has two complementary outputs. The output voltage edges are slowed down internally to reduce the harmonic contents of the signal.

Wide, low-impedance ground connections and a short capacitive bypass from the V_{CC} pin to ground are recommended.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	7 V
Input voltage	V_i	0 to V_{CC}	V
Storage temperature	T_{stg}	−55 to + 125	°C
Junction temperature	T_j	max. 125	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c\text{-}a}$	=	120 K/W

D.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V; T_{amb} = 25 °C unless otherwise specified.

The circuit has been designed to meet the d.c. specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

Output voltage				
HIGH level	V_{OH}	max.	V_{CC}	V
LOW level	V_{OL}	max.	V_{CC}–0,8	V
Supply current	I_{CC}	typ.	47	mA
		max.	55	mA

A.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V ± 10%; T_{amb} = 0 to + 70 °C.

		min.	typ.	max.	unit
Input voltage r.m.s. value (see Fig. 4)					
input frequency 70 MHz	$V_{i(rms)}$	–	9	17,5	mV
150 MHz		–	4	10	mV
300 MHz		–	3	10	mV
500 MHz		–	3	10	mV
900 MHz		–	2	10	mV
1 GHz		–	3	17,5	mV
Input overload voltage r.m.s. value					
input frequency range 70 MHz to 1 GHz	$V_{i(rms)}$	–	–	200	mV
Output voltage swing	$V_{o(p-p)}$	0,8	1	–	V
Output resistance	R_o	–	1	–	kΩ
Output unbalance	ΔV_o	–	–	0,1	V
Output rise time*					
f_i = 1 GHz	t_{TLH}	–	40	–	ns
Output fall time					
f_i = 1 GHz	t_{THL}	–	40	–	ns

* Between 10% and 90% of observed waveform.

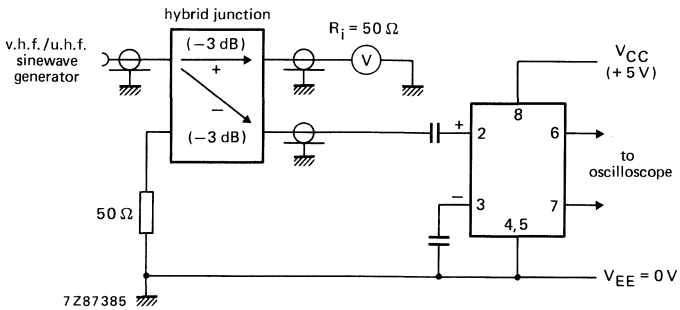


Fig. 3 Test circuit for defining input voltage.

- Cables must be 50 Ω coaxial.
- The capacitors are leadless ceramic (multilayer capacitors) of 10 nF.
- All connections to the device and to the meter must be kept short and of approximately equal lengths.
- Hybrid junction is ANZAC H-183-4 or similar.

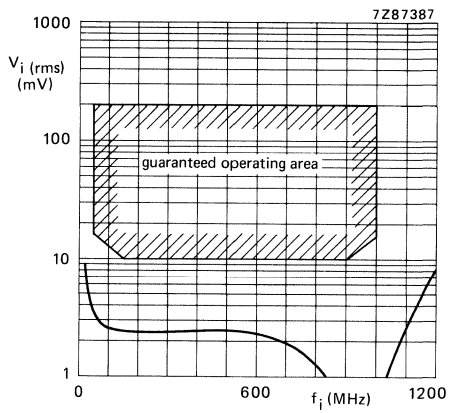


Fig. 4 Typical sensitivity curve under nominal conditions.

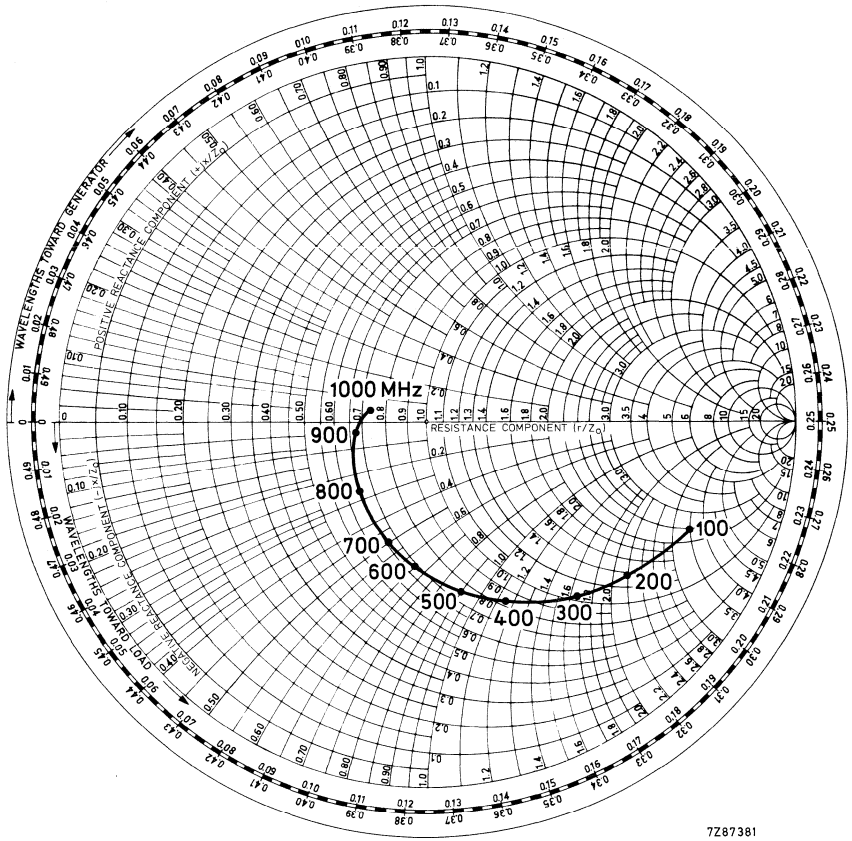


Fig. 5 Smith chart of typical input impedance.
$V_{i(rms)}$ = 25 mV; V_{CC} = 5 V; reference value = 50 Ω.

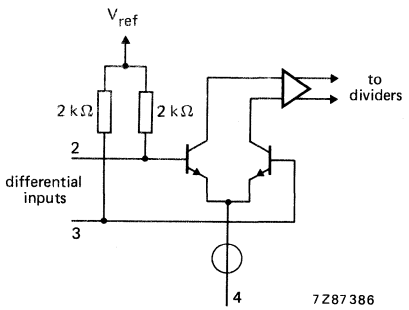


Fig. 6 Input stage.

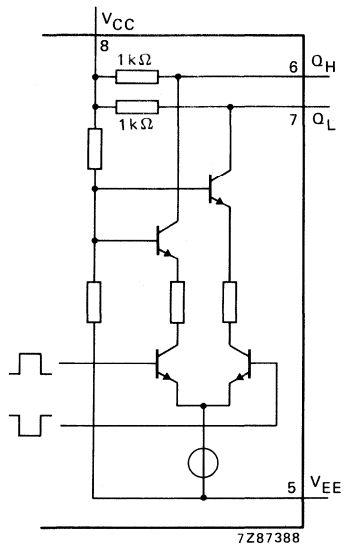


Fig. 7 Output stage.
V_{CC} = 5 V; I = 1 mA.

APPLICATION INFORMATION

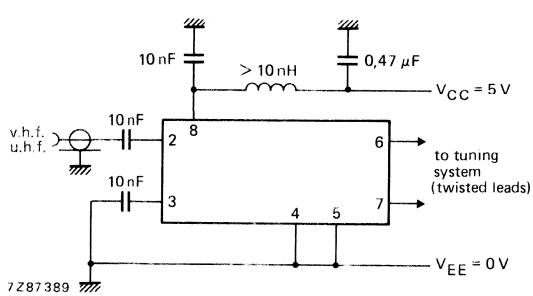


Fig. 8 Circuit diagram.
Application in a television tuning system. The output peak-to-peak voltage is about 1 V.

6-FUNCTION ANALOGUE MEMORY; MICROCOMPUTER CONTROLLED

The SAB3013 is a MOS N-channel integrated circuit which provides 6 analogue memories controlled by a microcomputer.

Features

- 6-function analogue memory; D/A converter with 6-bit resolution.
- The output of the analogue values is pulse-width modulated with adjustable repetition rate (max. 21,8 kHz).
- Microcomputer-adapted asynchronous serial interface for data input (CBUS).
- Parallel operation of up to four SAB3013 circuits is possible.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	typ.	5 V
Operating ambient temperature range	T_{amb}	0 to	+70 °C
Clock frequency	f_{CLK}	<	1,4 MHz
Supply current; V_{DD} = 5 V; I_O = 0; T_{amb} = 25 °C	I_{DD}	typ.	15 mA

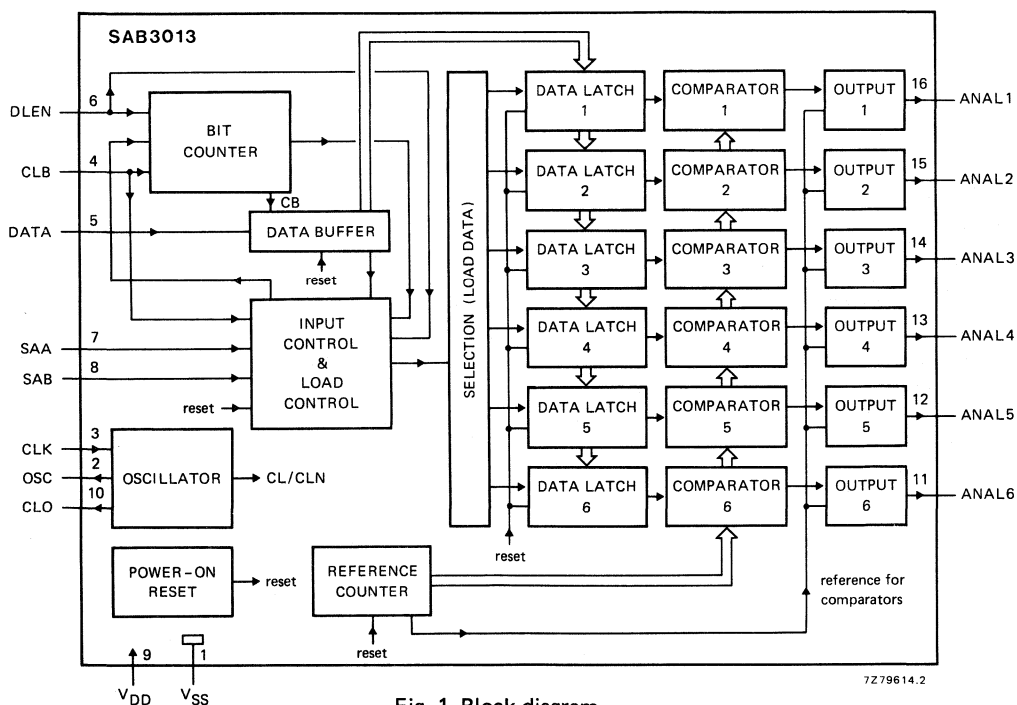


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

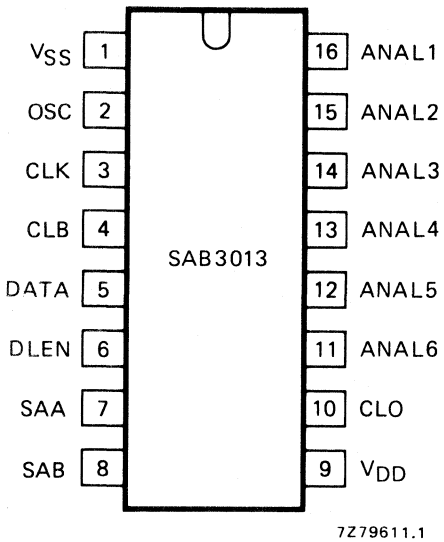


Fig. 2 Pinning diagram.

PINNING

1	V_{SS}	ground (0 V)	
9	V_{DD}	positive supply	
4	CLB	asynchronous clock pulse	CBUS
5	DATA	data input	CBUS
6	DLEN	data line enable input	CBUS
7	SAA	address inputs	
8	SAB	address inputs	
2	OSC	oscillator output	
3	CLK	oscillator input (Schmitt-trigger)	
16	ANAL1	analogue outputs	
15	ANAL2	analogue outputs	
14	ANAL3	analogue outputs	
13	ANAL4	analogue outputs	
12	ANAL5	analogue outputs	
11	ANAL6	analogue outputs	
10	CLO	buffered oscillator output	

GENERAL DESCRIPTION

The SAB3013 is designed to deliver analogue values in microcomputer-controlled television receivers and radio receivers. The circuit comprises an analogue memory and D/A converter for 6 analogue functions with a 6-bit resolution for each. The information for the analogue memory is transfered by the microcomputer via an asynchronous serial data bus.

The SAB3013 accomplishes a word format recognition, so it is able to operate one common data bus together with circuits having different word formats.

The data word of the microcomputer used for the SAB3013 consists of information for addressing the appropriate SAB3013 circuit (2-bits), for addressing the analogue memories concerned (3-bits) and processing of the wanted analogue value (6-bits). The address of the circuit is externally programmable via two inputs. It is possible to address up to four SAB3013 circuits via one common bus.

The built-in oscillator can be used for a frequency between 30 kHz and 1,4 MHz. The analogue values are generated as a pulse pattern with a repetition rate of $f_{CLK}/64$ (max. 21,8 kHz at f_{CLK} = 1,4 MHz), and the analogue values are determined by the ratio of the HIGH-time and the cycle time. A d.c. voltage proportional to the analogue value is obtained by means of an external integration network (low-pass filter).

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance to the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 7,5		V
Input voltage range	V_I	−0,3 to + 15		V
Input current	$\pm I_I$	max.	100	μA
Output voltage (open drain outputs)	V_O	V_{SS} to 15		V
Output current (open drain/push-pull outputs)	$\pm I_O$	max.	10	mA
Power dissipation per output	P_O	max.	25	mW
Total power dissipation per package	P_{tot}	max.	250	mW
Operating ambient temperature range	T_{amb}	0 to + 70		°C
Storage temperature range	T_{stg}	−20 to + 125		°C

CHARACTERISTICS

V_{SS} = 0; T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

	symbol	min.	typ.	max.	conditions
Supply voltage	V_{DD}	4,5	5	5,5 V	
Supply current	I_{DD}	–	–	35 mA	V_{DD} = 5,5 V
Inputs DATA, CLB, DLEN, SAA, SAB					
Input voltage LOW	V_{IL}	0	–	12 V	
Input voltage HIGH	V_{IH}	2,0	–	12 V	
Input leakage current	I_{IR}	–	–	1 μA	V_I = –0,3 to + 12 V
Outputs ANAL1 to ANAL6 (open drain)					
Output voltage LOW	V_{OL}	–	–	0,7 V	I_O = 6 mA
Output leakage current	I_{OR}	–	–	20 μA	V_{OH} = 15 V *
Load capacitance	C_L	–	–	1000 pF	
Input CLK					
Input voltage LOW	V_{IL}	–0,3	–	0,8 V	
Input voltage HIGH	V_{IH}	3,5	–	12 V	
Input leakage current	I_{IR}	–	–	1 μA	V_I = –0,3 to 12 V
Pulse duration HIGH	t_{WH}	355	–	– ns	
Pulse duration LOW	t_{WL}	355	–	– ns	
Output CLO					
Output voltage LOW	V_{OL}	–	–	0,8 V	I_O 500 μA
Output voltage HIGH	V_{OH}	3,5	–	– V	$-I_O$ = 100 μA
Inputs DATA, CLB					
Pulse duration HIGH	t_{WH}	450	–	– ns	see Fig. 3
Pulse duration LOW	t_{WL}	450	–	– ns	see Fig. 3
Input frequency CLB	f_{CLB}	0	–	1 MHz	
Internal oscillator CLK/OSC					
External resistor	R	27	–	1000 kΩ	
External capacitor	C	27	–	1000 pF	
Clock frequency	f_{CLK}	0,7	1,0	1,4 MHz	R = 27 kΩ; C = 27 pF
Frequency for external oscillator	f_{CLK}	0,03	–	1,4 MHz	

* For correct operation: V_{OHmin} = 3 V.

CHARACTERISTICS (continued)

V_{SS} = 0; T_{amb} = 0 to +70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Timing (see Fig. 3)						
Data set-up time DATA → CLB	t_{SUDA}	800	–	–	ns	measured with a voltage swing of min. $V_{IH}-V_{IL}$
Data hold time DATA → CLB	t_{HDDA}	300	–	–	ns	
Enable set-up time DLEN → CLB	t_{SUEN}	400	–	–	ns	
Disable set-up time CLB → DLEN	t_{SUDI}	400	–	–	ns	
Set-up time DLEN → CLB (load pulse)	t_{SULD}	1000	–	–	ns	

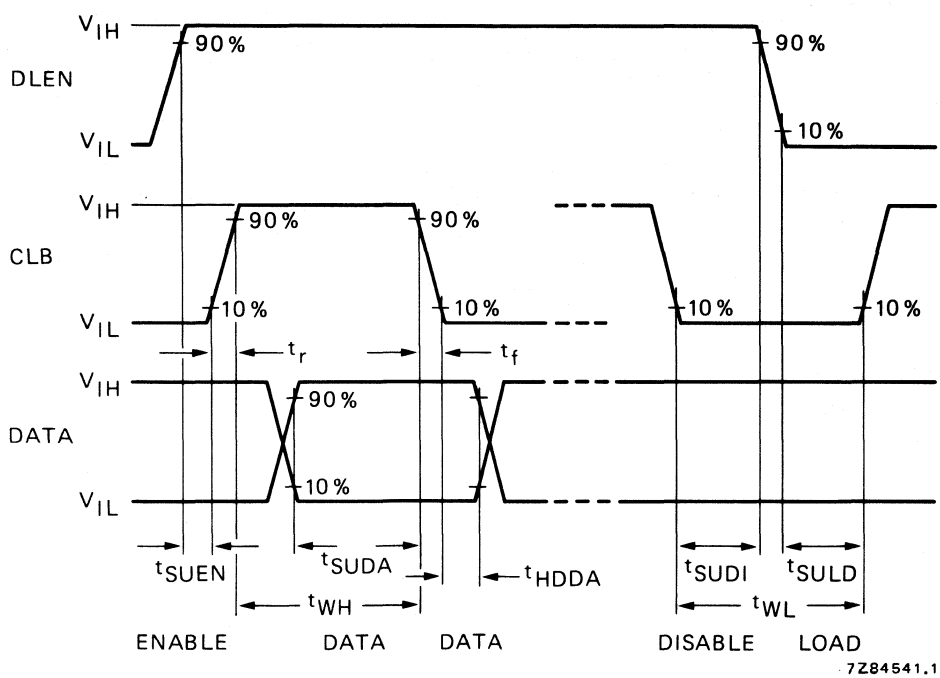


Fig. 3 CBUS timing.

OPERATION DESCRIPTION

The data input is achieved serially via the inputs DATA, DLEN and CLB. Clock pulses have to be applied at input CLB for data processing at input DATA. Data processing is only possible when DLEN = HIGH. The data from the data buffer is loaded directly into the output latch on receipt of a load pulse at input CLB (DLEN = LOW), provided the following conditions are met:

- 12 clock pulses must be received at input CLB (word format control) during transmission (DLEN = HIGH).
- The start-bit must be LOW.
- The system address bits must be A = SAA and B = SAB.
- The analogue address must be valid.

The data word for the SAB3013 consists of the following bits (see Fig. 4):

1 start-bit
2 system address bits (A and B)
3 address bits for selection of the required analogue memory
6 data bits for processing the analogue value

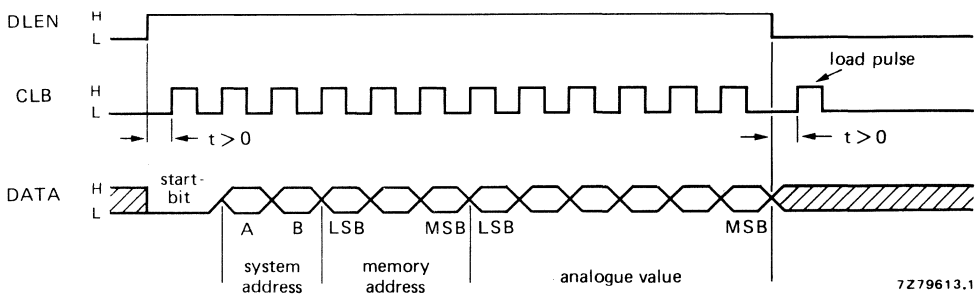


Fig. 4 Waveforms showing a CBUS transmission.

ADDRESS inputs (SAA, SAB)

The address of the SAB3013 is programmed at the inputs SAA and SAB. These inputs must be defined and not left open-circuit.

Reset

The circuit generates internally a reset-cycle with a duration of one clock cycle after switching on the supply. If a spike on the supply is likely to destroy data, a reset signal will be generated. All analogue memories are set to 50% (analogue value 32/64) after the reset cycle. The supply voltage rise dV_{DD}/dt must be max. 0,5 V/μs and min. 0,2 V/μs.

Oscillator inputs (CLK, OSC)

The oscillator frequency is determined by the external circuitry connected to the terminals CLK and OSC as shown in Fig. 5. Instead of this circuitry an externally generated oscillator signal can be connected to input CLK.

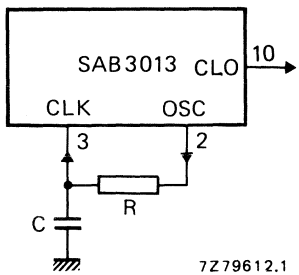


Fig. 5 Application advice for the oscillator.

At output CLO a buffered oscillator signal is available for control of other circuits.

For f_{CLK} = 0,7 to 1,4 MHz;
R = 27 kΩ; C = 27 pF.

Analogue outputs (ANAL1 to ANAL6)

The analogue values are generated as a pulse pattern with a repetition rate of $f_{CLK}/64$ at the outputs ANAL1 to ANAL6. The analogue value is determined by the ratio of the HIGH-time and the cycle time (values between 1/64 and 64/64 can be obtained).

Table 1 Addressing of the analogue data registers

R_A LSB	R_B	R_C MSB	addressing
0	0	0	not valid
1	0	0	ANAL1
0	1	0	ANAL2
1	1	0	ANAL3
0	0	1	ANAL4
1	0	1	ANAL5
0	1	1	ANAL6
1	1	1	not valid

Table 2 Correlation of analogue value to analogue output signal

analogue value	binary input data LSB ... MSB	duty cycle 'low'	duty cycle 'high'
lowest value	0 0 0 0 0 0	63/64	1/64
	1 0 0 0 0 0	62/64	2/64
power-on reset value	1 1 1 1 1 0	32/64	32/64
highest value	0 1 1 1 1 1	1/64	63/64
	1 1 1 1 1 1	0	64/64

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3035 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 8 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 8 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 16)	V_{P1}	typ.	12 V
(pin 22)	V_{P2}	typ.	13 V
(pin 17)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 16)	I_{P1}	typ.	32 mA
(pin 22)	I_{P2}	typ.	0,1 mA
(pin 17)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	400 mW
Operating ambient temperature range	T_{amb}	−20 to +70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

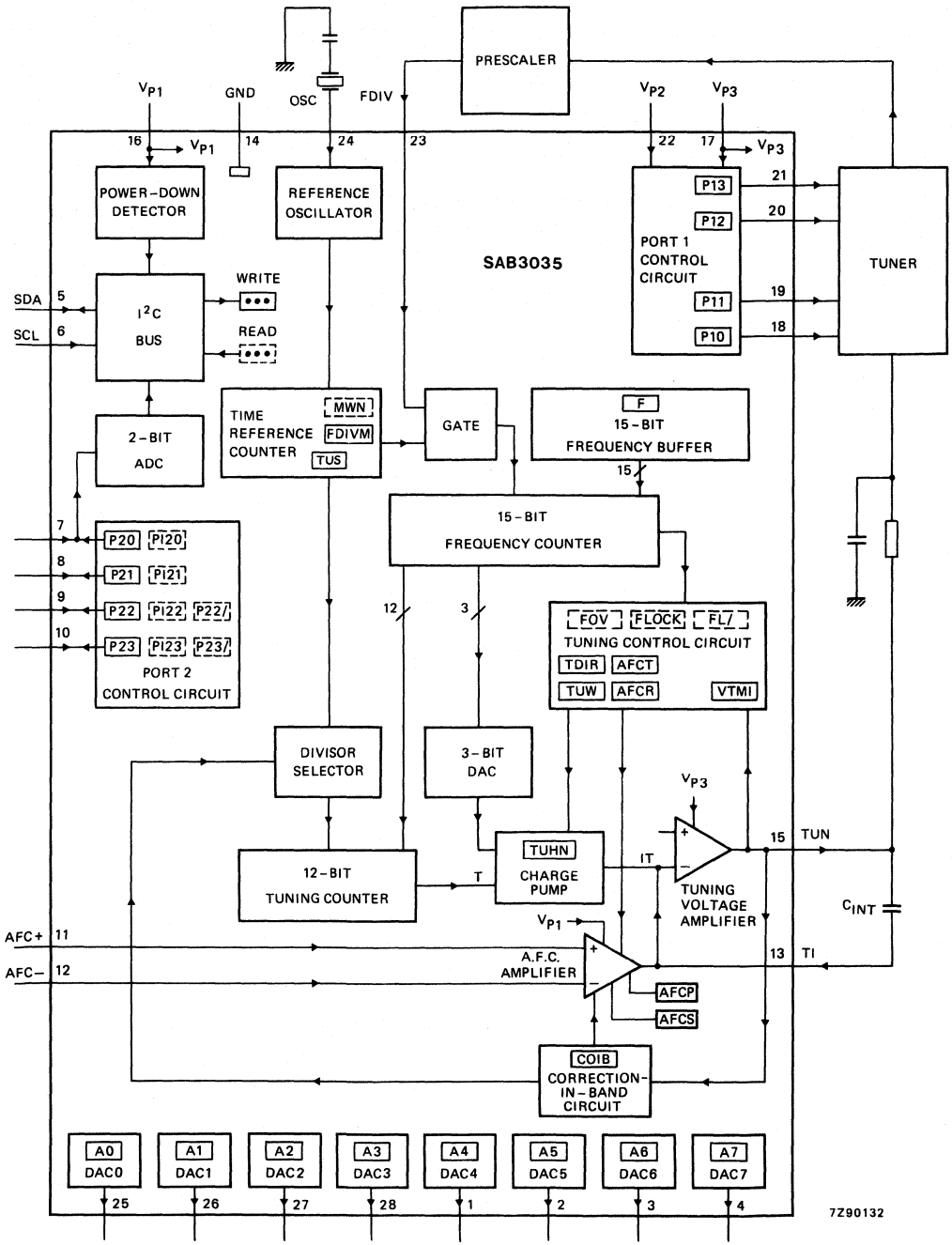


Fig. 1 Block diagram.

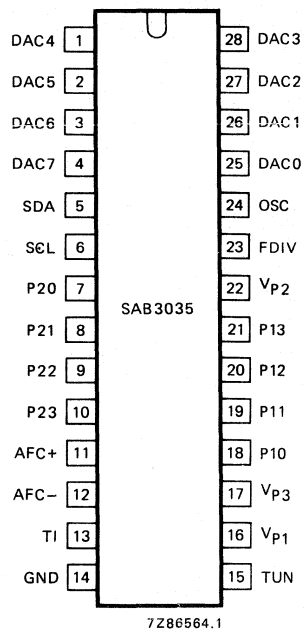


Fig. 2 Pinning diagram.

PINNING

1	DAC4	outputs of static DACs
2	DAC5	
3	DAC6	
4	DAC7	
5	SDA	serial data line (I²C bus)
6	SCL	serial clock line (I²C bus)
7	P20	general purpose input/output ports
8	P21	
9	P22	
10	P23	
11	AFC+	a.f.c. inputs
12	AFC−	
13	TI	tuning voltage amplifier inverting input
14	GND	ground
15	TUN	tuning voltage amplifier output
16	V_{P1}	+12 V supply voltage
17	V_{P3}	+32 V supply for tuning voltage amplifier
18	P10	High-current band-selection output ports
19	P11	
20	P12	
21	P13	
22	V_{P2}	positive supply for high-current band-selection output circuits
23	FDIV	input from prescaler
24	OSC	crystal oscillator input
25	DAC0	outputs of static DACs
26	DAC1	
27	DAC2	
28	DAC3	

FUNCTIONAL DESCRIPTION

The SAB3035 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Eight 6-bit digital-to-analogue converters DAC0 to DAC7 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

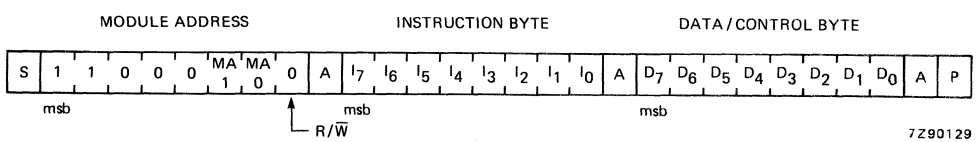


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	½V_{P1}
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

INSTRUCTION BYTE

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
freq.	1	F14	F13	F12	F11	F10	F9	F8
TCD0	0	0	1	0	1	0	0	1
TCD1	0	0	1	0	1	0	1	0
TCD2	0	0	1	0	1	0	1	1

DATA/CONTROL BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
F7	F6	F5	F4	F3	F2	F1	F0
AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X2, X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

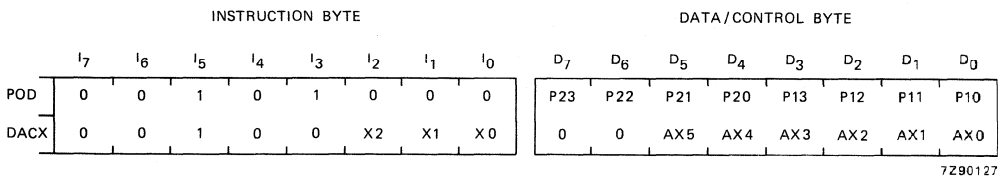


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

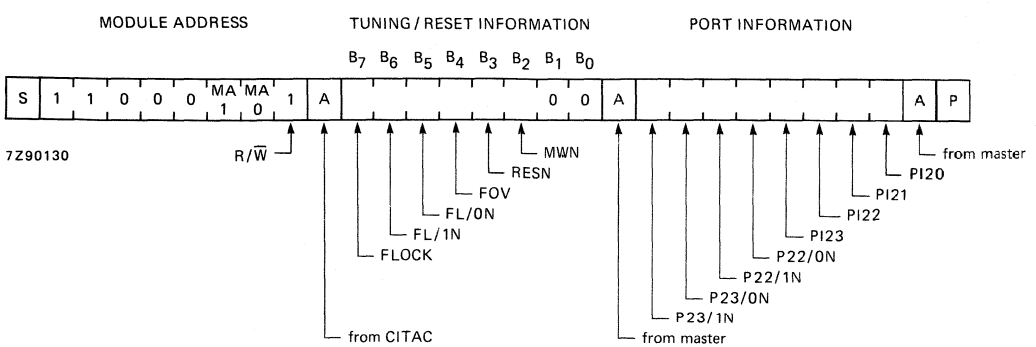


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

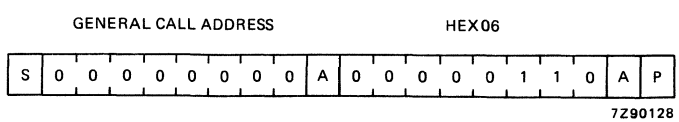


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 16)	V_{P1}	−0,3 to +18	V
(pin 22)	V_{P2}	−0,3 to +18	V
(pin 17)	V_{P3}	−0,3 to +36	V
Input/output voltage ranges:			
(pin 5)	V_{SDA}	−0,3 to +18	V
(pin 6)	V_{SCL}	−0,3 to +18	V
(pins 7 to 10)	V_{P2X}	−0,3 to +18	V
(pins 11 and 12)	$V_{AFC+,AFC-}$	−0,3 to V_{P1}*	V
(pin 13)	V_{TI}	−0,3 to V_{P1}*	V
(pin 15)	V_{TUN}	−0,3 to V_{P3}*	V
(pins 18 to 21)	V_{P1X}	−0,3 to V_{P2}**	V
(pin 23)	V_{FDIV}	−0,3 to V_{P1}*	V
(pin 24)	V_{OSC}	−0,3 to +5	V
(pins 1 to 4 and 25 to 28)	V_{DACX}	−0,3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	20	32	50	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	–2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	400	–	mW
Operating ambient temperature	T_{amb}	–20	–	+70	°C
I^2C bus inputs/outputs					
SDA input (pin 5); SCL input (pin 6)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	–0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 5, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 7 to 10, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	–0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 11, 12)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 13, 15)					
Maximum output voltage at $I_{load} = \pm 2,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 2,5$ mA:					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 18 to 21)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 23)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14,5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 7 (pins 25 to 28 and 1 to 4)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11,5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0,1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0,5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 7) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

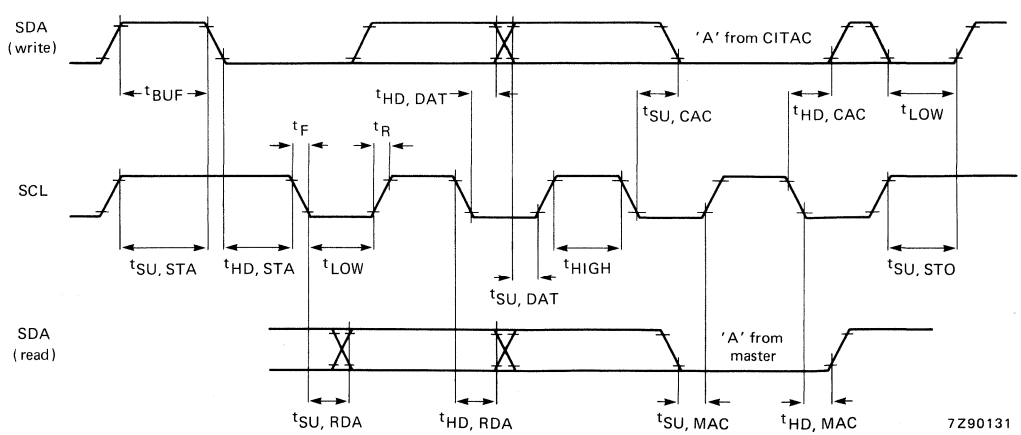


Fig. 8 I²C bus timing SAB3035.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3036 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 5)	V_{P1}	typ.	12 V
(pin 14)	V_{P2}	typ.	13 V
(pin 9)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 5)	I_{P1}	typ.	23 mA
(pin 14)	I_{P2}	typ.	0,1 mA
(pin 9)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	300 mW
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

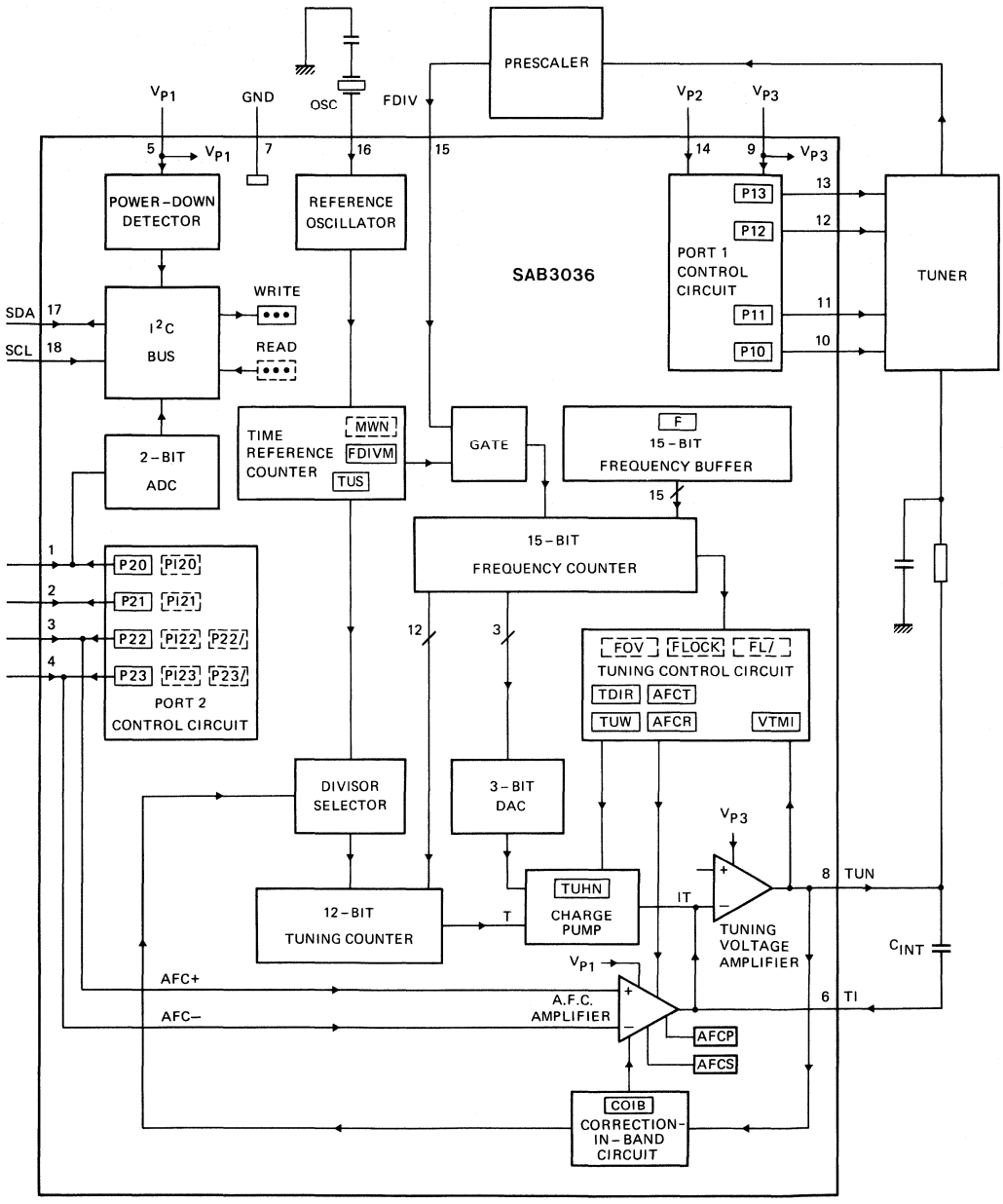


Fig. 1 Block diagram.

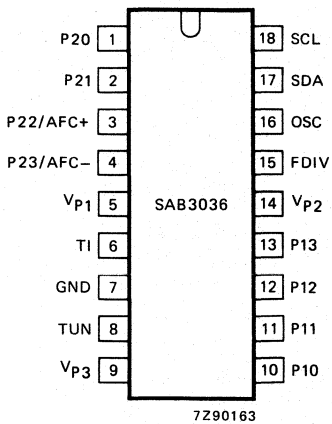


Fig. 2 Pinning diagram.

PINNING

1	P20	general purpose input/output ports
2	P21	
3	P22/AFC+	general purpose input/output ports and a.f.c. inputs
4	P23/AFC−	
5	V_{P1}	+ 12 V supply voltage
6	TI	tuning voltage amplifier inverting input
7	GND	ground
8	TUN	tuning voltage amplifier output
9	V_{P3}	+ 32 V supply for tuning voltage amplifier
10	P10	high-current band-selection output ports
11	P11	
12	P12	
13	P13	
14	V_{P2}	positive supply for high-current band-selection output circuits
15	FDIV	input from prescaler
16	OSC	crystal oscillator input
17	SDA	serial data line, I^2C bus
18	SCL	serial clock line, I^2C bus

Purchase of Philips I^2C components conveys a licence under the Philips' I^2C patent to use the components in the I^2C system provided the system conforms to the I^2C specifications defined by Philips.

FUNCTIONAL DESCRIPTION

The SAB3036 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals and are connected with the AFC+ and AFC− inputs respectively. The a.f.c. amplifier must be switched off when P22 and/or P23 are used. When a.f.c. is used, P22 and P23 must be programmed HIGH (high impedance state). With the aid of port P20, up to three independent module addresses can be programmed.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

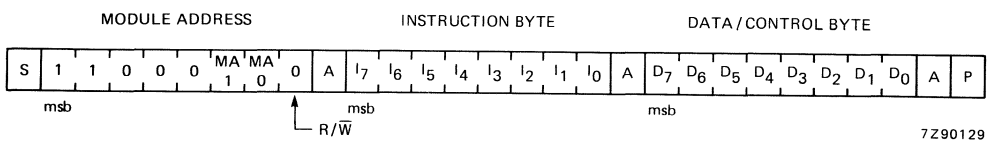


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

OPERATION (continued)

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

INSTRUCTION BYTE

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
freq.	1	F14	F13	F12	F11	F10	F9	F8
TCD0	0	0	1	0	1	0	0	1
TCD1	0	0	1	0	1	0	1	0
TCD2	0	0	1	0	1	0	1	1

DATA/CONTROL BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
F7	F6	F5	F4	F3	F2	F1	F0
AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\,\mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

OPERATION (continued)

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction byte POD (port output data) is shown in Fig. 5, together with the corresponding data/control byte. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

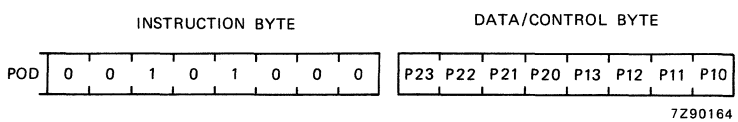


Fig. 5 Control programming.

OPERATION (continued)

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

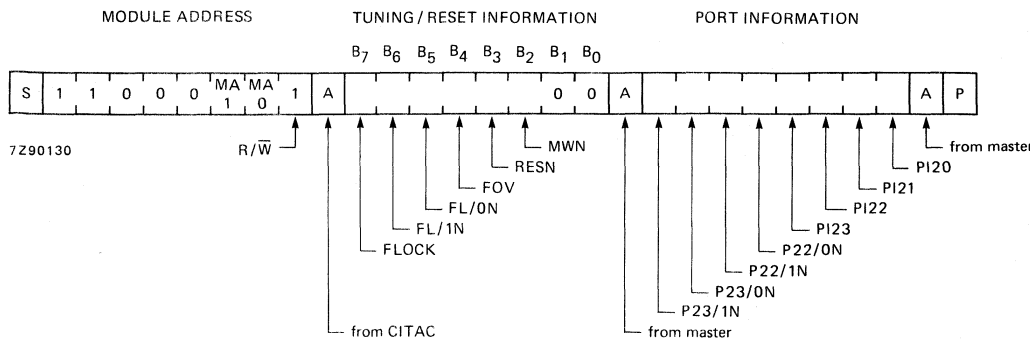


Fig. 6 Information byte format.

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

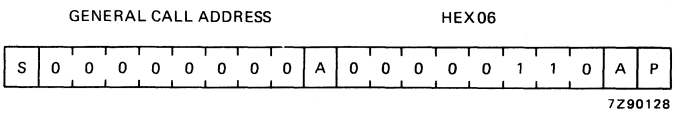


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:		
(pin 5)	V_{P1}	−0,3 to + 18 V
(pin 14)	V_{P2}	−0,3 to + 18 V
(pin 9)	V_{P3}	−0,3 to + 36 V
Input/output voltage ranges:		
(pin 17)	V_{SDA}	−0,3 to + 18 V
(pin 18)	V_{SCL}	−0,3 to + 18 V
(pins 1 and 2)	$V_{P20, P21}$	−0,3 to + 18 V
(pins 3 and 4)	$V_{P22, P23, AFC}$	−0,3 to V_{P1}* V
(pin 6)	V_{TI}	−0,3 to V_{P1}* V
(pin 8)	V_{TUN}	−0,3 to V_{P3}* V
(pins 10 to 13)	V_{P1X}	−0,3 to V_{P2}** V
(pin 15)	V_{FDIV}	−0,3 to V_{P1}* V
(pin 16)	V_{OSC}	−0,3 to + 5 V
Total power dissipation	P_{tot}	max. 1000 mW
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature	T_{amb}	−20 to + 70 °C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.
** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	14	23	40	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	–2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	300	–	mW
Operating ambient temperature	T_{amb}	–20	–	+70	°C
I^2C bus inputs/outputs					
SDA input (pin 17); SCL input (pin 18)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	–0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 17, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 1 to 4, open collector)					
Input voltage HIGH (P20, P21)	V_{IH}	2	–	16	V
Input voltage HIGH (P22, P23) AFC switched off	V_{IH}	2	–	$V_{P1}-2$	V
Input voltage LOW	V_{IL}	–0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 3, 4)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current (P22 and P23 programmed HIGH)	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 6, 8)					
Maximum output voltage at $I_{load} = \pm 2,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 2,5$ mA:					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 10 to 13)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 15)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	16	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 1) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	µs
Start condition set-up time	$t_{SU,STA}$	4	–	–	µs
Start condition hold time	$t_{HD,STA}$	4	–	–	µs
SCL, SDA LOW period	t_{LOW}	4	–	–	µs
SCL HIGH period	t_{HIGH}	4	–	–	µs
SCL, SDA rise time	t_R	–	–	1	µs
SCL, SDA fall time	t_F	–	–	0,3	µs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	µs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	µs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	µs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	µs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	µs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	µs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	µs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	µs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	µs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 µs delay.

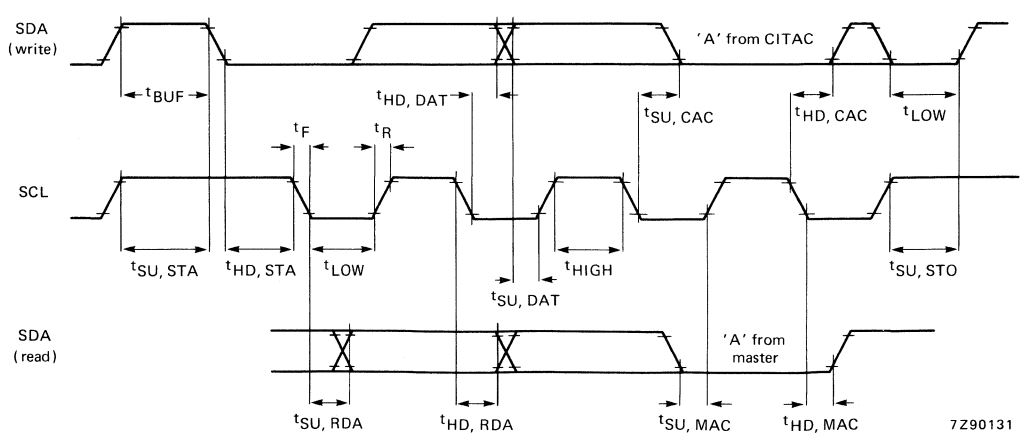


Fig. 8 I²C bus timing SAB3036.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3037 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 4 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 4 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages				
(pin 13)	V_{P1}	typ.	12	V
(pin 19)	V_{P2}	typ.	13	V
(pin 14)	V_{P3}	typ.	32	V
Supply currents (no outputs loaded)				
(pin 13)	I_{P1}	typ.	30	mA
(pin 19)	I_{P2}	typ.	0,1	mA
(pin 14)	I_{P3}	typ.	0,6	mA
Total power dissipation	P_{tot}	typ.	380	mW
Operating ambient temperature range	T_{amb}	−20 to +70		°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

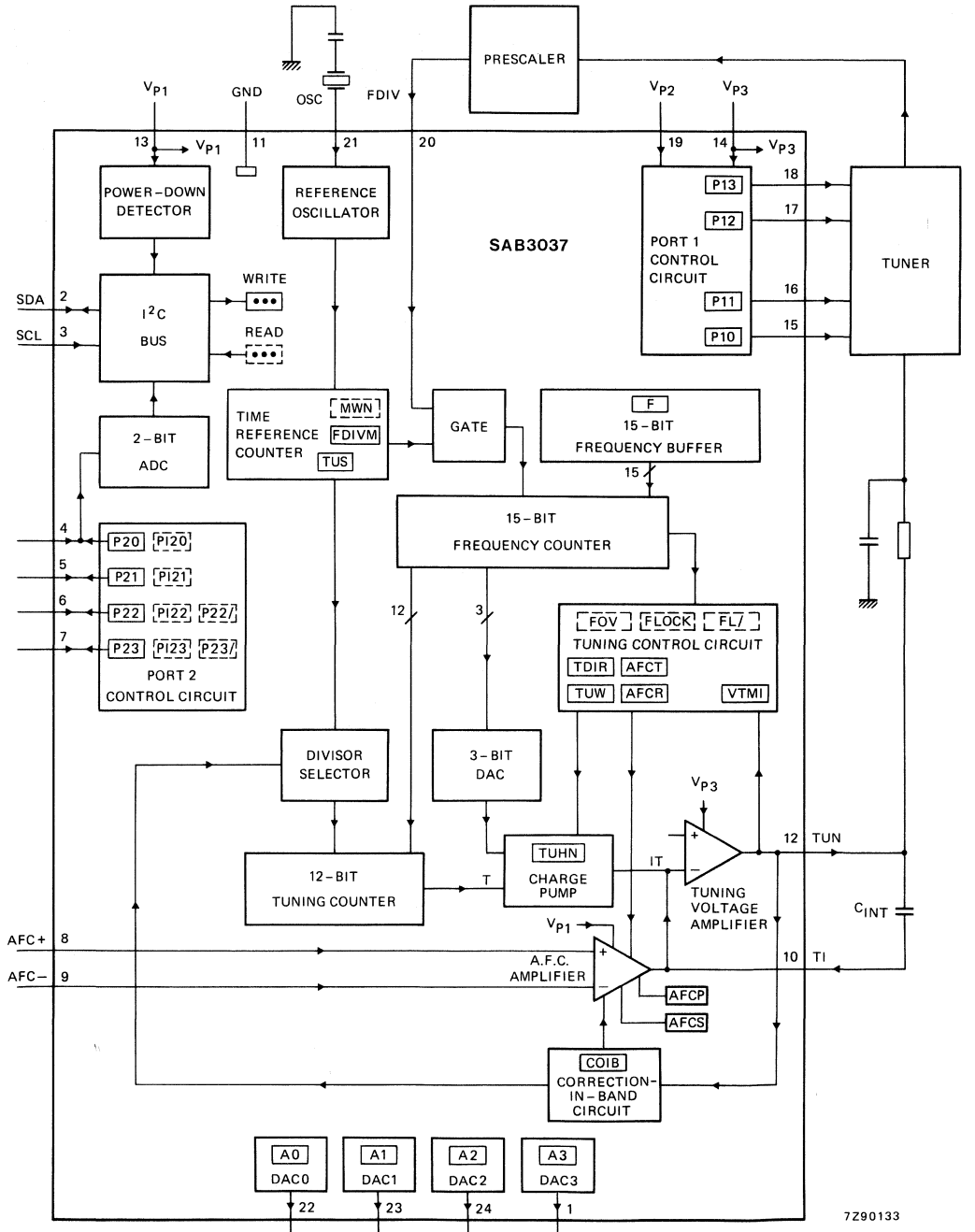


Fig. 1 Block diagram.

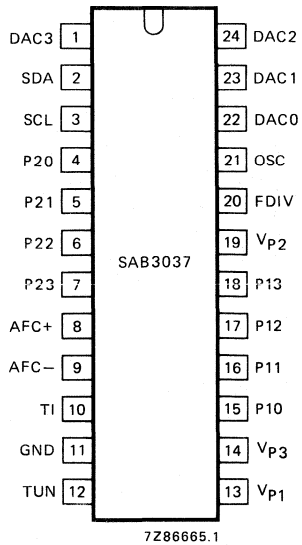


Fig. 2 Pinning diagram.

PINNING

1	DAC3	output of static DAC
2	SDA	serial data line (I²C bus)
3	SCL	serial clock line (I²C bus)
4	P20	general purpose input/output ports
5	P21	general purpose input/output ports
6	P22	general purpose input/output ports
7	P23	general purpose input/output ports
8	AFC +	a.f.c. inputs
9	AFC−	a.f.c. inputs
10	TI	tuning voltage amplifier inverting input
11	GND	ground
12	TUN	tuning voltage amplifier output
13	V_{P1}	+ 12 V supply voltage
14	V_{P3}	+ 32 V supply for tuning voltage amplifier
15	P10	high-current band-selection output ports
16	P11	high-current band-selection output ports
17	P12	high-current band-selection output ports
18	P13	high-current band-selection output ports
19	V_{P2}	positive supply for high-current band-selection output circuits
20	FDIV	input from prescaler
21	OSC	crystal oscillator input
22	DAC0	outputs of static DACs
23	DAC1	outputs of static DACs
24	DAC2	outputs of static DACs

FUNCTIONAL DESCRIPTION

The SAB3037 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at $\Delta f = 50$ kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at $\Delta f = 50$ kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Four 6-bit digital-to-analogue converters DAC0 to DAC3 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

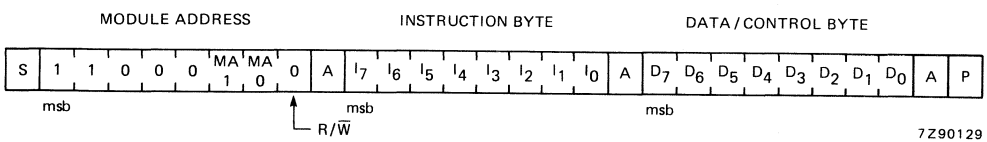


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

	INSTRUCTION BYTE								DATA/CONTROL BYTE							
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
freq.	1	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
TCD0	0	0	1	0	1	0	0	1	AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
TCD1	0	0	1	0	1	0	1	0	VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
TCD2	0	0	1	0	1	0	1	1	0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

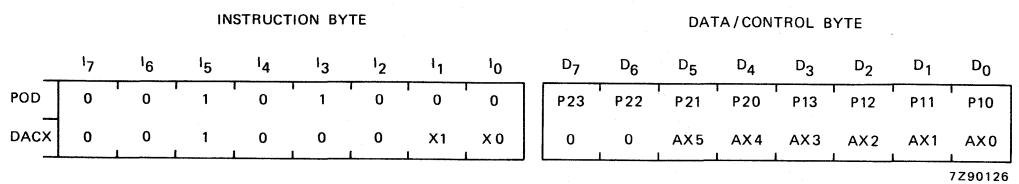


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

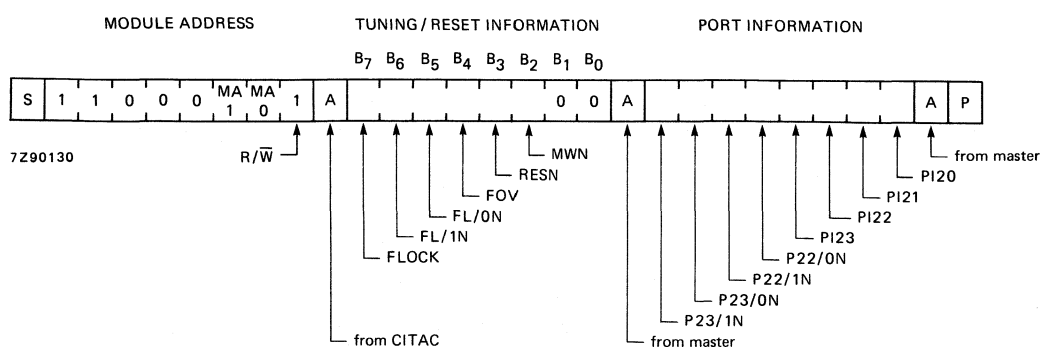


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

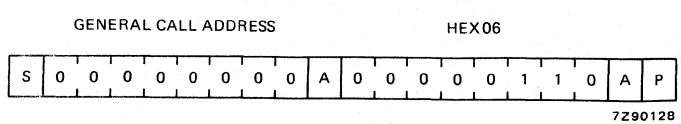


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 13)	V_{P1}	−0,3 to +18	V
(pin 19)	V_{P2}	−0,3 to +18	V
(pin 14)	V_{P3}	−0,3 to +36	V
Input/output voltage ranges:			
(pin 2)	V_{SDA}	−0,3 to +18	V
(pin 3)	V_{SCL}	−0,3 to +18	V
(pins 4 to 7)	V_{P2X}	−0,3 to +18	V
(pins 8 and 9)	$V_{AFC+,AFC-}$	−0,3 to V_{P1}*	V
(pin 10)	V_{TI}	−0,3 to V_{P1}*	V
(pin 12)	V_{TUN}	−0,3 to V_{P3}*	V
(pins 15 to 18)	V_{P1X}	−0,3 to V_{P2}**	V
(pin 20)	V_{FDIV}	−0,3 to V_{P1}*	V
(pin 21)	V_{OSC}	−0,3 to +5	V
(pins 1 and 22 to 24)	V_{DACX}	−0,3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	18	30	45	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	−2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	380	–	mW
Operating ambient temperature	T_{amb}	−20	–	+70	°C
I²C bus inputs/outputs					
SDA input (pin 2); SCL input (pin 3)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	−0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 2, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 4 to 7, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 8, 9)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 10, 12)					
Maximum output voltage at $I_{load} = \pm 2,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 2,5$ mA:					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current i into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 15 to 18)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 20)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14,5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 21)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 3 (pins 22 to 24 and pin 1)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11,5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0,1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0,5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 4) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

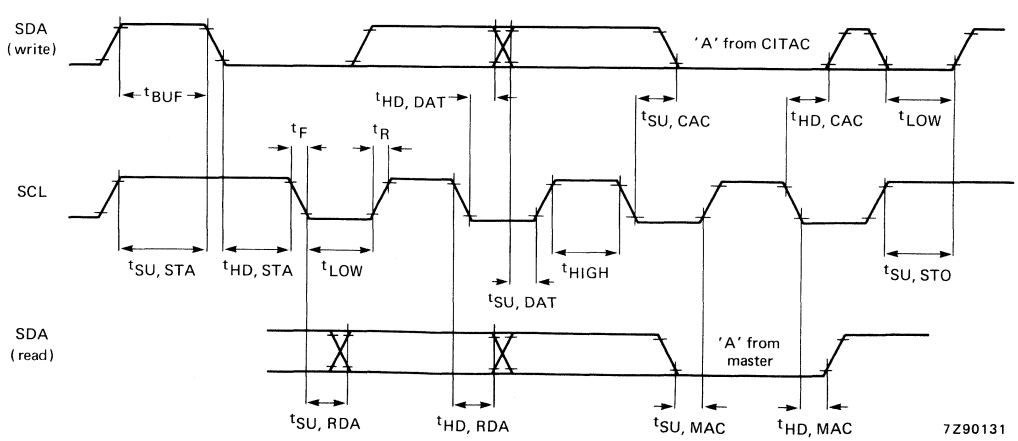


Fig. 8 I²C bus timing SAB3037.

REMOTE CONTROL SYSTEM FOR INFRARED OPERATION

The SAF1032P (receiver/decoder) and the SAF1039P (transmitter) form the basic parts of a sophisticated remote control system (pcm: pulse code modulation) for infrared operation. The ICs can be used, for example, in TV, audio, industrial equipment, etc.
Features:

SAF1032P receiver/decoder:
- 16 programme selection codes
- automatic preset to stand-by at power 'ON', including automatic analogue base settings to 50% and automatic preset of programme selection '1' code
- 3 analogue function controls, each with 63 steps
- single supply voltage
- protection against corrupt codes.

SAF1039P transmitter:
- 32 different control commands
- static keyboard matrix
- current drains from battery only during key closure time
- two transmission modes selectable.

The devices are implemented in LOCMOS (Local Oxidation Complementary MOS) technology to achieve an extremely low power consumption.
Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

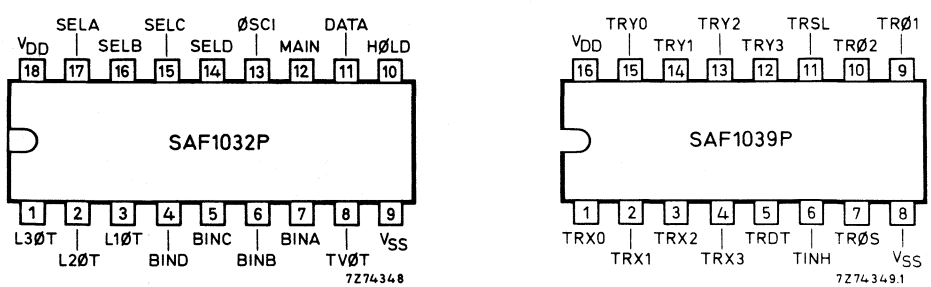


Fig. 1 Pin designations.

PACKAGE OUTLINES

SAF1032P: 18-lead DIL; plastic (SOT-102).
SAF1039P: 16-lead DIL; plastic (SOT-38Z).

PINNING

To facilitate easy function recognition, each integrated circuit pin has been allocated a code as shown below.

SAF1032P

1	L3ØT	linear output	10	HØLD	control input
2	L2ØT	linear output	11	DATA	data input
3	L1ØT	linear output	12	MAIN	reset input
4	BIND	binary 8 output	13	ØSCI	clock input
5	BINC	binary 4 output	14	SELD	binary 8 output
6	BINB	binary 2 output	15	SELC	binary 4 output
7	BINA	binary 1 output	16	SELB	binary 2 output
8	TVØT	on/off input/output	17	SELA	binary 1 output
9	V_{SS}		18	V_{DD}	

SAF1039P

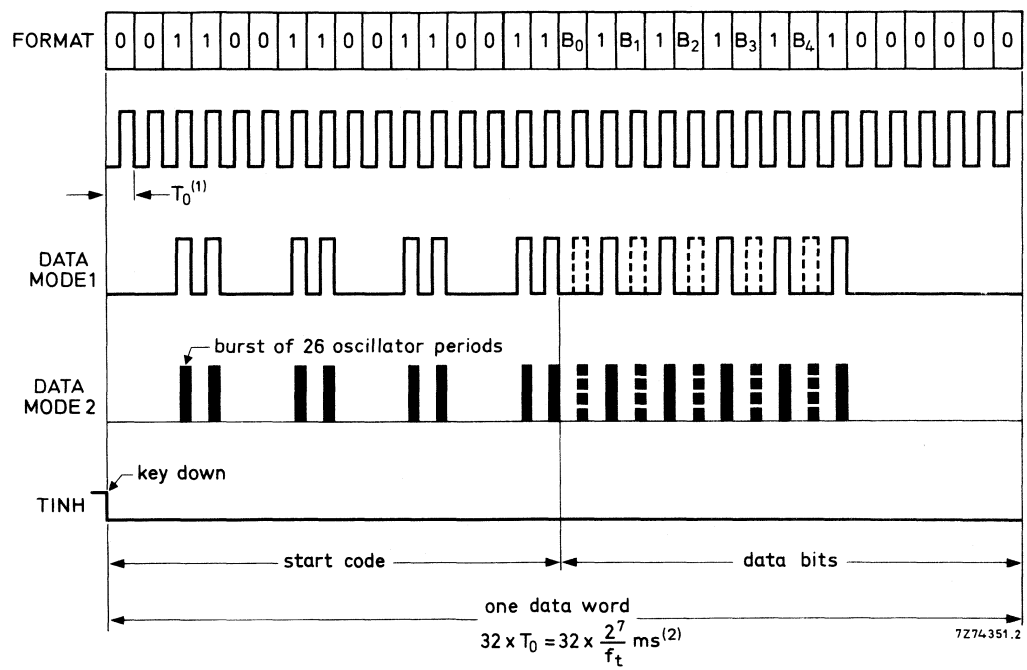
1	TRX0	keyboard input	9	TRØ1	oscillator control input
2	TRX1	keyboard input	10	TRØ2	oscillator control input
3	TRX2	keyboard input	11	$\overline{TRSL}$	keyboard select line
4	TRX3	keyboard input	12	TRY3	keyboard input
5	TRDT	data output	13	TRY2	keyboard input
6	TINH	inhibit output/mode select input	14	TRY1	keyboard input
7	TRØS	oscillator output	15	TRY0	keyboard input
8	V_{SS}		16	V_{DD}	

BASIC OPERATING PRINCIPLES

The data to be transmitted are arranged as serial information with a fixed pattern (see Fig. 2), in which the data bit-locations B_0 to B_4 represent the generated key-command code. To cope with IR (infrared) interferences of other sources a selective data transmission is present. Each transmitted bit has a burst of 26 oscillator periods.

Before any operation will be executed in the receiver/decoder chip, the transmitted data must be accepted twice in sequence. This means the start code must be recognized each time a data word is applied and comparison must be true between the data bits of two successively received data words. If both requirements are met, one group of binary output buffers will be loaded with a code defined by the stored data bits, and an internal operation can also take place. See operating code table.

The contents of the 3 analogue function registers are available on the three outputs in a pulse code versus time modulation format after D (digital) to A (analogue) conversion. The proper analogue levels can be obtained by using simple integrated networks. For local control a second transmitter chip (SAF1039P) is used (see Fig. 7).



(1) T_0 = 1 clock period = 128 oscillator periods. (2) f_t in kHz.

Fig. 2 Pattern for data to be transmitted.

TIMING CONSIDERATIONS

The transmitter and receiver operate at different oscillator frequencies. Due to the design neither frequency is very critical, but correlation between them must exist. Calculation of these timing requirements shows the following.

With a tolerance of ±10% on the oscillator frequency (f_t) of the transmitter, the receiver oscillator frequency ($f_r = 3 \times f_t$) must be kept constant with a tolerance of ±20%.
On the other hand, the data pulse generated by the pulse stretcher circuit (at the receiver side) may vary ±25% in duration.

GENERAL DESCRIPTION OF THE SAF1039P TRANSMITTER

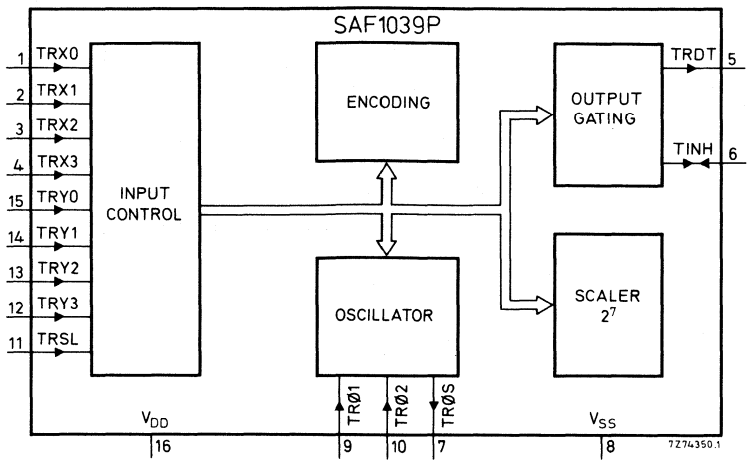


Fig. 3 Block diagram of SAF1039P transmitter.

Any keyboard activity on the inputs TRX0 to TRX3, TRY0 to TRY3 and TRSL will be detected. For a legal key depression, one key down at a time (one TRX and TRY input activated), the oscillator starts running and a data word, as shown on the previous page, is generated and supplied to the output TRDT. If none, or more than 2 inputs are activated at the same time, the input detection logic of the chip will generate an overall reset and the oscillator stops running (no legal key operation).

This means that for each key-bounce the logic will be reset, and by releasing a key the transmitted data are stopped at once.

The minimum key contact time required is the duration of two data words. The on-chip oscillator is frequency controlled with the external components R1 and C1 (see circuit Fig. 6); the addition of resistor R2 means that the oscillator frequency is practically independent of supply voltage variations. A complete data word is arranged as shown in Fig. 2, and has a length of 32 x T_0 ms, where $T_0 = 2^7/f_t$.

Operation mode

	DATA	FUNCTION OF TINH
1	unmodulated: LOCAL operation	output, external pull-up resistor to V_{DD}
2	modulated: REMOTE control	input, connected to V_{SS}

GENERAL DESCRIPTION OF THE SAF1032P RECEIVER/DECODER

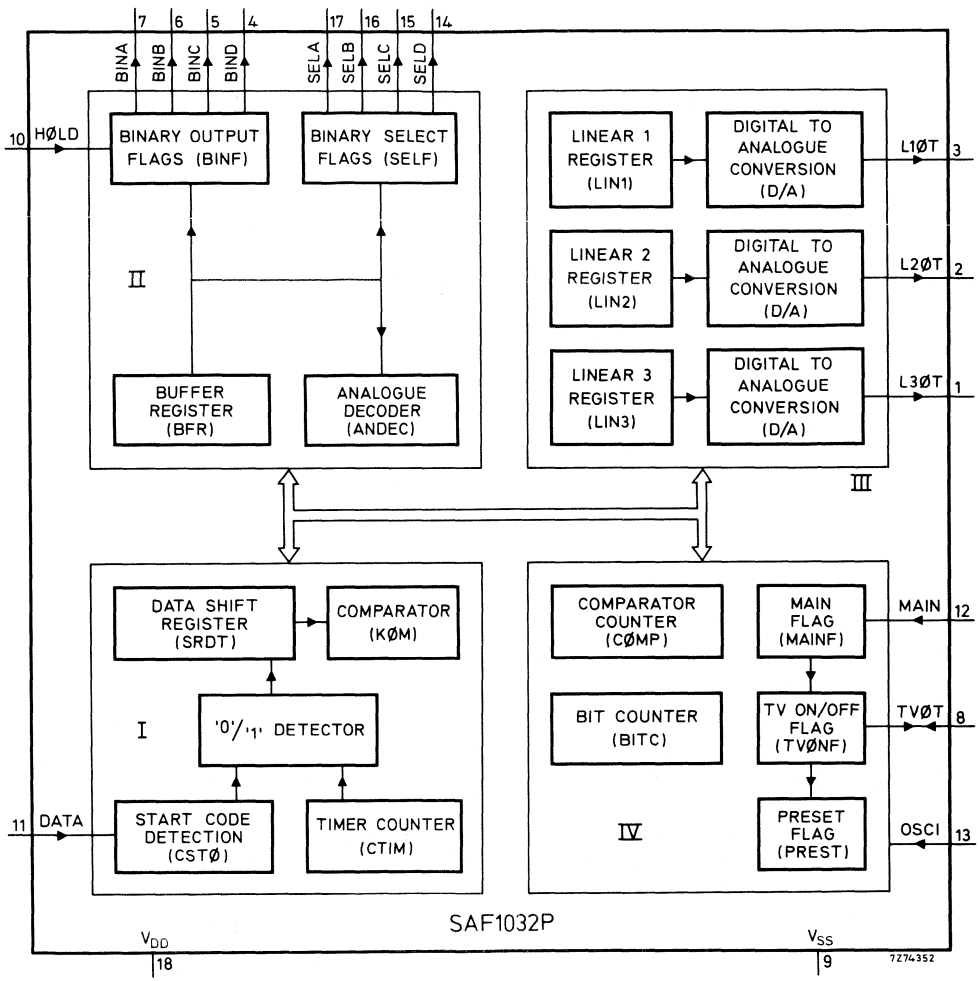


Fig. 4 Block diagram of SAF1032P receiver/decoder.

The logic circuitry of the receiver/decoder chip is divided into four main parts as shown in the block diagram above.

Part I

This part decodes the applied DATA information into logic '1' and '0'.
It also recognizes the start code and compares the stored data-bits with the new data-bits accepted.

Part II

This part stores the programme selection code in the output group (BINF) and memorizes it for condition HØLD = LOW.

It puts the functional code to output group (SELF) during data accept time, and decodes the internally used analogue commands (ANDEC).

Part III

This part controls the analogue function registers (each 6-bits long), and connects the contents of the three registers to the analogue outputs by means of D/A conversion. During sound mute, output L1ØT will be forced to HIGH level.

Part IV

This part keeps track for correct power 'ON' operation, and puts chip in 'stand-by' condition at supply voltage interruptions.

The logic design is dynamic and synchronous with the clock frequency (ØSCI), while the required control timing signals are derived from the bit counter (BITC).

Operation

Serial information applied to the DATA input will be translated into logic '1' and '0' by means of a time ratio detector.

After recognizing the start code (CSTØ) of the data word, the data bits will be loaded into the data shift register (SRDT). At the first trailing edge of the following data word a comparison (KØM) takes place between the contents of SRDT and the buffer register (BFR). If SRDT equals BFR, the required operation will be executed under control of the comparator counter (CØMP).

As shown in the operating code table on the next page, the 4-bit wide binary output buffer (BINF) will be loaded for BFR0 = '0', while for BFR0 = '1' the binary output buffer (SELF), also 4-bit wide will be activated during the data accept time.

At the same time operations involving the internal commands are executed. The contents of the analogue function registers (each 6-bits long) are controlled over 63 steps, with minimum and maximum detection, while the D/A conversion results in a pulsed output signal with a conversion period of 384 clock periods (see Fig. 5).

First power 'ON' will always put the chip in the 'stand-by' position. This results in an internal clearing of all logic circuitry and a 50% presetting of the contents of the analogue registers (analogue base value). The programme selection '1' code will also be prepared and all the outputs will be non-active (see operating output code table).

From 'stand-by' the chip can be made operational via a programme selection command, generated LOCAL or via REMOTE, or directly by forcing the TV ON/OFF output (TVØT) to zero for at least 2 clock periods of the oscillator frequency.

For POWER ON RESET a negative-going pulse should be applied to input MAIN, when V_{DD} is stabilized; pulse width LOW $\geqslant$ 100 μs.

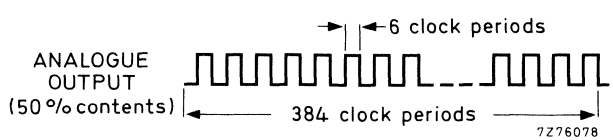


Fig. 5 Analogue output pulses.

OPERATING CODE TABLE

key-matrix position			buffer BFR					BINF (BIN.)				SELF (SEL.)				function
TRX.	TRY.	TRSL	0	1	2	3	4	A	B	C	D	A	B	C	D	
0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	1	programme select + ON
0	1	0	0	0	0	1	0	1	0	0	0	1	1	1	1	
0	2	0	0	0	1	0	0	0	1	0	0	1	1	1	1	
0	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	
1	0	0	0	1	1	1	0	0	0	1	0	1	1	1	1	
1	1	0	0	1	0	1	0	1	0	1	0	1	1	1	1	
1	2	0	0	1	1	0	0	0	1	1	0	1	1	1	1	
1	3	0	0	1	0	0	0	1	1	1	0	1	1	1	1	
2	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1	programme select + ON
2	1	0	0	0	0	1	1	1	0	0	1	1	1	1	1	
2	2	0	0	0	1	0	1	0	1	0	1	1	1	1	1	
2	3	0	0	0	0	0	1	1	1	0	1	1	1	1	1	
3	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1	
3	1	0	0	1	0	1	1	1	0	1	1	1	1	1	1	
3	2	0	0	1	1	0	1	0	1	1	1	1	1	1	1	
3	3	0	0	1	0	0	1	1	1	1	1	1	1	1	1	
0	0	1	1	0	1	1	0	X	X	X	X	0	1	1	1	analogue base reg. (LIN3) + 1
0	1	1	1	0	0	1	0	X	X	X	X	0	0	1	1	reg. (LIN2) + 1
0	2	1	1	0	1	0	0	X	X	X	X	0	1	0	1	reg. (LIN1) + 1
0	3	1	1	0	0	0	0	X	X	X	X	0	0	0	1	OFF
1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	reg. (LIN3) − 1
1	1	1	1	1	0	1	0	X	X	X	X	1	0	1	1	reg. (LIN2) − 1
1	2	1	1	1	1	0	0	X	X	X	X	1	1	0	1	reg. (LIN1) − 1
1	3	1	1	1	0	0	0	X	X	X	X	1	0	0	1	
2	0	1	1	0	1	1	1	X	X	X	X	0	1	1	0	mute (set/reset)
2	1	1	1	0	0	1	1	X	X	X	X	0	0	1	0	spare functions
2	2	1	1	0	1	0	1	X	X	X	X	0	1	0	0	
2	3	1	1	0	0	0	1	X	X	X	X	0	0	0	0	
3	0	1	1	1	1	1	1	X	X	X	X	1	1	1	0	
3	1	1	1	1	0	1	1	X	X	X	X	1	0	1	0	
3	2	1	1	1	1	0	1	X	X	X	X	1	1	0	0	
3	3	1	1	1	0	0	1	X	X	X	X	1	0	0	0	

Note

Reset mute also on programme select codes, (LIN1) ± 1, and analogue base.

OPERATING OUTPUT CODE

	(BIN.)				(SEL.)				(LØT)			TVØT
	A	B	C	D	A	B	C	D	1	2	3	
'stand-by' OFF via remote	0	0	0	0	0	0	0	0	1	0	0	1
ON – 'not hold' condition non-operating	1	1	1	1	1	1	1	1	X	X	X	0
ON – 'hold' condition non-operating	X	X	X	X	1	1	1	1	X	X	X	0

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}-V_{SS}		−0,5 to 11	V
Input voltage	V_I	max.	11	V
Current into any terminal	$\pm I_I$	max.	10	mA
Power dissipation (per output)	P_o	max.	50	mW
Power dissipation (per package)	P_{tot}	max.	200	mW
Operating ambient temperature	T_{amb}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

CHARACTERISTICS

T_{amb} = 0 to +85 °C (unless otherwise specified)

SAF1039P only

	symbol	min.	typ.	max.		V_{DD} V	T_{amb} °C
Recommended supply voltage	V_{DD}	7	–	10	V		
Supply current							
quiescent	I_{DD}	–	–	10	μA	10	25
		–	1	50	μA	7	65
operating; TRØ1 at V_{SS}; outputs unloaded; one keyboard switch closed	I_{DD}	–	–	1,7	mA	10	all
		–	0,8	–	mA	10	25
Inputs (note 1)							
TRØ2; TINH (note 2)							
input voltage HIGH	V_{IH}	$0,8V_{DD}$	–	V_{DD}	V	7 to 10	all
input voltage LOW	V_{IL}	0	–	$0,2V_{DD}$	V	7 to 10	all
input current	I_I	–	10^{-5}	1	μA	10	25
Outputs							
TRDT; TRØS; TRØ1							
output current HIGH at $V_{OH} = V_{DD} - 0,5$ V	$-I_{OH}$	0,4	–	–	mA	7	all
output current LOW at V_{OL} = 0,4 V	I_{OL}	0,4	–	–	mA	7	all
TRDT output leakage current when disabled $V_O = V_{SS}$ to V_{DD}	I_{OL}	–	–	1	μA	10	25
TINH							
output current LOW V_{OL} = 0,4 V	I_{OL}	0,4	–	–	mA	7	all
Oscillator							
maximum oscillator frequency	f_{osc}	120	–	–	kHz		
frequency variation with supply voltage, temperature and spread of IC properties at f_{nom} = 36 kHz (note 3)	Δf	–	–	$0,15f_{nom}$		7 to 10	all
oscillator current drain at f_{nom} = 36 kHz	I_{osc}	–	1,3	2,5	mA	10	25

Notes follow characteristics.

CHARACTERISTICS

T_{amb} = 0 to +85 °C (unless otherwise specified)

SAF1032P only

	symbol	min.	typ.	max.		V_{DD} V	T_{amb} °C
Recommended supply voltage	V_{DD}	8	–	10	V		
Supply current							
quiescent	I_{DD}	–	–	50	μA	10	25
		–	1	300	μA	10	85
operating; I_O = 0; at ØSCI frequency of 100 kHz	I_{DD}	–	–	1	mA	10	all
Inputs							
DATA; ØSCI; HØLD; TVØT (see note 4)							
input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V	8 to 10	all
input voltage LOW	V_{IL}	0	–	$0{,}2V_{DD}$	V	8 to 10	all
MAIN; tripping levels							
input voltage increasing	V_{ti}	$0{,}4V_{DD}$	–	$0{,}9V_{DD}$	V	5 to 10	all
input voltage decreasing	V_{td}	$0{,}1V_{DD}$	–	$0{,}6V_{DD}$	V	5 to 10	all
input current; all inputs except TVØT	I_I	–	10^{-5}	1	μA	10	25
input signal rise and fall times (10% and 90% V_{DD}) all inputs except MAIN	t_r, t_f	–	–	5	μs	8 to 10	all
Outputs							
programme selection: BINA/B/C/D							
auxiliary: SELA/B/C/D							
analogue: L3ØT; L2ØT; L1ØT TVØT (note 4)							
all open drain n-channel output current LOW at V_{OL} = 0,4 V	I_{OL}	1,6	–	–	mA	8	all
output leakage current at $V_O = V_{SS}$ to V_{DD}	I_{OL}	–	–	10	μA	10	all

For note 4 see next page.

Notes to characteristics

1. The keyboard inputs (TRX.; TRY.; TRSL) are not voltage driven (see application information diagram Fig. 6).

   If one key is depressed, the circuit generates the corresponding code. The number of keys depressed at a time, and this being recognized by the circuit as an illegal operation, depends on the supply voltage (V_{DD}) and the leakage current (between device and printed-circuit board) externally applied to the keyboard inputs.

   If no leakage is assumed, the circuit recognizes an operation as illegal for any number of keys > 1 depressed at the same time with $V_{DD} = 7$ V. At a leakage due to a 1 MΩ resistor connected to each keyboard input and returned to either V_{DD} or V_{SS}, the circuit recognizes at least 2 keys depressed at a time with $V_{DD} = 7$ V.

   The highest permissible values of the contact series resistance of the keyboard switches is 500 Ω.

2. Inhibit output transistor disabled.

3. Δf is the width of the distribution curve at 2 σ points (σ = standard deviation).

4. Terminal TVØT is input for manual 'ON'. When applying a LOW level TVØT becomes an output carrying a LOW level.

APPLICATION INFORMATION

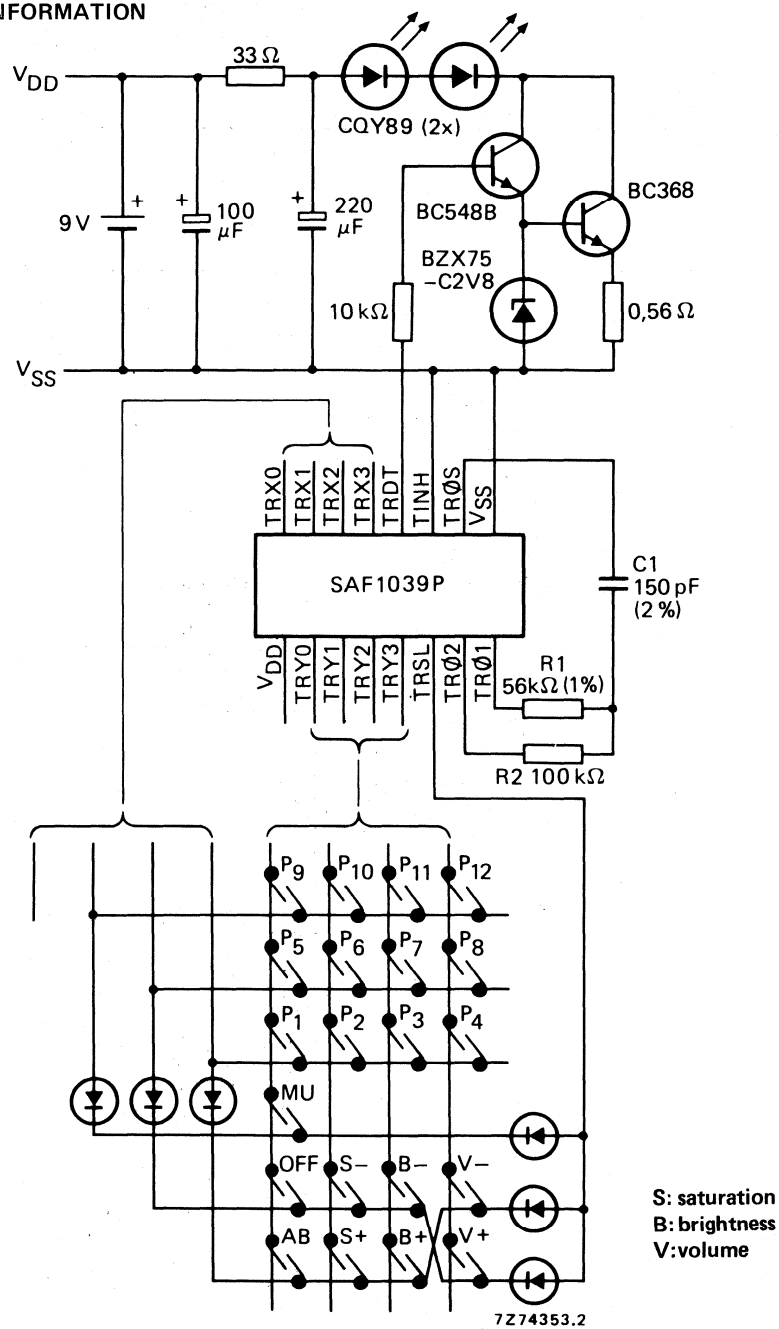


Fig. 6 Interconnection diagram of transmitter circuit SAF1039P in a remote control system, for a television receiver with 12 programmes.

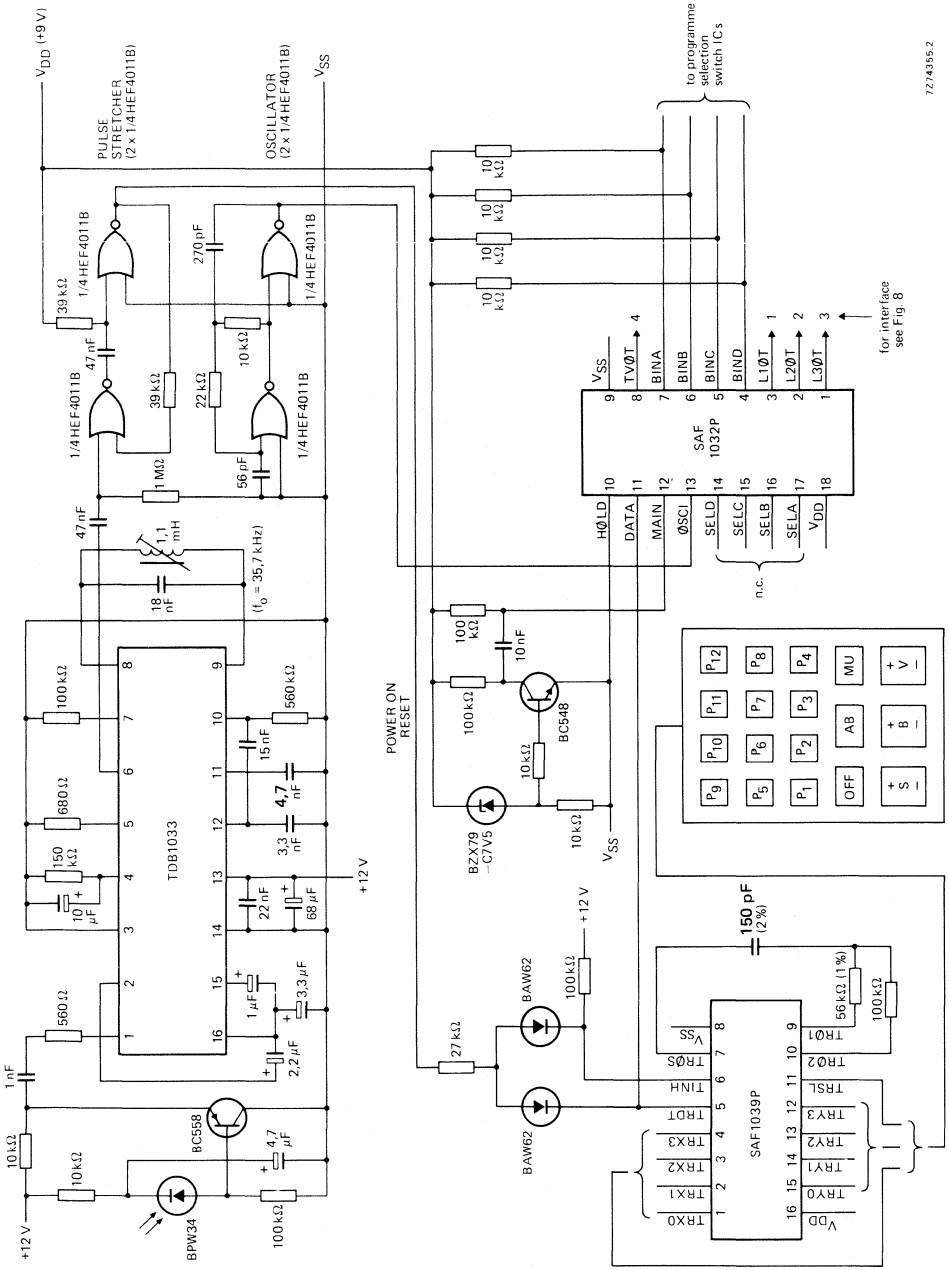


Fig. 7 Interconnection diagram showing the SAF1032P and SAF1039P used in a TV control system.

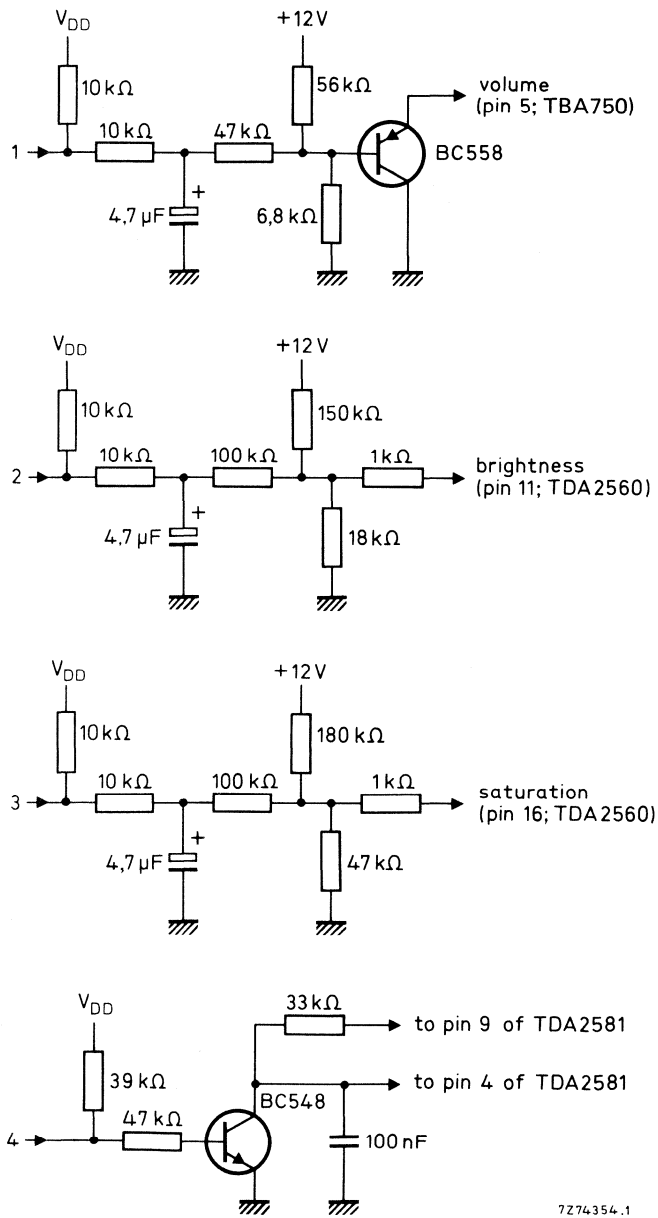


Fig. 8 Additional circuits from outputs L1ØT (1), L2ØT (2), L3ØT (3) and TVØT (4) of the SAF1032P in circuit of Fig. 7.

SOUND I.F. AMPLIFIER/DEMODULATOR FOR TV

The TBA120U is an i.f. amplifier with a symmetrical FM demodulator and an a.f. amplifier with adjustable output voltage. The a.f. amplifier is also provided with an output for volume control and an input for VCR operation.

The input and output of the TBA120U are especially designed for LC-circuits, but the input can also be used with a ceramic filter.

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	12 V
Supply current	I_P	typ.	13,5 mA
I.F. voltage gain at f = 5,5 MHz	$G_{v\ if}$	typ.	68 dB
Input voltage starting limiting	V_i	typ.	30 μV
AM suppression at $\Delta f = \pm 50$ kHz	α	typ.	60 dB
A.F. output voltage adjustment range (pin 8)	$\Delta V_{o\ af}$	typ.	85 dB
A.F. output voltage at $\Delta f = \pm 50$ kHz (r.m.s. value)			
at pin 8	$V_{o\ af(rms)}$	typ.	1,2 V
at pin 12	$V_{o\ af(rms)}$	typ.	1,0 V

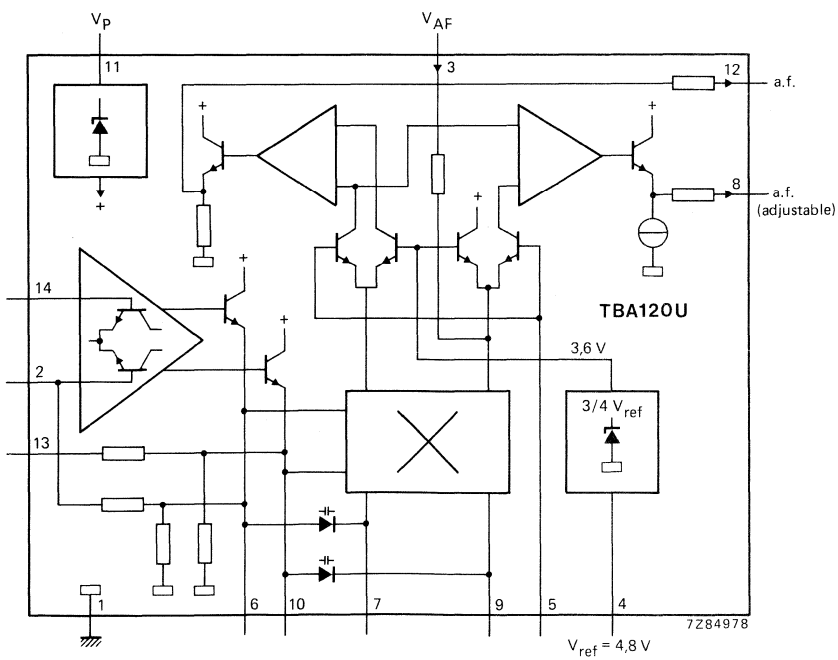


Fig. 1 Block diagram.

PACKAGE OUTLINE

14-lead DIL; plastic (SOT-27K, M, T).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11-1}$	max.	18	V*
Adjustment voltage (pin 5)	V_{5-1}	max.	6	V
Total power dissipation	P_{tot}	max.	400	mW
By-pass resistance	R_{13-14}	max.	1	kΩ
Storage temperature range	T_{stg}		−40 to + 125	°C
→ Operating ambient temperature range	T_{amb}		0 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; f = 5,5 MHz

I.F. voltage gain	$G_{v\ if\ 6-14}$	typ.	68	dB
Input voltage starting limiting at Δf = ± 50 kHz; f_m = 1 kHz	V_i	typ. <	30 60	μV μV
I.F. output voltage at limiting (peak-to-peak value)	$V_{o\ if\ (p-p)}$	typ.	250	mV
AM suppression at Δf = ± 50 kHz; V_i = 500 μV; f_m = 1 kHz; m = 30%	α	> typ.	50 60	dB dB
I.F. residual voltage without de-emphasis				
at pin 12	$V_{if\ 12}$	typ.	30	mV
at pin 8	$V_{if\ 8}$	typ.	20	mV
A.F. voltage gain	$G_{v\ af\ 8-3}$	typ.	7,5	
A.F. adjustment at R_{4-5} = 5 kΩ; R_{5-1} = 13 kΩ	$\Delta V_{o\ af}$	 typ.	20 to 36 28	dB dB
A.F. output voltage control range	$\Delta V_{o\ af}$	> typ.	70 85	dB dB
Adjustment resistor**	R_{4-5}		1 to 10	kΩ
D.C. voltage portion at the a.f. outputs				
pin 12	V_{12-1}	typ.	5,6	V
pin 8	V_{8-1}	typ.	4,0	V
Output resistance of the a.f. outputs				
pin 12	$R_{o\ 12-1}$	typ.	1,1	kΩ
pin 8	$R_{o\ 8-1}$	typ.	1,1	kΩ
Input resistance of the a.f. input	$R_{i\ 3-1}$	typ.	2	kΩ
Stabilized reference voltage	$V_{4-1} = V_{ref}$	 typ.	4,2 to 5,3 4,8	V V
Source resistance of reference voltage source	R_{4-1}	typ.	12	Ω

* Supply voltage operating range is 10 to 18 V.

** Pin 5 must be connected to pin 4, when volume control adjustment is not applicable.

Hum suppression			
at pin 12	V_{12}/V_{11}	typ.	30 dB
at pin 8	V_8/V_{11}	typ.	35 dB
Supply current (pin 11)	$I_P = I_{11}$		9,5 to 17,5 mA
		typ.	13,5 mA
I.F. input impedance	$\|Z_i\|$	typ.	40 kΩ/4,5 pF
		>	15 kΩ/< 6 pF
A.F. output voltage at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 45$; r.m.s. value			
at pin 12	$V_{o\,af\,(rms)}$	typ.	1,0 V
at pin 8	$V_{o\,af\,(rms)}$	typ.	1,2 V
Distortion at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 20$	d_{tot}	typ.	1 %

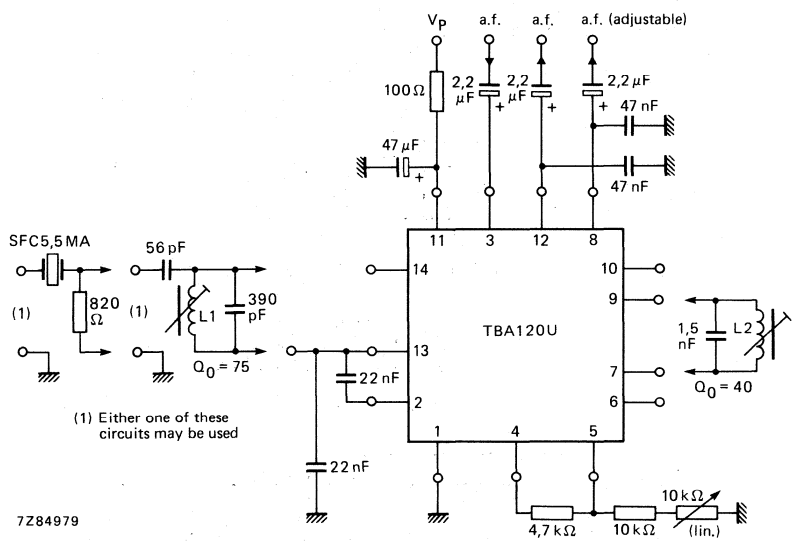


Fig. 2 Application example using TBA120U.

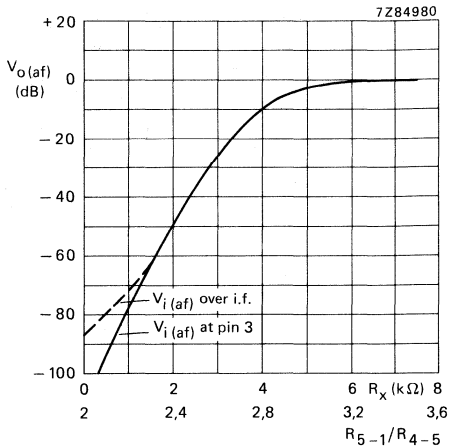


Fig. 3 The a.f. output voltage at pin 8 as a function of the resistance values as shown in Fig. 4.

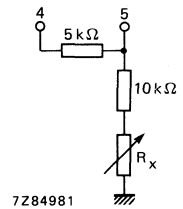
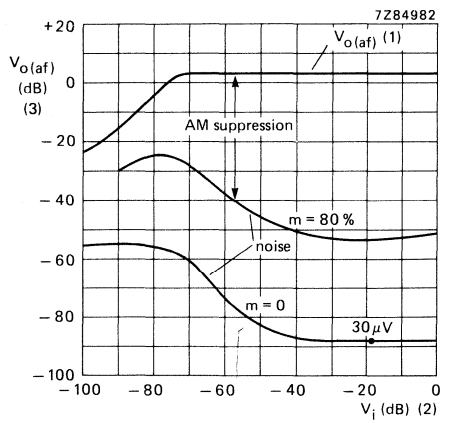


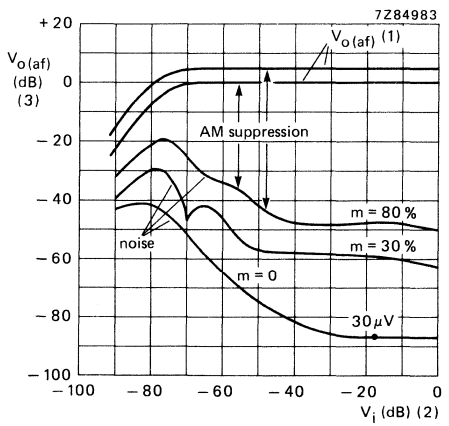
Fig. 4 Resistor conditions for curves in Fig. 3.



(1) $V_{o\,af}$ with de-emphasis at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $d_{tot} = 1{,}5\%$; 0 dB ≙ 770 mV.

(2) V_i: 0 dB ≙ 200 mV at 60 Ω.

Fig. 5 The a.f. output voltage at pin 8 as a function of the input voltage with SFC 5,5 MA at the input (see Fig. 2).



(1) $V_{o\,af}$ with de-emphasis at $f_m = 1$ kHz; 0 dB ≙ 770 mV;
curve a: $\Delta f = \pm 50$ kHz; $d_{tot} = 3\%$;
curve b: $\Delta f = \pm 25$ kHz; $d_{tot} = 1\%$.

(2) V_i: 0 dB ≙ 200 mV at pin 14.

Fig. 6 The a.f. output voltage at pin 8 as a function of the input voltage with broadband input (60 Ω).

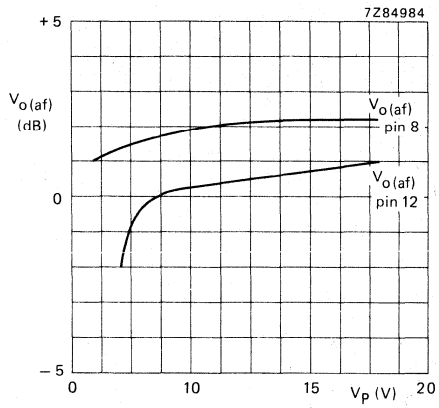


Fig. 7 The a.f. output voltages at pins 8 and 1 as a function of the supply voltage; 0 dB ≙ 770 mV.

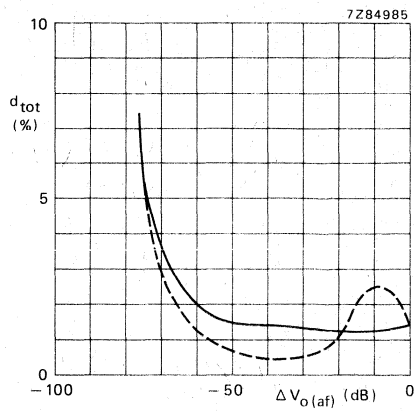


Fig. 8 Total distortion as a function of the a.f. output voltage change.
——— 0 dB ≙ 900 mV over i.f. (pin 8)
– – – – 0 dB ≙ 1,15 V (pin 8)

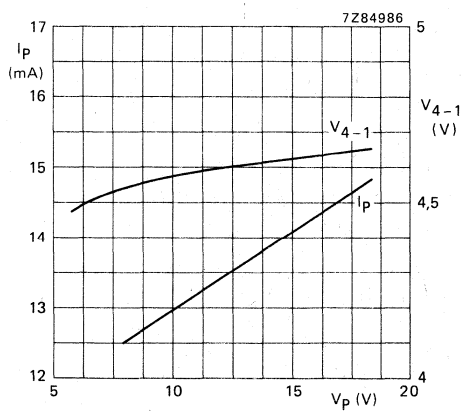


Fig. 9 Supply current and the reference voltage at pin 4 as a function of supply voltage.

HORIZONTAL COMBINATION

The TBA920 is a monolithic integrated circuit intended for television receivers with transistor, thyristor, or tube-equipped output stages.
It combines the following functions:
- noise gated sync separator
- line oscillator
- phase comparison between sync pulse and oscillator
- loop gain and time constant switching (also for video recorder applications)
- phase comparison between line-flyback pulse and oscillator
- output stage for drive a variety of line output stages

QUICK REFERENCE DATA

Supply voltage	V_{1-16}	nom.	12 V
Ambient temperature	T_{amb}		25 °C
Input signals			
Video input voltage (positive-going sync) top sync to white value	$V_{8-16(p-p)}$	typ.	3 V 1 to 7 V
Noise gate input current (peak value)	I_{9M}	>	30 μA
Input resistance of noise gate	R_{9-16}	typ.	200 Ω
Flyback signal input voltage (peak value)	V_{5-16M}	typ.	±1 V
Flyback signal input current (peak value)	I_{5M}	typ.	1 mA
Output signals			
Line driver output voltage (peak-to-peak value)	$V_{2-16(p-p)}$	typ.	10 V
Line driver output current (average value)	$I_{2(AV)}$	max.	20 mA
Line driver output current (peak value)	I_{2M}	max.	200 mA
Composite sync output voltage (peak value)	V_{7-16M}	typ.	10 V

PACKAGE OUTLINE

16-lead dual in-line; plastic (SOT-38).

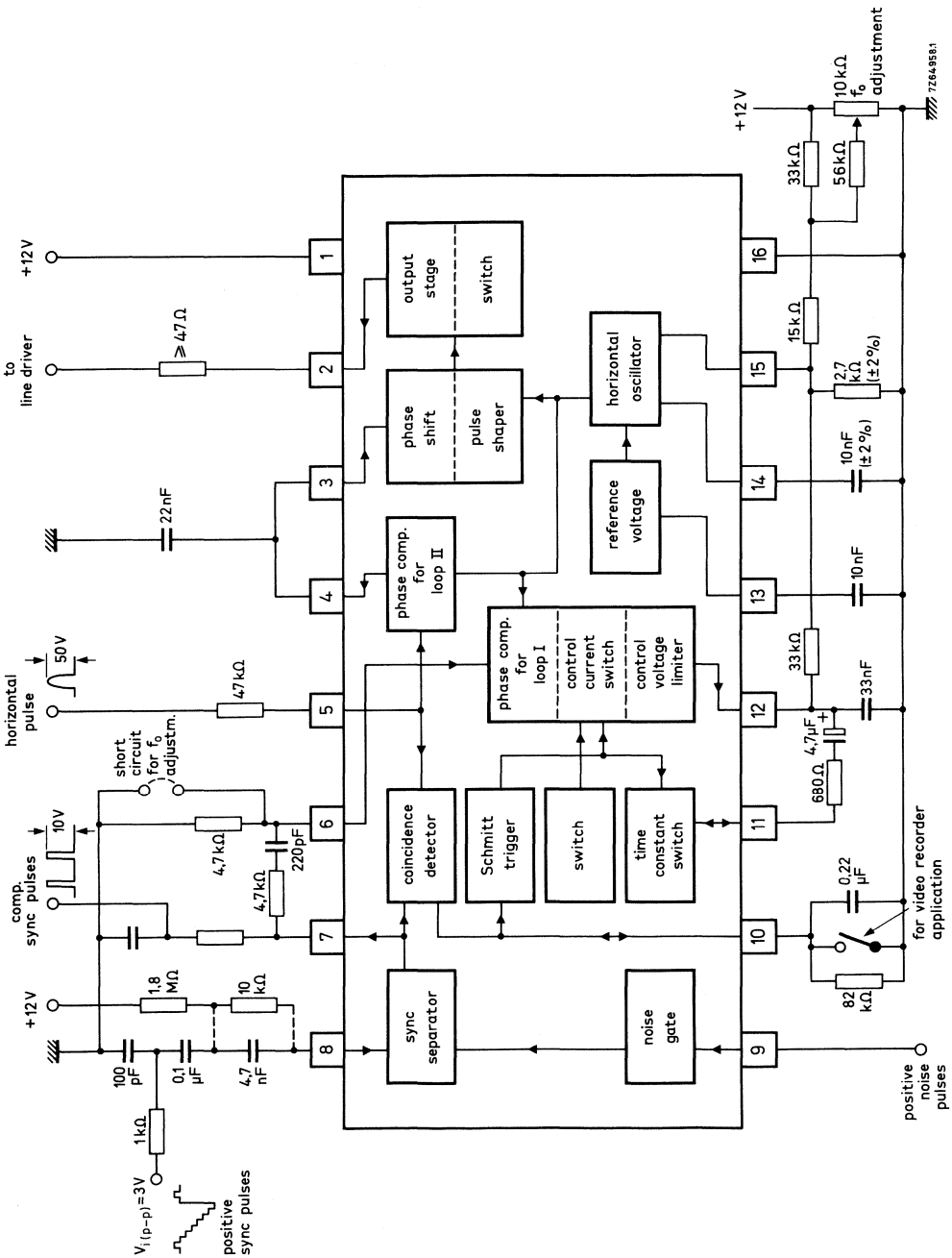


Fig. 1 Block diagram and application information.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (Vp)	V_{1-16}	max.	13,2 V
Phase shift voltage	V_{3-16}		0 to 13,2 V
Video input voltage	$-V_{8-16}$	max.	12 V
Coincidence detector voltage	V_{10-16}		−0,5 to +5 V
Line driver output current (average value)	$I_{2(AV)}$	max.	20 mA
(peak value)	I_{2M}	max.	200 mA
Horizontal pulse current (peak value)	I_{5M}	max.	10 mA
Composite sync current (peak value)	I_{7M}	max.	10 mA
Pos. sync pulse current (peak value)	I_{8M}	max.	10 mA
Noise gate current (peak value)	I_{9M}	max.	10 mA
Total power dissipation	P_{tot}	max.	600 mW*
Storage temperature	T_{stg}		−55 to +125 °C
Operating ambient temperature	T_{amb}		0 to + 70 °C ←

CHARACTERISTICS

At V_{1-16} = 12 V; T_{amb} = 25 °C. Measured in circuit of Fig. 1 (CCIR standard).

Current consumption at $I_2 = 0$	I_1	typ.	36 mA

Required input signals

Video signal

Input voltage (positive going sync) peak-to-peak value	$V_{i(p-p)}$	typ.	3 V 1 to 7 V
Input current during sync pulse (peak value)	I_{8M}	typ.	100 μA

Noise gating (pin 9)

Input voltage (peak value)	V_{9-16M}	>	0,7 V
Input current (peak value)	I_{9M}	> <	30 μA 10 mA
Input resistance	R_{9-16}	typ.	200 Ω

Flyback pulse (pin 5)

Input voltage (peak value)	V_{5-16M}	typ.	±1 V
Input current (peak value)	I_{5M}	> typ.	50 μA 1 mA
Input resistance	R_{5-16}	typ.	400 Ω
Pulse duration at 15 625 Hz	t_5	>	10 μs

* 800 mW permissible while tubes are heating up.

CHARACTERISTICS (continued)

Delivered output signals

Composite sync pulses (positive; pin 7)			
Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	typ.	10 V
Output resistance			
at leading edge of pulse (emitter follower)	$R_{7\text{-}16}$	$\approx$	50 Ω
at trailing edge	$R_{7\text{-}16}$	typ.	2,2 kΩ
Additional external load resistance	$R_{7\text{-}16(ext)}$	$>$	2 kΩ
Driver pulse (pin 2)			
Output voltage (peak-to-peak value)	$V_{2\text{-}16(p\text{-}p)}$	typ.	10 V
Average output current	$I_{2(AV)}$	$<$	20 mA
Peak output current	I_{2M}	$<$	200 mA
Output resistance (low ohmic)	$R_{2\text{-}16}$	typ.	2,5 or 15 Ω *
Output pulse duration when synchronized	t_2		12 to 32 μs **
Permissible delay between leading edge of output pulse and flyback pulse at t_5 = 12 μs	$t_{o\ tot}$		0 to 15 μs
Supply voltage at which output pulses are obtained	$V_{1\text{-}16}$	$>$	4 V

* Depends on switch position and polarity output current. $R_{2\text{-}16}$ = 2,5 Ω is valid for $V_{2\text{-}16}$ = +10,5 V and a load between pins 2 and 16 (e.g. an external resistor).

** The output pulse duration is adjusted by shifting the leading edge ($V_{3\text{-}16}$ from 6 V to 8 V). The pulse duration is a result of delay in the line output device and the action of the second control loop in the TBA920S.
For a line output stage with a BU108 high-voltage transistor the resulting duration is about 22 μs, and in such a way that the line output transistor is switched on again about 8 μs after the middle of the line-flyback pulse. This pulse duration must be taken into account when designing the driver stage and driver transformer as this way of driving the line output device differs from the usual, i.e. a driver duty cycle of about 50%.

Oscillator

Frequency; free running (R_{15-16} = 3,3 kΩ)	f_o		15 625 Hz	*
Spread of frequency at R_{15-16} = 3,3 kΩ; C_{14-16} = 10 nF	$\frac{\Delta f_o}{f_o}$	<	1,5 %	**
Frequency change when decreasing the supply down to minimum 4 V	$\left\lvert\frac{\Delta f_o}{f_o}\right\rvert$	<	10 %	
Frequency control sensitivity	$\frac{\Delta f_o}{\Delta I_{15}}$	typ.	16,5 Hz/μA	
Adjustment range of frequency (in Fig. 2)	$\frac{\Delta f_o}{f_o}$	typ.	±5 %	
Influence of supply voltage on frequency at V_P = 12 V	$\frac{\delta f_o}{f_o} / \frac{\delta V_P}{V_{Pnom}}$	<	5 %	
Control loop 1 (between sync pulse and oscillator)				
Control voltage range	V_{12-16}		0,8 to 5,5 V	
Control current (peak values)				
at $V_{10-16} > 4{,}5$ V; $V_{6-16} > 1{,}5$ V	I_{12M}	typ.	±2 mA	
at $V_{10-16} < 2$ V; $V_{6-16} > 1{,}5$ V	I_{12M}	typ.	±6 mA	
Loopgain of APC system				
a. Time coincidence between sync pulse and flyback pulse or $V_{10-16} > 4{,}5$ V	$\frac{\Delta f}{\Delta t}$	typ.	1 kHz/μs	
b. No time coincidence or $V_{10-16} < 2$ V	$\frac{\Delta f}{\Delta t}$	typ.	3 kHz/μs	
Catching and holding range	Δf	typ.	±1 kHz ▲	

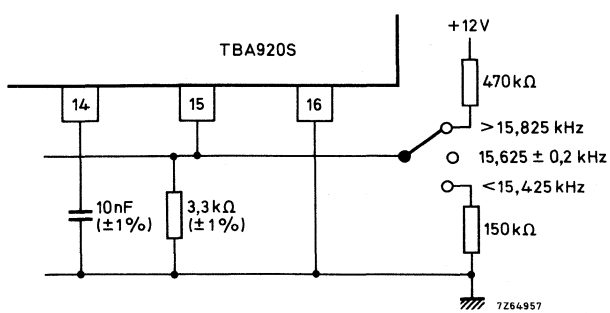


Fig. 2 Possibilities for oscillator frequency adjustment.

* The oscillator frequency can be changed for other TV standards by an appropriate value of C_{14-16}.

** Exclusive external components tolerances.

▲ Adjustable with R_{12-15}.

CHARACTERISTICS (continued)

Pull-in time for $\Delta f/f_o = \pm 3\% (\Delta f = 470$ Hz)	t	$\approx$	20	ms	(note 1)
Switch-over from large control sensitivity to small control sensitivity after catching	t	$\approx$	20	ms	(note 1)
Control loop II (between flyback pulse and oscillator)					
Permissible delay between leading edge of output pulse (pin 2) and leading edge of flyback pulse	$t_{d\ tot}$		0 to 15	μs	
Static control error	$\frac{\Delta t}{\Delta t_d}$	$<$	0,5	%	(note 2)
Output current during flyback pulse (peak value)	I_{4M}	typ.	$\pm$0,7	mA	
Overall phase relation					
Phase relation between leading edge of sync pulse and middle of flyback pulse	t	typ.	4,9	μs	(note 3)
Tolerance of phase relation	$\lvert\Delta t\rvert$	$<$	0,4	μs	(note 4)
Voltage for $T_2 = 12$ to 32 μs	$V_{3\text{-}16}$		6 to 8	V	
Adjustment sensitivity	$\frac{\Delta T_2}{\Delta V_{3\text{-}16}}$	typ.	10	μs/V	
Input current	I_3	$<$	2	μA	

External switch-over of parameters (loop filter and loop gain) of control loop I (e.g. for video recorder application) see note 5.

Required switch-over voltage					
at $R_{11\text{-}16} = 150\ \Omega$	$V_{10\text{-}16}$	$>$	4,5	V	
at $R_{11\text{-}16} = 2$ kΩ	$V_{10\text{-}16}$	$<$	2	V	
Required switch-over current					
at $R_{11\text{-}16} = 150\ \Omega$; $V_{10\text{-}16} = 4,5$ V	I_{10}	typ.	80	μA	(note 5)
at $R_{11\text{-}16} = 2$ kΩ; $V_{10\text{-}16} = 2$ V	I_{10}	typ.	120	μA	

1. See Fig. 1.
2. The control error is the remaining error in reference to the nominal phase position between leading edge of the sync pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.
3. This phase relation assumes a luminance delay line with a delay of 500 ns between the input of the sync separator and the drive to the picuture tube. If the sync separator is inserted after the luminance delay line or if there is no delay line at all (black-and-white sets), then the phase relation is achieved at $C_{5\text{-}16} = 560$ pF.
4. The adjustment of the overall phase relation and consequently the leading edge of the output pulse at pin 2 occurs automatically by the control loop II or by applying a d.c. voltage to pin 3.
5. With sync pulses at pin 7 and 8; without RC network at pin 10.

CHROMINANCE AMPLIFIER FOR SECAM OR PAL/SECAM DECODERS

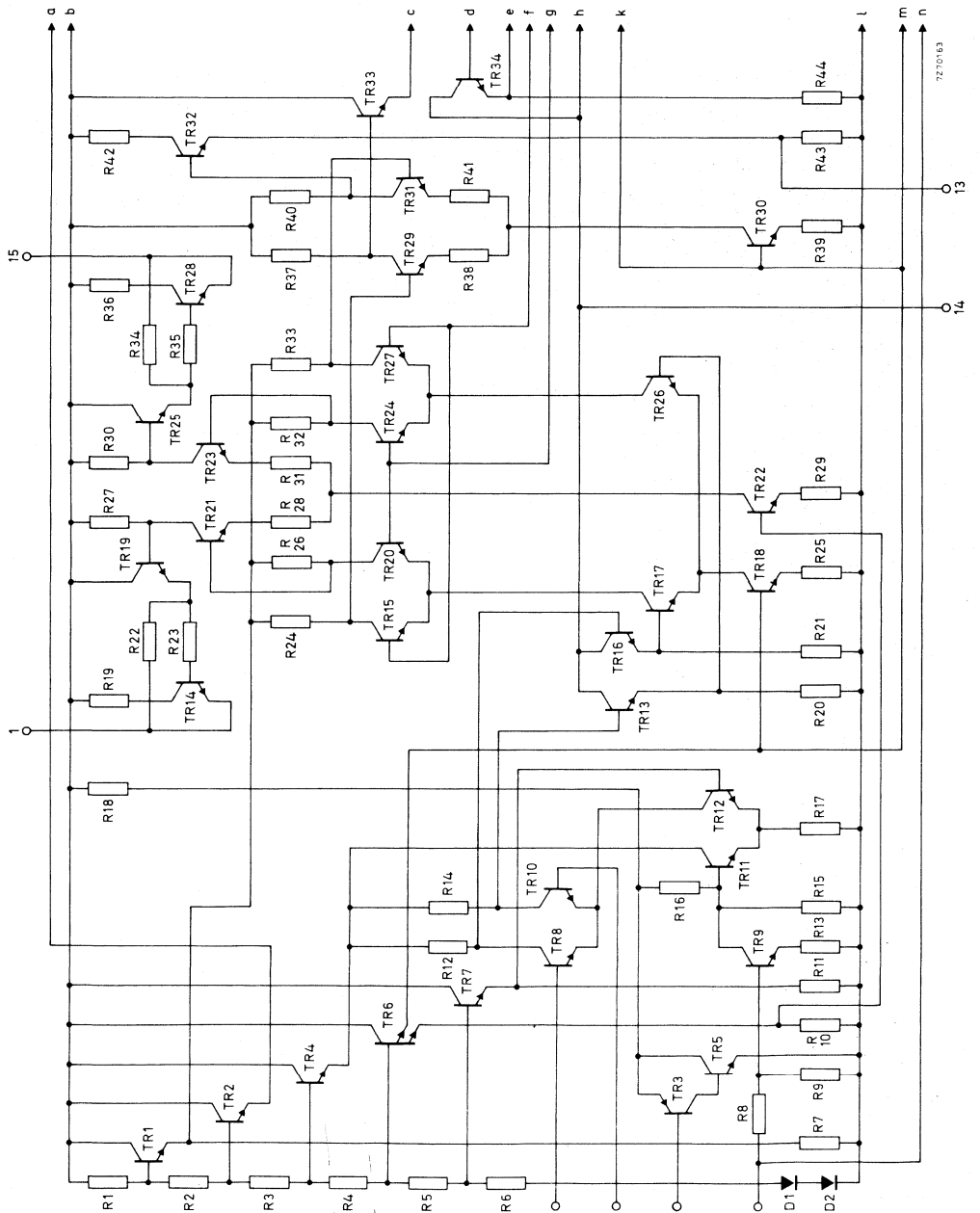
The TCA640 is an integrated chrominance amplifier for either a SECAM decoder or a double standard PAL/SECAM decoder.
Switching of the standard is performed internally, controlled by an external applied d.c. signal.
In addition to the chrominance amplifier the circuit also incorporates a 7,8 kHz flip-flop and an identification circuit for SECAM.
For PAL identification the circuit included in the TBA540 should be used.
Furthermore, the TCA640 incorporates a blanking circuit, a burst gating circuit and a colour killer detector.

QUICK REFERENCE DATA

Supply voltage			V_{14-2}	nom. 12	V
Supply current			I_{14}	nom. 37	mA
			PAL	SECAM	
Chrominance input signals (peak-to-peak value)	$V_{3-5(p-p)}$	>	4	7	mV
		<	80	400	mV
Chrominance output signals (peak-to-peak value)	$V_{15-2\ (p-p)}$ / $V_{1-2\ (p-p)}$	typ.	500	2000	mV
Burst output (closed a.c.c. loop) (peak-to-peak value)	$V_{13-2(p-p)}$	typ.	1	–	V
System switching signal	V_{4-2}	typ.	12	0	V
Burst blanking of chrominance signal		>	40	–	dB
Chrominance blanking at field identification		>	–	40	dB
Square-wave output (7,8 kHz) (peak-to-peak value)	$V_{12-2(p-p)}$	typ.	3	3	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).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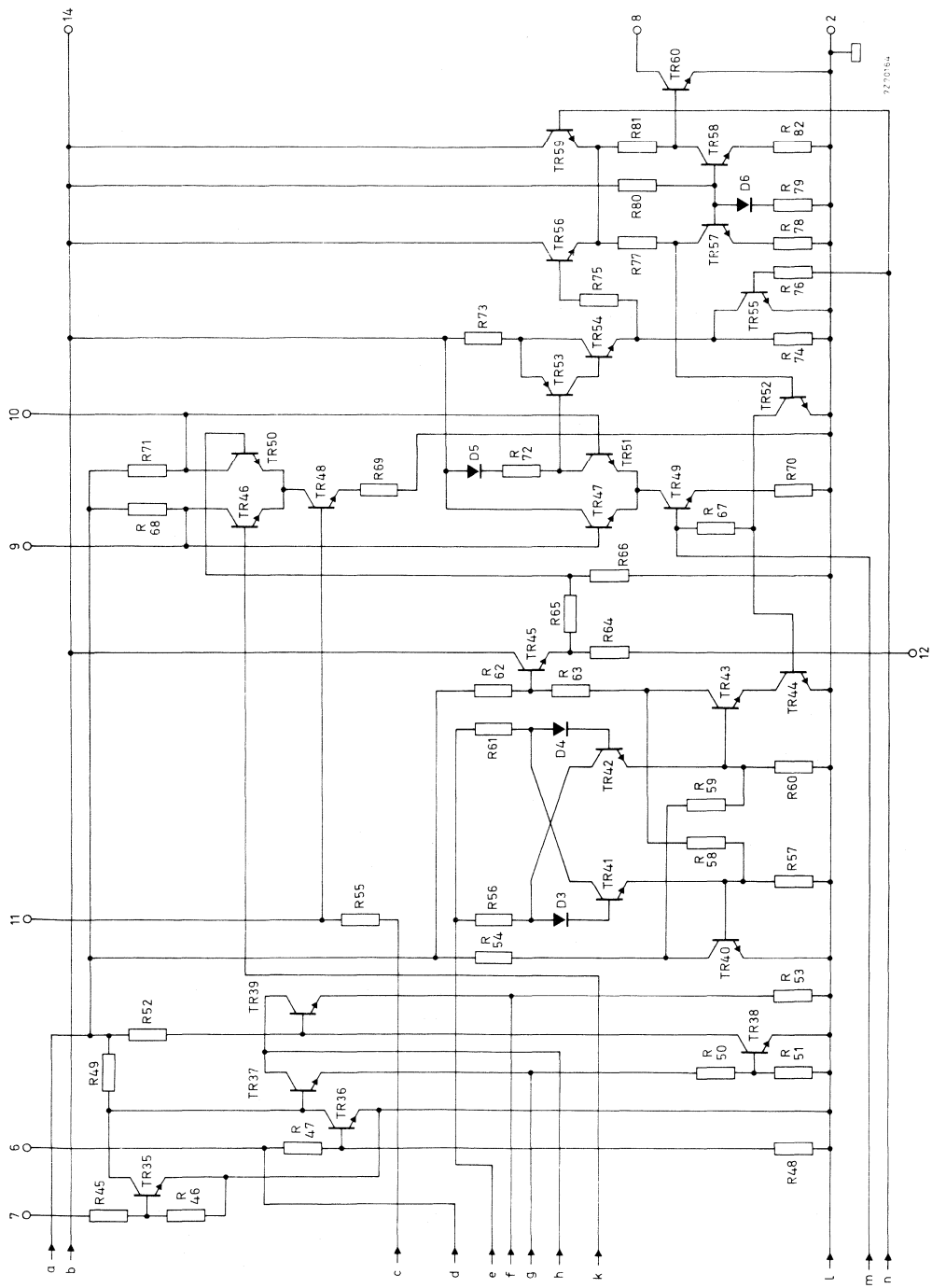
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RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage			
Supply voltage	V_{14-2}	max.	13,2 V
Power dissipation			
Total power dissipation	P_{tot}	max.	625 mW
Temperatures			
Storage temperature	T_{stg}		−25 to +125 °C
Operating ambient temperature	T_{amb}		−25 to +65 °C [1]

CHARACTERISTICS measured in the circuit on page 6

Supply voltage	V_{14-2}	typ.	12 V
			10,2 to 13,2 V
Required input signals at V_{14-2} = 12 V and T_{amb} = 25 °C			
Chrominance input signal			
peak-to-peak value	$V_{3-5(p-p)}$	PAL	4 to 80 mV
		SECAM	7 [2] to 400 mV
Automatic chrominance control starting	V_{16-2}	PAL typ.	1,2 V [3]
Flyback pulses for blanking and burst/identification lines-keying			See note 4
Line flyback pulses (positive)			
peak-to-peak value	$V_{6-2(p-p)}$		4,5 to 12 V
Field idenfication pulses (positive)			
peak-to-peak value	$V_{7-2(p-p)}$		4 to 12 V
System switch signal	V_{4-2}	PAL	7 to V_{14-2} V
		SECAM	0 to 1 V
Colour killer threshold	V_{16-2}	PAL typ.	2,5 V [5]

[1]) When a stabilized power supply of ⩽12 V is applied, T_{amb} is max. 75 °C.

[2]) Start of limiting.

[3]) A negative-going potential provides a 26 dB a.c.c. range.

[4]) The line flyback pulses also provide the clock pulses for the flip-flop.

[5]) The colour killer is operative above the quoted input voltage.

CHARACTERISTICS (continued)

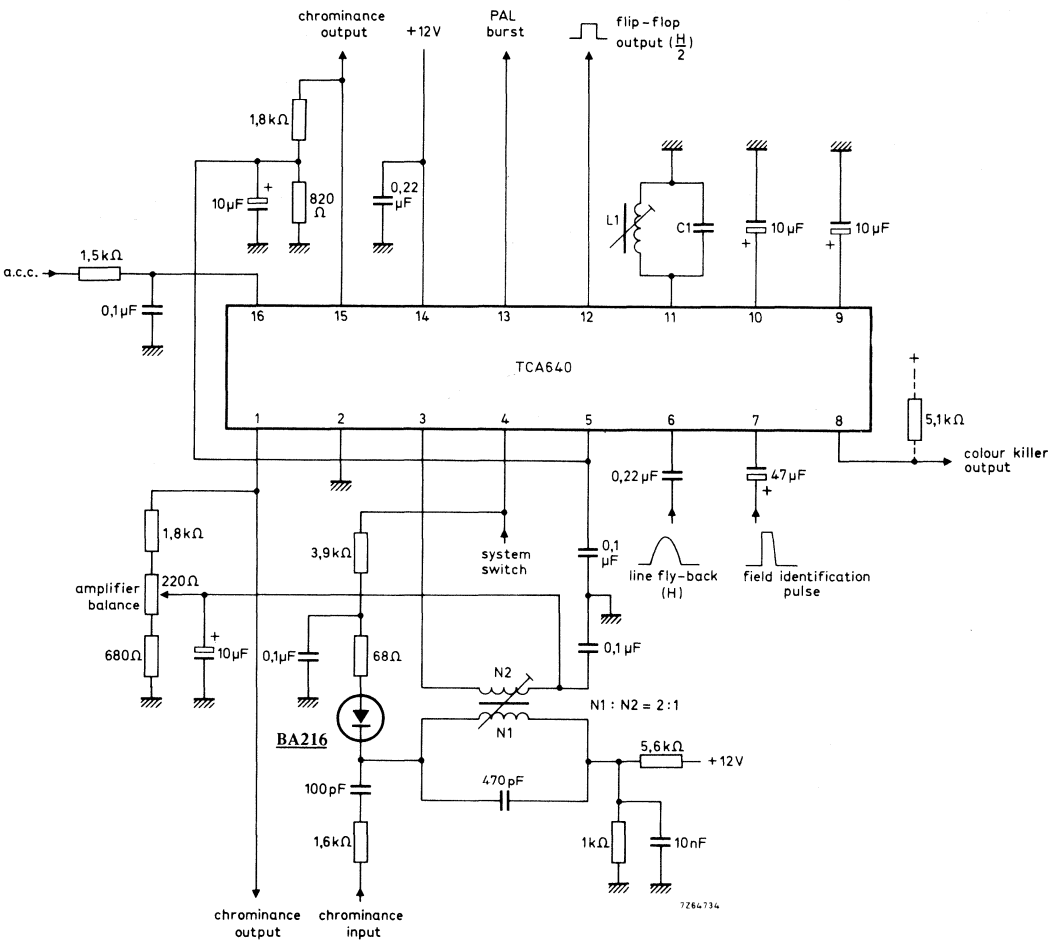
Obtainable output signals

Chrominance output signals						
peak-to-peak value		$V_{15-2(p-p)}$	PAL		425 to 575	mV
		$V_{1-2(p-p)}$	SECAM		1,8 to 2,3	V
Phase difference between output pins		$\Delta\varphi$ 15-1	PAL		170° to 190°	[1]
Burst signal (peak-to-peak value)		$V_{13-2(p-p)}$	PAL	typ.	1	[2]
Identification signal						
peak-to-peak value		$I_{11(p-p)}$	SECAM		1,4 to 2,4	mA
Output resistance		R_{11-2}			2 to 2,9	kΩ
Flip-flop signal						
peak-to-peak value		$V_{12-2(p-p)}$			2,5 to 3,5	V
Colour killer	killed	V_{8-2}		<	0,5	V
		I_8		<	10	mA
	unkilled	V_{8-2}			V_{14-2}	V
		I_8		<	10	μA
Bandwidth of chrominance amplifier (−1 dB)						
at a carrier frequency of 4,2 MHz				>	± 1	MHz
Blanking						
burst rejection			PAL	>	40	dB
rejection identification lines with field identification			SECAM	>	40	dB

1) Over the a.c.c. control range the phase difference varies less than 2,5°.

2) The burst is kept constant at 1 V peak-to-peak by automatic gain control.

APPLICATION INFORMATION



Pinning

1. Chrominance output
2. Earth (negative supply)
3. Chrominance input
4. System switch input
5. Chrominance input
6. Line fly-back pulse input
7. Field identification pulse input
8. Colour killer output
9. Identification integrating
10. capacitor (SECAM)
11. Identification tank circuit (SECAM)
12. Flip-flop output
13. Burst output (PAL)
14. Supply voltage (12 V)
15. Chrominance output
16. A.C.C. input

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Chrominance output (in conjunction with pin 15)

   A balanced output is available at pins 1 and 15.
   At SECAM reception a limited signal of 2 V peak-to-peak is available, starting from an input voltage of 15 mV peak-to-peak.
   At PAL reception the output signal is 500 mV peak-to-peak for a burst signal of 1 V peak-to-peak.
   An external d.c. network is required which provides negative feedback to pin 3. The same holds for the feedback from pin 15 to pin 5.
   The figures for input and output signals are based on a 100% saturated colour bar signal.

2. Negative supply (earth)

3. Chrominance input (in conjunction with pin 5)

   The input signal is derived from a bandpass filter which provides the required "bell" shape bandpass for the SECAM signal and a flat bandpass for the PAL signal.
   The input signal can be supplied either in a balanced mode or single ended. Both inputs (pins 3 and 5) require a d.c. potential of about 2,5 V obtained from a resistive divider connected to output pins 1 and 15. The figures for the input signals are based on a 100% saturated colour bar signal and a burst-to-chrominance ratio of 1:3 of the input signal (PAL).

4. System switch input

   Between 7 V and the supply voltage, the gain of the chrominance amplifier is controlled by the a.c.c. voltage at pin 16.
   The chrominance amplifier then provides linear amplification required for the PAL signal.
   Between 0 V and 1 V the chrominance amplifier operates as a limiter for the SECAM signal.

5. Chrominance input (see pin 3)

6. Line fly-back pulse input (in conjunction with pin 11)

   Positive going pulses provide

   - blanking of the chrominance signal at the outputs (pins 1 and 15).
   - burst gating for both PAL and SECAM.
     The carrier signal present during the second half of the back porch of the SECAM signal is gated. It provides line identification when the circuit L_1C_1 (see circuit on page 6) is tuned to 4,25 MHz (at C_1 = 470 pF).
   - trigger signal for the flip-flop.

7. Field identification pulse input (in conjunction with pin 11)

   Like the line fly-back pulses, positive going identification pulses provide blanking and burst gating.
   To operate the TCA640 on the identification lines (SECAM) in the field blanking period the circuit L_1C_1 (see circuit on page 6) should be tuned to 3,9 MHz and the capacitor C_1 should be increased to 1 nF. The field fly-back pulse should be shaped so that its amplitude exceeds 4 V during the identification lines.

APPLICATION INFORMATION (continued)

8. Colour killer output

   This pin is driven from the collector of an internal switching transistor and requires an external load resistor connected to the supply voltage. The killer is operative when the a.c.c. voltage exceeds the threshold, when the SECAM chrominance signal at the input is below the limiting level or when the flip-flop operates in the wrong phase.

9. Identification integrating capacitor (SECAM)

10. Identification integrating capacitor (SECAM)

11. Identification detector tank circuit (see pins 6 and 7)

12. Flip-flop output

    A square wave of 7,8 kHz with an amplitude of 3 V is available at this pin.
    An external load resistor is not required.

13. Burst output (PAL)

    A 1 V peak-to-peak burst (kept constant by the a.c.c. system) is produced here.

14. Supply voltage (12 V)

    Correct operation occurs within the range 10,2 to 13,2 V.
    The power dissipation must not exceed 625 mW at 65 °C ambient temperature.

15. Chrominance output (see pin 1)

16. A.C.C. input

    With the system switch input (pin 4) connected for PAL operation, a negative going potential gives a 26 dB range of a.c.c. starting at + 1,2 V
    During SECAM operation, the voltage at the input should not exceed +0,5 V, otherwise the SECAM identification circuit and the colour killer become inoperative.

CHROMINANCE DEMODULATOR FOR SECAM OR PAL/SECAM DECODERS

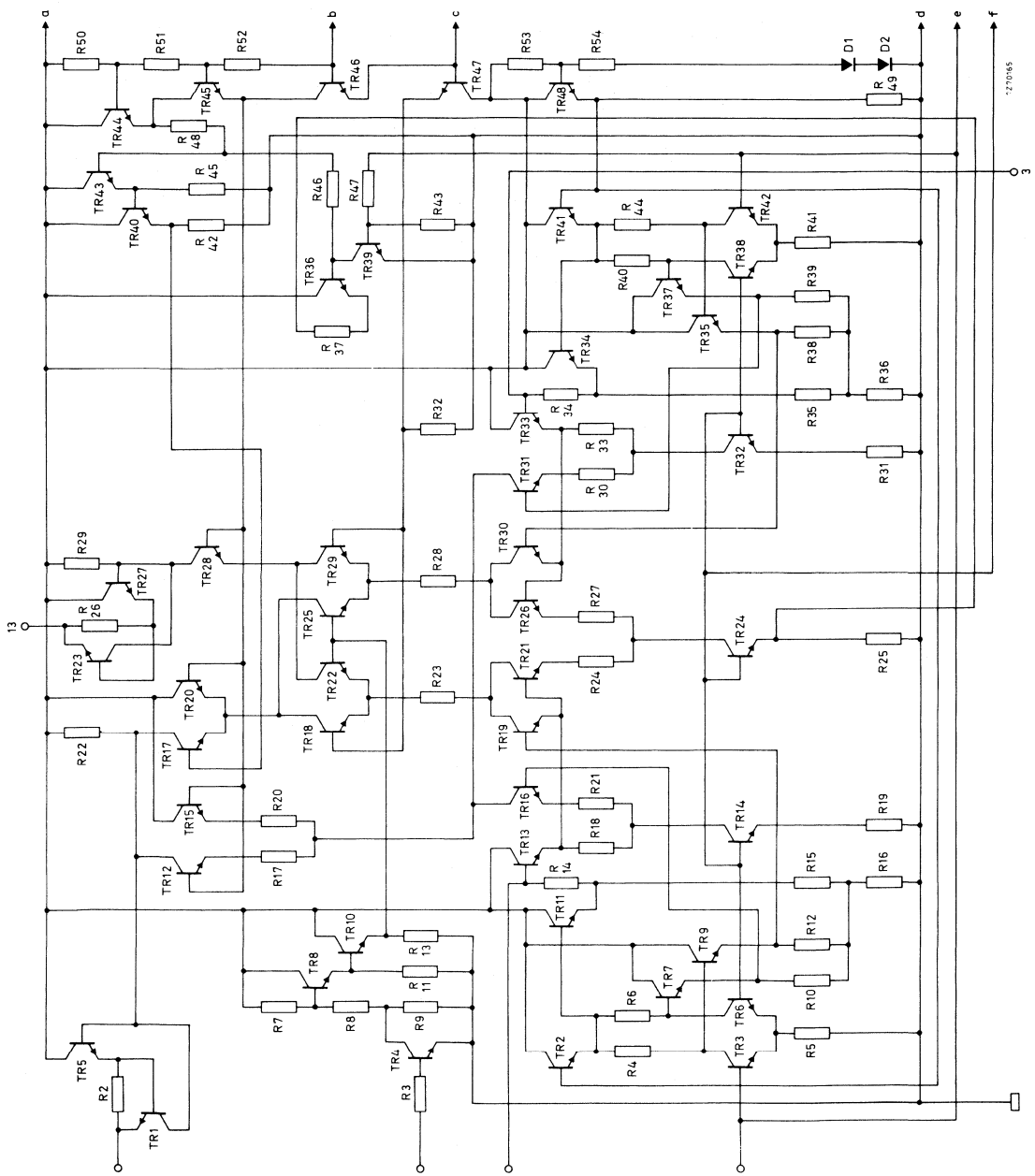
The TCA650 is an integrated synchronous demodulator for both the SECAM and PAL chrominance signals.
Switching of the standard is performed internally, controlled by an external applied d.c. signal.
In addition to the synchronous demodulator, which delivers colour difference signals, the circuit also incorporates:

- a PAL matrix, used for adding the delayed and non-delayed signals to obtain separately the (R-Y) and (B-Y) components of the chrominance signal.
- a PAL switch, which reverses the phase of the (R-Y) component of the chrominance signal on alternating lines.
- a SECAM switch, which performs the separation of the D_R and D_B components of the chrominance signal by switching the delayed and non-delayed signals.
- a SECAM limiter.

QUICK REFERENCE DATA						
Supply voltage		V_{14-2}	nom.	12		V
Supply current		I_{14}	nom.	36		mA
				PAL	SECAM	
Chrominance input signals (peak-to-peak value)	$V_{1-2(p-p)}$ / $V_{3-2(p-p)}$		typ.	50	200	mV
System switch input	V_{4-2}		typ.	12	0	V
Colour difference output signals (peak-to-peak value)	(R-Y):	$V_{12-2(p-p)}$	typ.	1,1		V
	(B-Y):	$V_{10-2(p-p)}$	typ.	1,47		V
Reference input signals (PAL) (peak-to-peak value)		$V_{6-2(p-p)}$ / $V_{7-2(p-p)}$	typ.	1		V
Square-wave input (peak-to-peak value)		$V_{16-2(p-p)}$	typ.	3		V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).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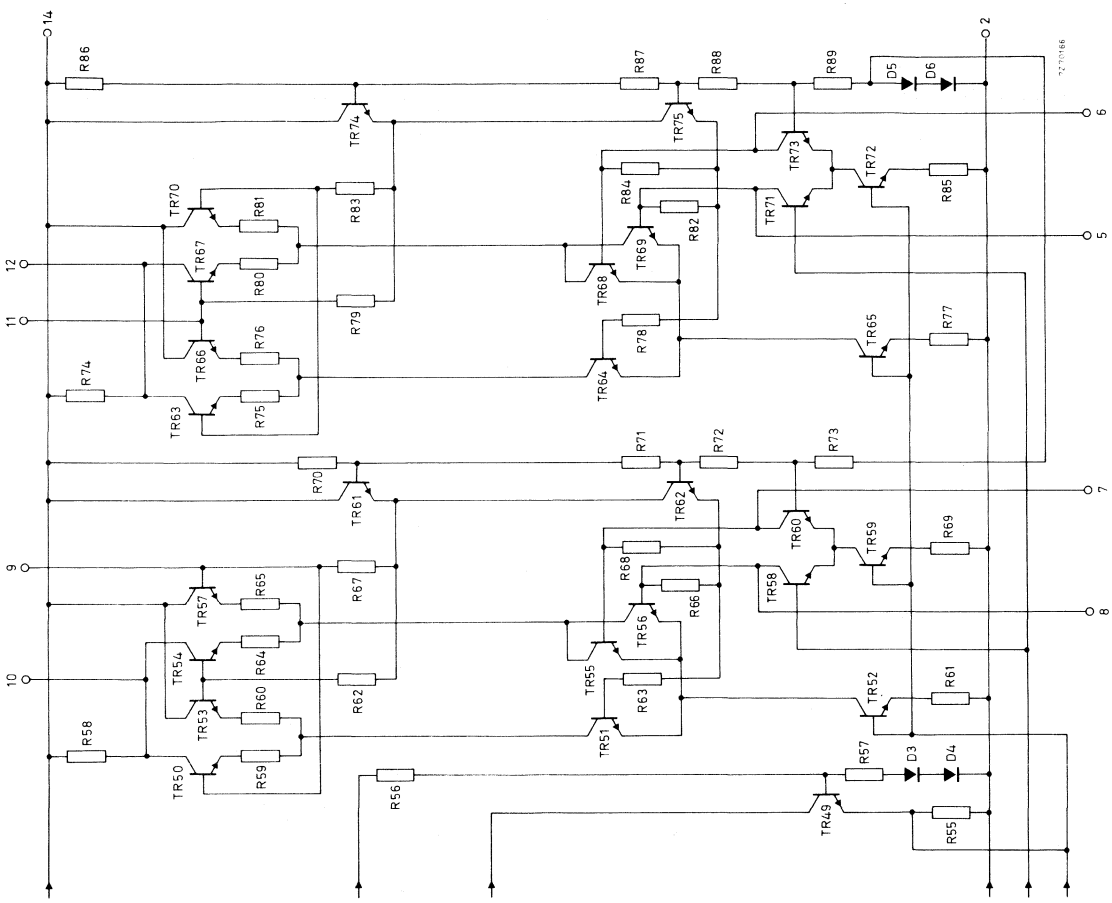
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RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage	V_{14-2}		max. 13,2	V
Power dissipation				
Total power dissipation	P_{tot}		max. 510	mW
Temperatures				
Storage temperature	T_{stg}		−25 to +125	°C
Operating ambient temperature	T_{amb}		−25 to +65	°C [1]

CHARACTERISTICS measured in the circuit on page 6

Supply voltage	V_{14-2}		typ. 12 10,2 to 13,2	V V
Required input signals at V_{14-2} = 12 V and T_{amb} = 25 °C				
Chrominance input signal				
peak-to-peak value	$V_{1-2(p-p)}$	PAL	35 to 75	mV
	$V_{3-2(p-p)}$	SECAM	150 to 400	mV
Input impedance	$\lvert Z_{1-2}\rvert$ $\lvert Z_{3-2}\rvert$		1,2 to 2,6	kΩ
PAL matrix				
Gain from both inputs to pin 13			2,3 to 3,3	
Gain from both inputs to pin 15			2,6 to 3,6	
Gain difference from line-to-line			< 5	%
Phase errors from line-to-line in the (R-Y) output for zero error in the (B-Y) output			< 2,5°	
Output impedance	$\lvert Z_{13-2}\rvert$ $\lvert Z_{15-2}\rvert$		< 100	Ω
SECAM permutator				
Diaphotie			< −46	dB
Output signal (peak-to-peak value)	$V_{13-2(p-p)}$ $V_{15-2(p-p)}$		1,6 [2] to 2,2	V
Output impedance	$\lvert Z_{13-2}\rvert$ $\lvert Z_{15-2}\rvert$		< 100	Ω

[1] When a stabilized power supply of ≤ 12 V is applied, T_{amb} is max. 75 °C.

[2] At an input voltage of 0,15 V; at an input voltage > 0,2 V the figure is 1,7 V.

CHARACTERISTICS (continued)

Demodulator

Chrominance input signal amplitude

PAL: (B-Y); peak-to-peak value	$V_{9-2(p-p)}$	typ.	0,22	V
(R-Y); peak-to-peak value	$V_{11-2(p-p)}$	typ.	0,28	V
SECAM: peak-to-peak value	$V_{9-2(p-p)}$; $V_{11-2(p-p)}$		1,5 to 3	V
Input impedance	$\lvert Z_{9-2}\rvert$; $\lvert Z_{11-2}\rvert$	>	1	kΩ

Reference input signal amplitude

PAL: peak-to-peak value	$V_{6-2(p-p)}$; $V_{7-2(p-p)}$		0,5 to 1,5	V
SECAM: peak-to-peak value	$V_{5-2(p-p)}$; $V_{8-2(p-p)}$		0,18 [1] to 1,5	V
Input impedance	$\lvert Z_{5-2}\rvert$; $\lvert Z_{7-2}\rvert$; $\lvert Z_{6-2}\rvert$; $\lvert Z_{8-2}\rvert$		0,75 to 1,25	kΩ

Colour difference output signal

(R-Y); peak-to-peak value	$V_{12-2(p-p)}$		0,99 to 1,21	V [2]
(B-Y); peak-to-peak value	$V_{10-2(p-p)}$		1,32 to 1,62	V [2]
Output impedance	$\lvert Z_{10-2}\rvert$; $\lvert Z_{12-2}\rvert$		2,4 to 4,2	kΩ

Diaphotie at SECAM operation

Diaphotie of the total circuit at frequencies corresponding to saturated green D_R = 4,72 MHz and D_B = 4,04 MHz		<	−40	dB

Square wave input

peak-to-peak value	$V_{16-2(p-p)}$		2,5 to 3,5	V
Input impedance	$\lvert Z_{16-2}\rvert$	>	3,8	kΩ

System switch input [3]

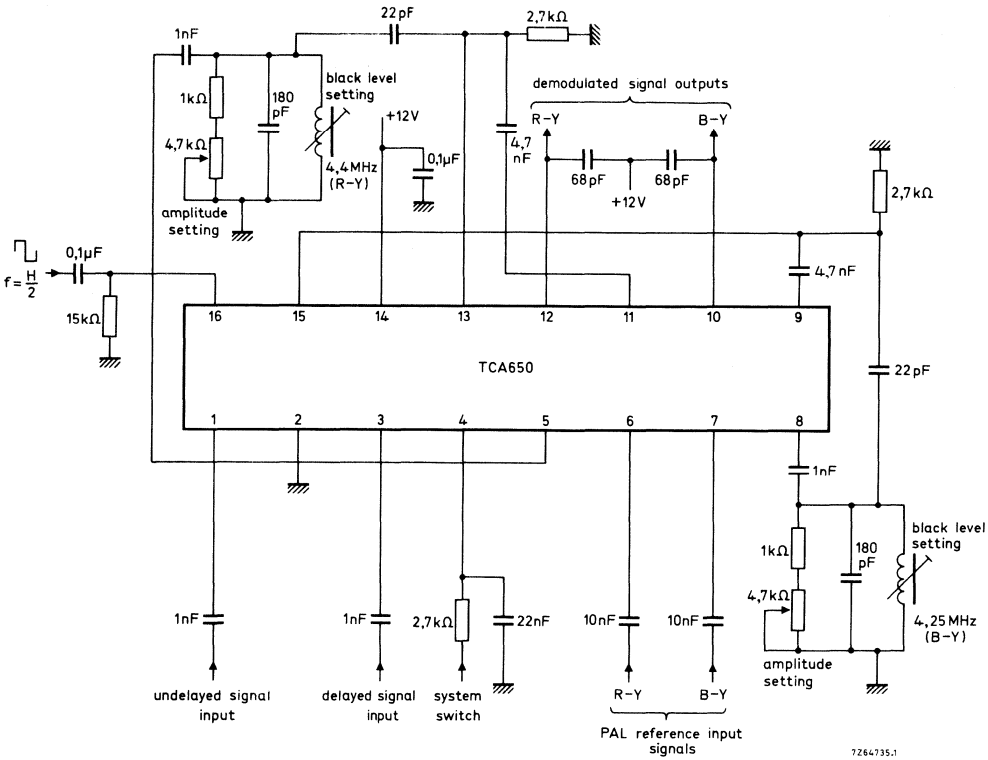
PAL:		7 to V_{14-2}	V
SECAM:		0 to 1	V

[1] Limiting starts at the quoted value.

[2] The peak-to-peak clipping level for PAL is about 4,7 V for (B-Y) and 3 V for (R-Y). The discriminator characteristic allows a maximum peak-to-peak output signal of 3,6 V for (B-Y) and 2,4 V for (R-Y) (SECAM).

[3] The switching signal is applied to pin 4 via a resistor of 2,7 kΩ (±10%).

APPLICATION INFORMATION



Pinning

1. Chrominance input
2. Earth (negative supply)
3. Chrominance input
4. System switch input
5. Reference (R-Y) input SECAM
6. Reference (R-Y) input PAL
7. Reference (B-Y) input PAL
8. Reference (B-Y) input SECAM
9. Chrominance (B-Y), D_B input
10. Colour difference (B-Y) output
11. Chrominance (R-Y), D_R input
12. Colour difference (R-Y) output
13. Chrominance (R-Y), D_R output
14. Supply voltage (12 V)
15. Chrominance (B-Y), D_B output
16. Square wave input

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Chrominance input

   The blanked composite chrominance signal from pin 1 of the TCA640 is applied to this input via a resistive divider.

2. Negative supply (earth)

3. Chrominance input

   The blanked composite chrominance signal from pin 15 of the TCA640 is applied to this input via a delay-line, which has a delay time of 64 µs.

4. System switch input

   The control voltage for switching the standard is applied to this input via a resistor of 2,7 kΩ (± 10%). A decoupling capacitor of at least 10 nF is recommended. Between 7 V and the supply voltage the circuit operates in the PAL mode, whereas between 0 V and 1 V the mode SECAM is selected.

5. Reference input for the (R-Y) demodulator

   The SECAM reference signal is applied to this pin. The reference signal is obtained from pin 11 via a tank circuit. The tank circuit is tuned such that the level at the (R-Y) output (pin 12) during black (f_o = 4, 4 MHz) equals the level during blanking (no signal). The output voltage amplitude at pin 12 can be adjusted by damping the tank circuit.

6. Reference input for the (R-Y) demodulator

   A PAL reference signal having (R-Y) phase is applied to this pin.

7. Reference input for the (B-Y) demodulator

   A PAL reference signal having (B-Y) phase is applied to this pin.

8. Reference input for the (B-Y) demodulator

   The SECAM reference signal is applied to this pin. The reference signal is obtained from pin 15 via a tank circuit. The tank circuit is tuned such that the level at the (B-Y) output (pin 10) during black (f_o = 4, 25 MHz) equals the level during blanking (no signal). The output voltage amplitude at pin 10 can be adjusted by damping the tank circuit.

9. Chrominance input to the (B-Y), D_B demodulator

   The output signal of pin 15 is applied via a coupling capacitor of 4, 7 nF.

10. Output of the (B-Y) demodulator

    The output signal of the balance demodulator contains an r.f. ripple of twice the chrominance frequency to be filtered by a π filter. At SECAM the required de-emphasis circuit should be applied.

11. Chrominance input to the (R-Y), D_R demodulator

    The output signal of pin 13 is applied via a coupling capacitor of 4, 7 nF.

APPLICATION INFORMATION (continued)

12. Output of the (R-Y) demodulator

See pin 10.

13. Chrominance (R-Y), D_R output

The (R-Y) component of the chrominance signal (D_R component at SECAM) is present at this pin.
The signal is applied to the input of the (R-Y) demodulator (pin 11) and to the tank circuit for the SECAM reference signal.
The emitter follower output should be loaded with a 2,7 kΩ resistor to obtain an output impedance of $<100\ \Omega$.

14. Supply voltage (12 V)

Correct operation occurs within the range 10,2 to 13,2 V.
The power dissipation must not exceed 510 mW at 65 °C ambient temperature.

15. Chrominance (B-Y), D_B output

The (B-Y) component of the chrominance signal (D_B component at SECAM) is present at this pin.
The signal is applied to the input of the (B-Y) demodulator (pin 9) and to the tank circuit for the SECAM reference signal.
The emitter follower output should be loaded with a 2,7 kΩ resistor to obtain an output impedance of $<100\ \Omega$.

16. Square wave input

A square wave with an amplitude of 3 V drives the PAL switch or the SECAM permutator.
The square wave is available at pin 12 of the TCA640.

CONTRAST, SATURATION AND BRIGHTNESS CONTROL CIRCUIT FOR COLOUR DIFFERENCE AND LUMINANCE SIGNALS

The TCA660B is an integrated circuit performing the control functions of contrast, saturation and brightness in colour television receivers.
Contrast is controlled by three tracking electronic potentiometers; one for the luminance signal and the other two for the (R-Y) and (B-Y) colour difference signals.
In addition two tracking electronic potentiometers provide the saturation control of the colour difference signals.
Brightness is controlled by varying the black level of the luminance signal at the output.
An inverting amplifier is also included for matrixing the (G-Y) signal from the (R-Y) and (B-Y) colour difference signals.

QUICK REFERENCE DATA

Supply voltage	V_{13-4}	nom.	12	V	
Supply current	I_{13}	nom.	35	mA	
Luminance input current (black-to-white positive video signal)	I_{16}	typ.	0,7	mA	
Luminance output voltage (black-to-white positive video signal; peak-to-peak value)	$V_{1-4(p-p)}$	typ.	3	V	1)
Black level (nominal value)	V_{1-4}	typ.	4,2	V	
Brightness control (around nominal black level)	V_{1-4}		+1 to −2	V	
Gain of the (R-Y) and (B-Y) amplifier		typ.	5	dB	1) 2)
Gain of the (G-Y) amplifier		typ.	1		
Contrast control range			+3 to −20	dB	3)
Saturation control range			+6 to −20	dB	3)

1) At nominal contrast setting (max. contrast −3 dB)

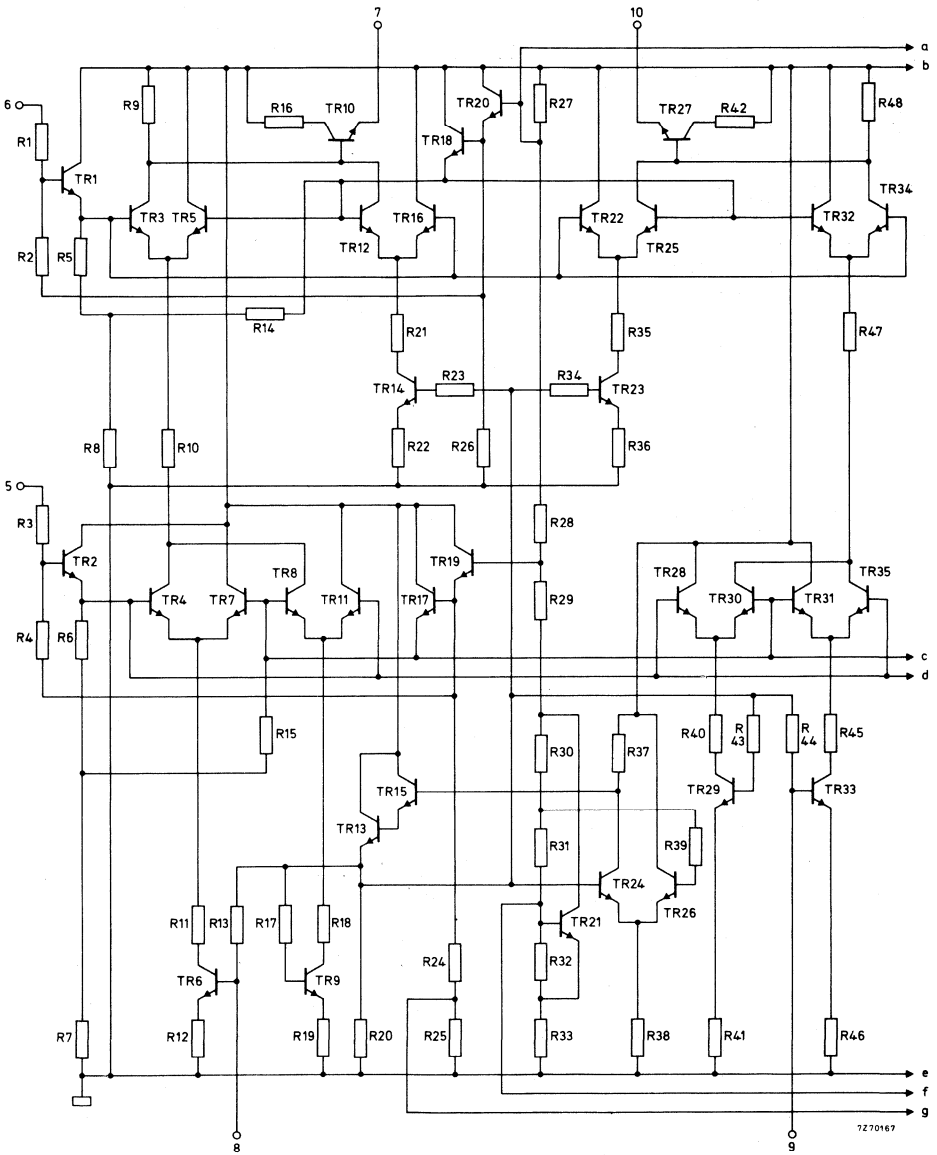
2) At nominal saturation control setting (max. saturation −6 dB)

3) Nominal contrast and nominal saturation are specified as 0 dB.

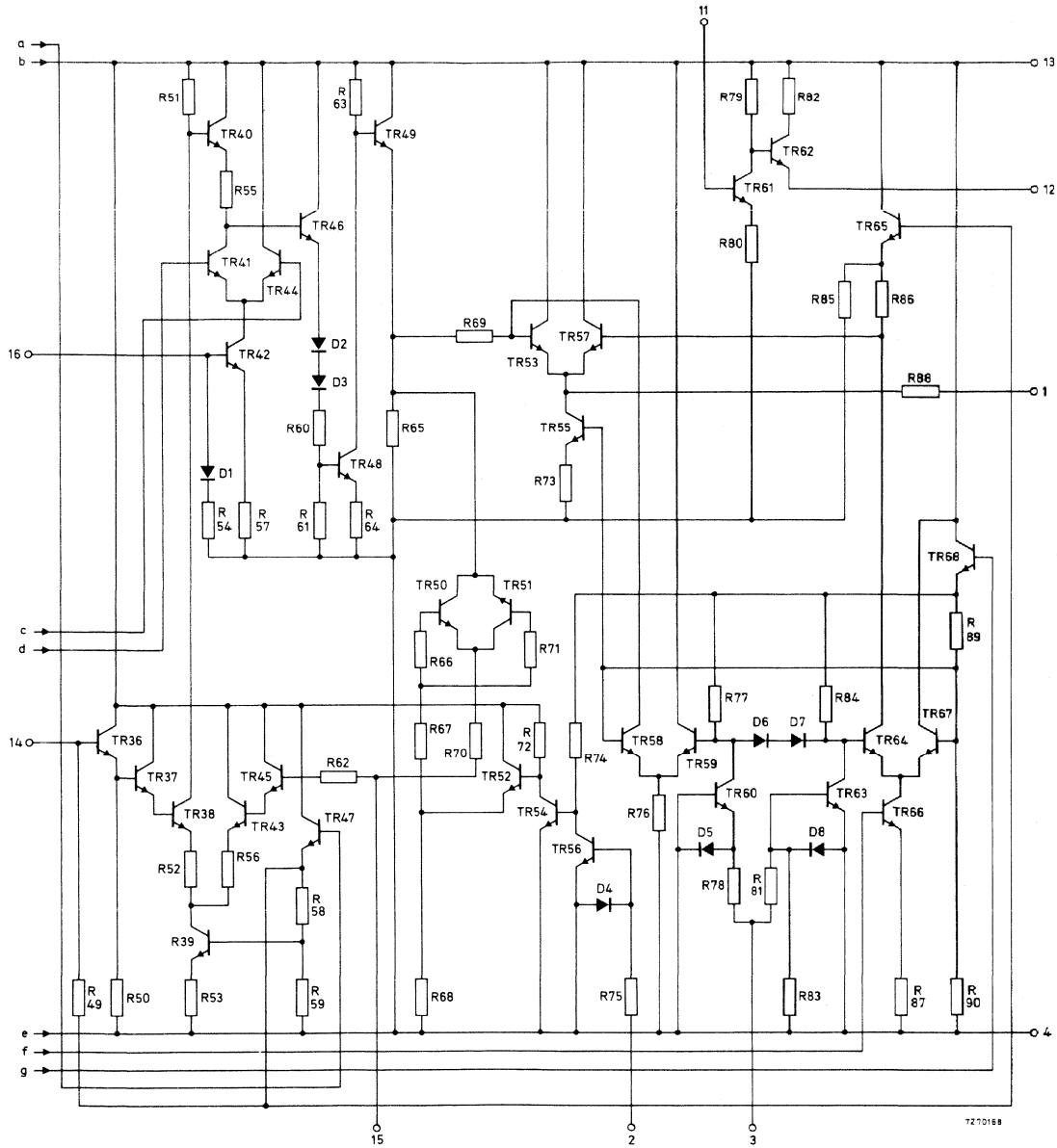
PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

CIRCUIT DIAGRAM



CIRCUIT DIAGRAM (continued)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage			
Supply voltage	V_{13-4}	max.	13,2 V
Power dissipation			
Total power dissipation	P_{tot}	max.	600 mW
Temperatures			
Storage temperature	T_{stg}		−25 to +125 °C
Operating ambient temperature	T_{amb}		−25 to +65 °C [1]

CHARACTERISTICS measured in the circuit on page 7

Supply voltage	V_{13-4}	typ.	12 V 10,2 to 13,2 V
Required input signals at V_{13-4} = 12 V and T_{amb} = 25 °C			
Luminance input current			
black-to-white positive video signal	I_{16}	typ.	0,7 mA 0 to 2,5 mA
Input impedance at I_{16} = 1 mA	$\lvert Z_{16-4}\rvert$		60 to 90 Ω
Input impedance variation for an			
input current variation $\Delta I_{16} = \pm 0,5$ mA	$\lvert \Delta Z_{16-4}\rvert$		∓25 Ω
Colour difference input voltage			
(R-Y); peak-to-peak value	$V_{9-4(p-p)}$	<	0,7 V
(B-Y); peak-to-peak value	$V_{8-4(p-p)}$	<	0,9 V
Input voltage variation before clipping			
of the output voltage occurs	ΔV_{8-4} ΔV_{9-4}	typ.	0,8 V
Input impedance	$\lvert Z_{8-4}\rvert$ $\lvert Z_{9-4}\rvert$		3,5 to 6,5 kΩ
Blanking pulse (peak value)	V_{3-4M}		−1,5 to −10 V
Black level reinsertion pulse (peak value)	V_{3-4M}		+2 to +12 V [2]
Black level clamp pulse (peak value)	V_{2-4M}		+1 to +12 V
Luminance output voltage at nominal contrast			
black-to-white positive video signal; peak-to-peak value	$V_{1-4(p-p)}$		2 to 4 V [3]

[1] When a stabilized power supply of ≤ 12 V is applied, T_{amb} is max. 75 °C.
[2] During scan V_{3-4} must be kept lower than 0,7 V (positive and negative) to avoid blanking of the luminance signal.
[3] Nominal contrast is specified as maximum contrast −3 dB.

CHARACTERISTICS (continued)

Black level at nominal brightness setting	V_{1-4}	typ.	4,2	V	1)
Black level variation with brightness setting	ΔV_{1-4}		+1 to −2	V	
Contrast control voltage range	V_{5-4}	See graph on page 6			
Black level variation with contrast control	ΔV_{1-4}	<	40	mV	2)
Black level variation with video contents	ΔV_{1-4}	<	20	mV	3)
Variation between video black level and reinserted black level at ΔT_{amb} = 25 °C and ΔV_{13-4} ± 10%	V_{1-4}	<	±20	mV	
Blanking level with respect to nominal brightness	V_{1-4}		−0,8 to −1,2	V	
Bandwidth (−3 dB) of luminance signal	B	>	6	MHz	
Colour difference output signal for nominal contrast and saturation 4) 5)					
(R-Y); peak-to-peak value	$V_{10-4\,(p-p)}$	typ.	1,25	V	6)
(B-Y); peak-to-peak value	$V_{7-4\,(p-p)}$	typ.	1,6	V	6)
D.C. output level	V_{7-4} } V_{10-4} }	typ.	6,1	V	
Output level variation with contrast and saturation control	ΔV_{7-4} } ΔV_{10-4} }	<	500	mV	
Permissible d.c. load impedance	$\lvert Z_{7-4}\rvert$ } $\lvert Z_{10-4}\rvert$ }	>	4	kΩ	
Saturation control voltage range	V_{6-4}	See graph on page 6			
Saturation control at V_{6-4} < 0,5 V		<	−50	dB	
Bandwidth (−3 dB) of colour difference signal	B	>	2,5	MHz	

1) Nominal brightness setting V_{14-4} = 5,7 V.
2) Only valid if the input current does not exceed 0,5 mA during black.
3) For a.c. coupling only.
4) Nominal contrast is specified as maximum contrast −3 dB.
5) Nominal saturation is specified as maximum saturation −6 dB.
6) This value is obtained at the specified maximum input voltage.

CHARACTERISTICS (continued)

(G-Y) amplifier

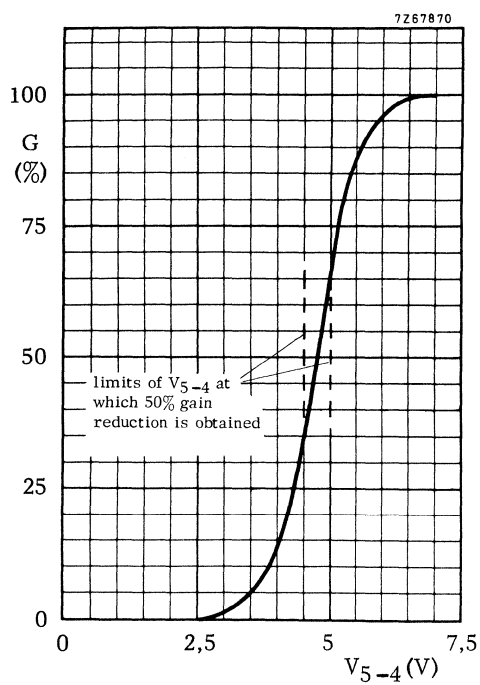
input voltage (peak-to-peak value)	$V_{11-4(p-p)}$	<	1 V
output voltage (peak-to-peak value)	$V_{12-2(p-p)}$	<	1 V
voltage gain	G_{11-12}		−1 to +0,5 dB

Tracking during contrast and saturation control

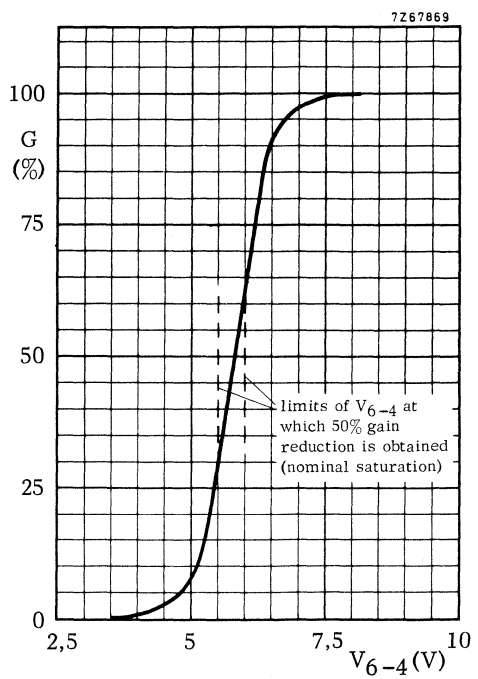
at a contrast decrease of 20 dB			
change of the ratio $\frac{(R-Y)}{(B-Y)}$		<	±1 dB
change of the ratio $\frac{Y}{(B-Y)}$			0 to 4 dB
at a saturation decrease of 20 dB			
change of the ratio $\frac{(R-Y)}{(B-Y)}$		<	±1 dB

Cross coupling

luminance signal to colour difference signal		<	−40 dB
(B-Y) signal to (R-Y) signal		<	−30 dB
colour difference signal to luminance signal		<	−40 dB

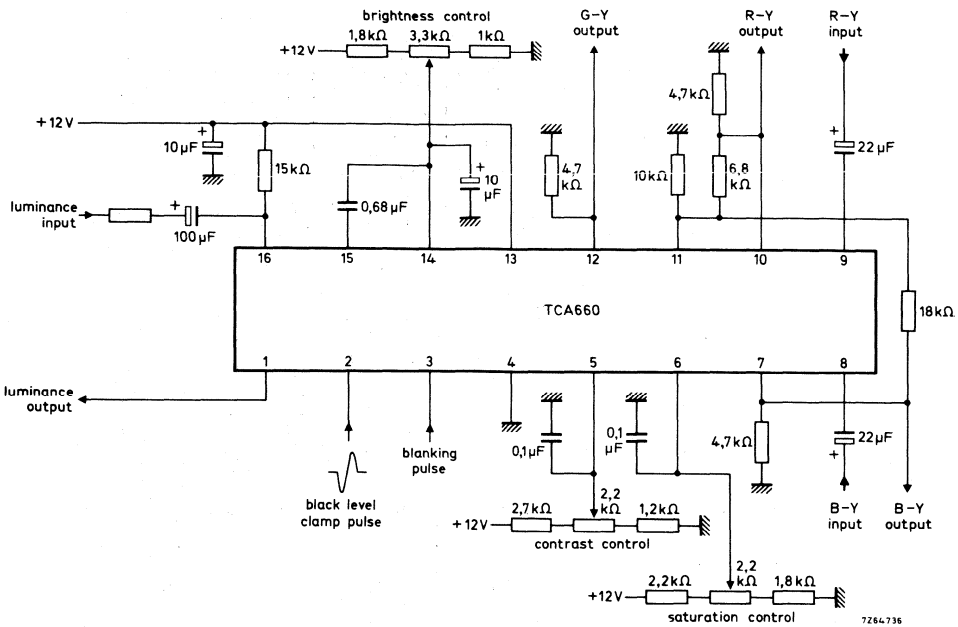


Contrast control of luminance amplifier



Saturation control of chrominance amplifier

APPLICATION INFORMATION



Pinning

1. Luminance signal output
2. Black level clamp pulse input
3. Blanking pulse input
4. Earth (negative supply)
5. Contrast control input
6. Saturation control input
7. (B-Y) signal output
8. (B-Y) signal input
9. (R-Y) signal input
10. (R-Y) signal output
11. (G-Y) signal input
12. (G-Y) signal output
13. Supply voltage (12 V)
14. Brightness control input
15. Black level clamp capacitor
16. Luminance signal input

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Luminance signal output

   A positive video signal of 3 V peak-to-peak is available at nominal contrast setting. The black level is clamped internally on the back porch.
   By means of the brightness control the black level can be varied between 2,2 V and 5,2 V. The blanking level of the output signal will assume a value of 3,0 to 3,4 V.

2. Black level clamp pulse input

   A positive pulse with a peak value between +1 V and +12 V will clamp the black level of the video signal to a nominal level of 4,2 V. The pulse may only be present during the back porch and should have a duration of about 3 μs.

3. Blanking pulse input

   Two modes operation can be selected by the choice of the amplitude of the pulse applied:

   - blanking

   - black level reinsertion

   Blanking of the luminance output signal is obtained when the peak value of the pulse ranges from −1,5 to −10 V. An artificial black level of nominally +4,2 V is inserted in the luminance output signal during the blanking period when the peak value of the pulse ranges from +2 to +12 V.
   During scan the amplitude at pin 3 should remain between +0,7 V and −0,7 V to avoid blanking.

4. Negative supply (earth)

5. Contrast control input

   The contrast curve is given on page 4. To avoid damaging of the circuit by flash-over pulses, picked-up by the leads, it is recommended that a capacitor of 100 nF be connected between this pin and earth.

6. Saturation control input

   The control curve is given on page 4. To avoid damaging of the circuit by flash-over pulses, picked-up by the leads, it is recommended that a capacitor of 100 nF be connected between this pin and earth.

7. (B-Y) signal output

   The amplitude of this signal is controlled by the contrast setting and the saturation setting simultaneously. At nominal contrast and nominal saturation setting an amplitude of 1,6 V peak-to-peak is obtained at an input amplitude of 0,9 V peak-to-peak. The average level is typically 6,1 V.

8. (B-Y) signal input

   The signal has to be a.c. coupled to the input.
   To cope with the variation of picture contents an input voltage margin of ±0,8 V is provided, whereas the input signal has a typical value of ±0,45 V for a saturated colour bar signal.

APPLICATION INFORMATION (continued)

9. (R-Y) signal input

The signal has to be a.c. coupled to the input.
To cope with the variation of picture contents an input voltage margin of ± 0,8 V is provided, whereas the input signal has a typical value of ± 0,35 V for a saturated colour bar input.

10. (R-Y) signal output

The amplitude of this signal is controlled by the contrast setting and saturation setting simultaneously. At nominal contrast and nominal saturation setting an amplitude of 1,25 V peak-to-peak is obtained at an input amplitude of 0,7 V peak to peak.
The average level is typically 6,1 V.

11. (G-Y) signal input

The (G-Y) signal is obtained by matrixing a part of the (R-Y) and (B-Y) signals in a resistor network. The input may range from 1 to 6,5 V.
An average level of typical 5,9 V is required to produce an average output level of 6,1 V.
The gain of the inverter stage is typically 1.

12. (G-Y) signal output

An inverted signal with an amplitude of maximum 1 V peak-to-peak is available at this pin.

13. Supply voltage (12 V)

Correct operation occurs within the range 10,2 to 13,2 V.
The power dissipation must not exceed 600 mW at 65 °C ambient temperature.

14. Brightness control input

The black level of the luminance output signal tracks the potential applied to this pin.
A typical value for setting the brightness control is 5,7 V, for which a black level of 4,2 V is obtained.
It is recommended that a capacitor of at least 10 µF be connected between this pin and earth.

15. Black level clamp capacitor

The level of the back porch of the luminance output signal is stored in an external capacitor of about 0,68 µF; the latter to be connected between pins 14 and 15.

16. Luminance signal input

A positive luminance signal of 0,7 mA peak-to-peak between black and white level drives the luminance amplifier.
A black level of about 0,3 mA is recommended. For a.c. coupling a bias resistor to the supply line is required to bias the amplifier properly.
The resistance depends on the signal amplitude e.g.: 15 kΩ is recommended for a input signal of 0,7 mA peak-to-peak.

DOUBLE BALANCED MODULATOR/DEMODULATOR

The TDA0820T is a monolithic integrated circuit for use at frequencies up to 650 MHz.
Typical applications are:

- modulator
- mixer
- switch/chopper
- a.m. synchronous demodulator
- f.m. quadrature demodulator
- phase comparator
- differential amplifier

The circuit is arranged to offer very flexible circuit design possibilities. The excellent matching and temperature tracking of the transistors in the circuit allow the use of circuit techniques which are not available when using discrete devices.

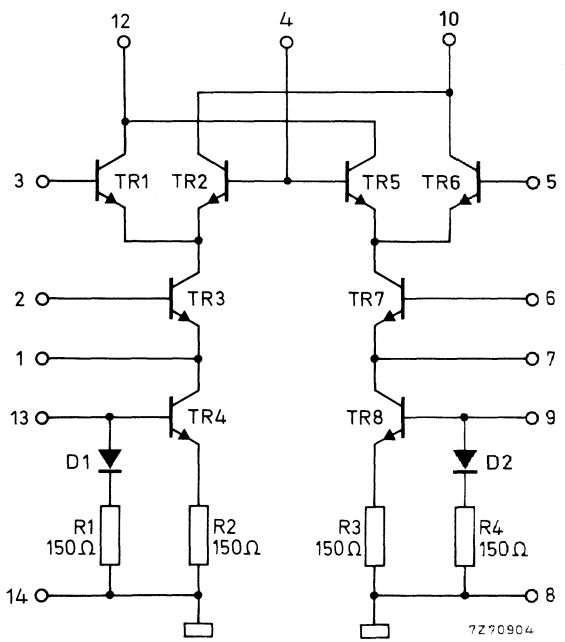


Fig. 1 Circuit diagram.

PACKAGE OUTLINE

14-lead mini-pack; plastic (SO-14; SOT-108A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{10-8}; V_{10-14}; V_{12-8}; V_{12-14}	0 to 13,2	V
Voltages (each transistor)			
Collector-substrate voltage (open base) and emitter)	V_{CSO}	max. 15	V
Collector-base voltage (open emitter)	V_{CBO}	max. 12	V
Collector-emitter voltage (open base)	V_{CEO}	max. 10	V
Emitter-base voltage (open collector)	V_{EBO}	max. 5	V
Currents (each transistor)			
Emitter current	I_E	max. 10	mA
Base current	I_B	max. 10	mA
Total power dissipation when mounted on a printed-circuit board	P_{tot}	max. 250	mW
Storage temperature	T_{stg}	−55 to + 125	°C
Operating ambient temperature	T_{amb}	0 to + 70	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	= 220	K/W

CHARACTERISTICS

$V_{10-8} = V_{10-14} = V_{12-8} = V_{12-14} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 2

Supply current	$I_{10} + I_{12}$	typ. 2,5	mA
		< 3	mA
Input signals			
carrier signal (r.m.s. value)	$V_{3-4(rms)}$; $V_{5-4(rms)}$	< 100	mV
video signal; negative modulated (peak-to-peak value)	$V_{6-2(p-p)}$	< 1,4	V
Output signal at top sync over 75 Ω (peak-to-peak value)	$V_{10-12(p-p)}$	> 22	mV
Carrier suppression in balanced condition	V_{10-12}	> 38	dB
Differential phase		< 6°	
Differential gain		< 15	%
Distortion of video signal		< −38	dB

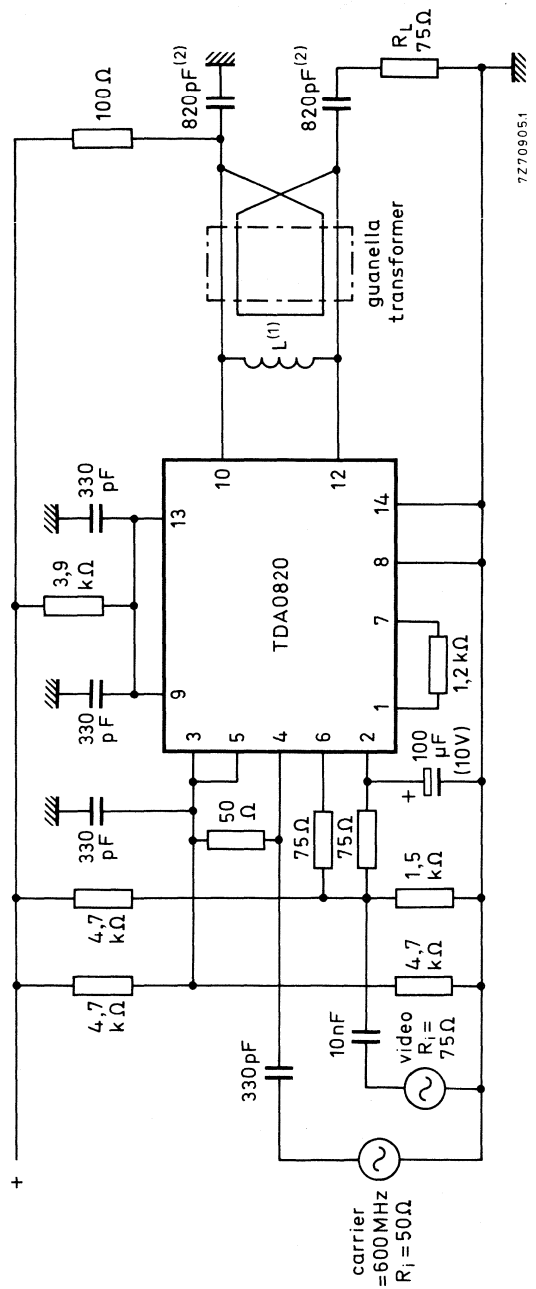


Fig. 2 Test circuit.

(1) L = air coil; 3 turns; ϕ 3 mm.
(2) U.H.F. decoupling capacitor 2212 669 98003.

4 W AUDIO POWER AMPLIFIER WITH D.C. VOLUME CONTROL

The TDA1013A is a monolithic integrated audio amplifier circuit with d.c. volume control in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit very suitable for applications in mains-fed apparatus such as television receivers and record players.

The d.c. volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control can be obtained by means of a variable d.c. voltage between 3,5 and 8 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop gain. This offers an optimum in number of external components, performance and stability.

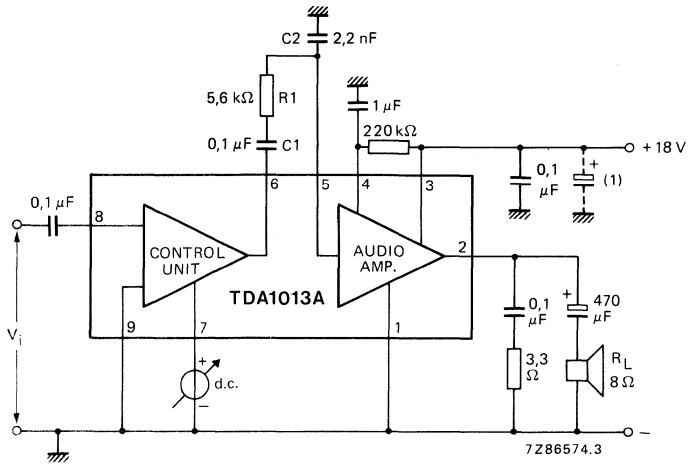
The SIL package (SOT-110B) offers a simple and low-cost heatsink connection.

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35 V
Repetitive peak output current	I_{ORM}	max.	1,5 A
Total sensitivity (d.c. control at max. gain) for P_o = 2,5 W	V_i	typ.	55 mV
Audio amplifier			
Output power at d_{tot} = 10% V_P = 18 V; R_L = 8 Ω	P_o	typ.	4,5 W
Total harmonic distortion at P_o = 2,5 W; R_L = 8 Ω	d_{tot}	typ.	0,5 %
Sensitivity for P_o = 2,5 W	V_i	typ.	125 mV
D.C. volume control unit			
Gain control range	ϕ	>	80 dB
Signal handling at $d_{tot} < 1\%$ (d.c. control at 0 dB)	V_i	>	1,2 V
Sensitivity for V_o = 125 mV at max. voltage gain	V_i	typ.	55 mV
Input impedance (pin 8)	$\|Z_i\|$	typ.	250 kΩ

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).



(1) Belongs to power supply.

Fig. 1 Basic application diagram also used as test circuit with R1 = 5,1 kΩ and C1 = 22 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1,5 A
Storage temperature	T_{stg}		−55 to + 150 °C
Crystal temperature	T_j		−25 to + 150 °C
Total power dissipation	see derating curve Fig. 2		

HEATSINK DESIGN

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C (max.); T_j = 150 °C (max); for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,5 W.
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{T_{j\ max} - T_{amb\ max}}{P_{max}} = \frac{150 - 60}{2,5} = 36\ K/W.$$

Since $R_{th\ j\text{-}tab}$ = 9 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 36 − (9 + 1) = 26 K/W.

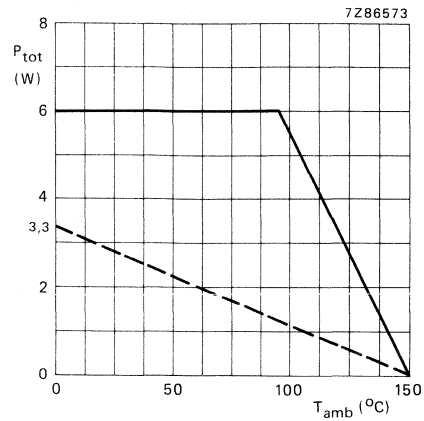


Fig. 2 Power derating curve.
——— infinite heatsink;
– – – without heatsink.

CHARACTERISTICS

V_P = 18 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

Supply voltage	V_P	typ.	18 V
			15 to 35 V
Total quiescent current	I_{tot}	typ.	35 mA
Noise output voltage (see also note)	V_n	<	1,4 mV
Total sensitivity (d.c. control at maximum gain) for P_o = 2,5 W	V_i		38 to 69 mV
		typ.	55 mV
Frequency response (–3 dB)	f		35 Hz to 20 kHz

Audio amplifier

Repetitive peak output current	I_{ORM}	<	1,5 A
Output power at d_{tot} = 10%	P_o	>	4 W
		typ.	4,5 W
Total harmonic distortion at P_o = 2,5 W	d_{tot}	typ.	0,5 %
		<	1 %
Voltage gain	G_v	typ.	30 dB
Sensitivity for P_o = 2,5 W	V_i	typ.	125 mV
Input impedance (pin 5)	$\|Z_i\|$	>	100 kΩ
		typ.	250 kΩ

Note

Measured in a bandwidth according to IEC 179-curve 'A'; R_S = 5 kΩ and d.c. control at minimum gain.

CHARACTERISTICS (continued)

D.C. volume control unit

Gain control range (see also Fig. 3)	ϕ	>	80 dB
Signal handling at $d_{tot} < 1\%$ (d.c. control at 0 dB)	V_i	>	1,2 V
Sensitivity for V_o = 125 mV at max. voltage gain	V_i	typ.	55 mV
Input impedance (pin 8)	$\|Z_i\|$	>	100 kΩ
		typ.	250 kΩ
Output impedance (pin 6)	$\|Z_o\|$	100 to	400 Ω
		typ.	200 Ω

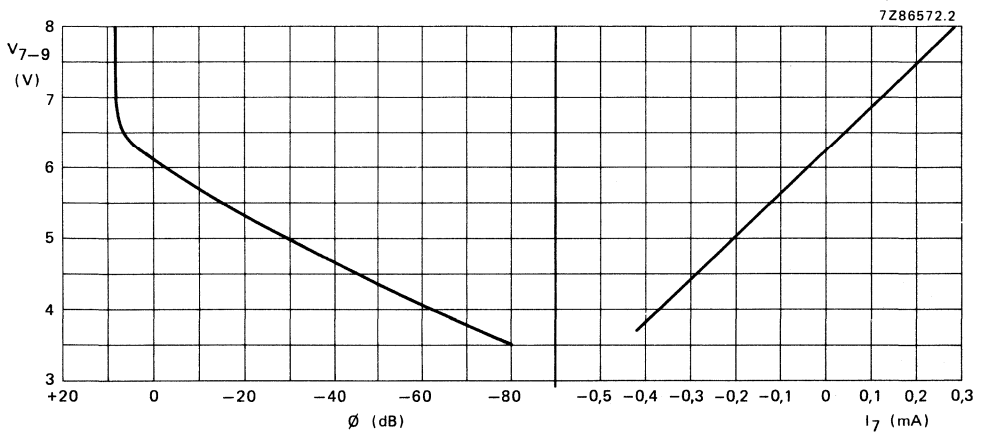


Fig. 3 Typical values gain control; V_i at pin 7.

1 TO 4 W AUDIO POWER AMPLIFIER

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P	3,6 to 18	V
Peak output current	I_{OM}	max. 2,5	A
Output power at d_{tot} = 10%			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ. 0,3	%
Input impedance			
preamplifier (pin 8)	$\lvert Z_i \rvert$	> 100	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ. 20	kΩ
Total quiescent current	I_{tot}	typ. 14	mA
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

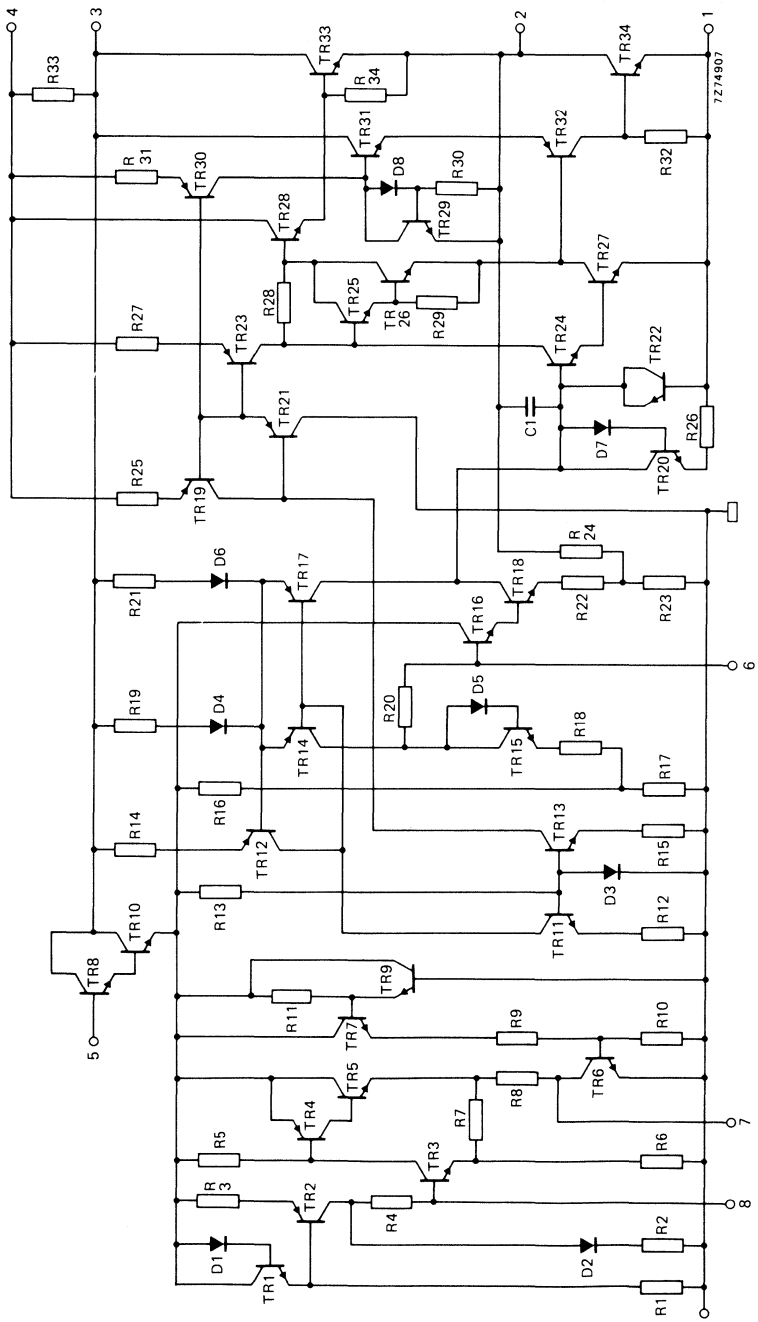


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18 V
Peak output current	I_{OM}	max.	2,5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100 hours

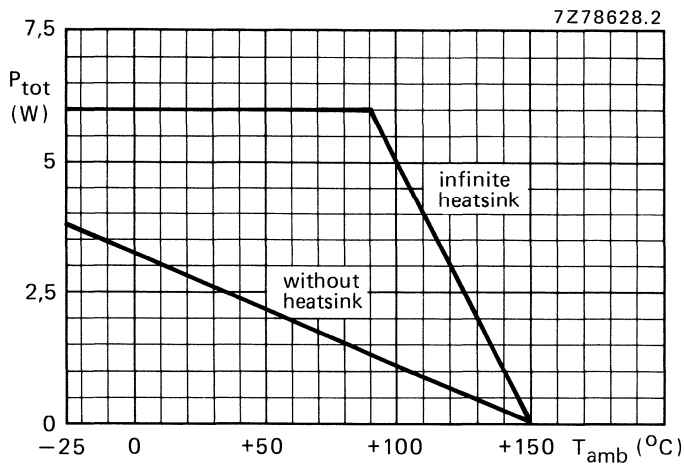


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 45 °C maximum.

The maximum sine-wave dissipation is 1,8 W.

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 45}{1,8} = 58\ K/W.$$

Where $R_{th\ j\text{-}a}$ of the package is 45 K/W, so no external heatsink is required.

D.C. CHARACTERISTICS

Supply voltage range	V_P	3,6 to 18	V
Repetitive peak output current	I_{ORM}	< 2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ. 14 < 25	mA mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)			
with bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
without bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 3,0	W
Voltage gain:			
preamplifier (note 2)	G_{v1}	typ. 23	dB
power amplifier	G_{v2}	typ. 29	dB
total amplifier	$G_{v\,tot}$	typ. 52 49 to 55	dB dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ. 0,3 < 1,0	% %
Frequency response; −3 dB (note 3)	B	60 Hz to 15	kHz
Input impedance:			
preamplifier (note 4)	$\lvert Z_{i1} \rvert$	> 100 typ. 200	kΩ kΩ
power amplifier	$\lvert Z_{i2} \rvert$	typ. 20	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ. 1	kΩ
Output voltage preamplifier (r.m.s. value)			
d_{tot} < 1% (note 2)	$V_{o(rms)}$	typ. 0,8	V
Noise output voltage (r.m.s. value; note 5)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. 0,5	mV
Noise output voltage at f = 500 kHz (r.m.s. value)			
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ. 8	μV
Ripple rejection (note 6)			
f = 100 Hz	RR	typ. 38	dB

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_O = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

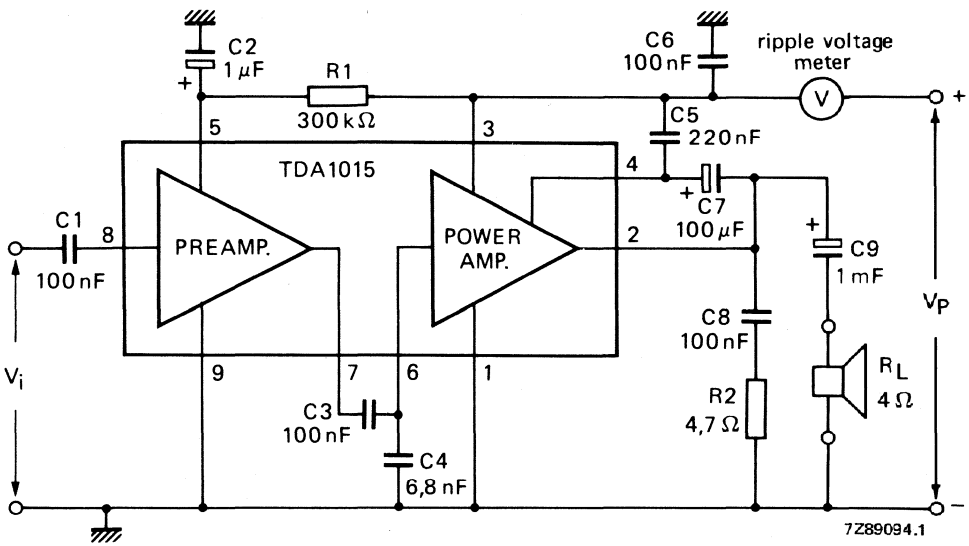


Fig. 3 Test circuit.

APPLICATION INFORMATION

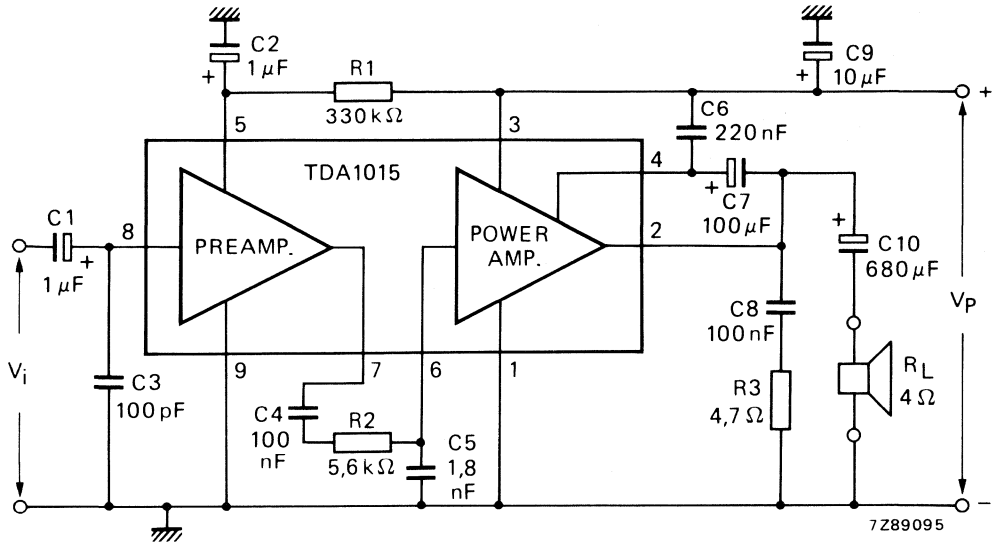


Fig. 4 Circuit diagram of a 1 to 4 W amplifier.

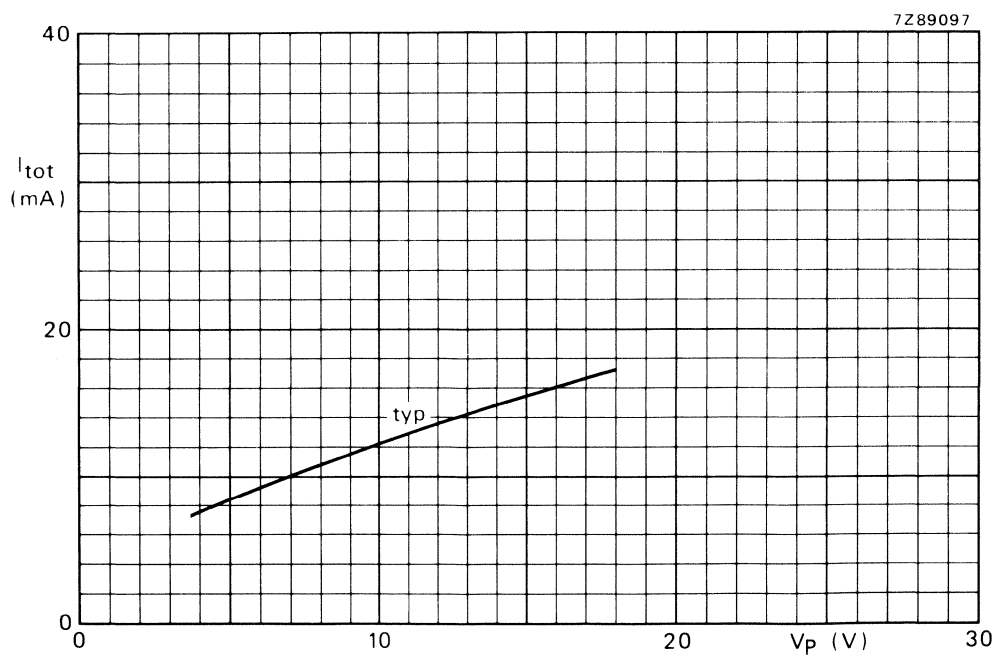


Fig. 5 Total quiescent current as a function of supply voltage.

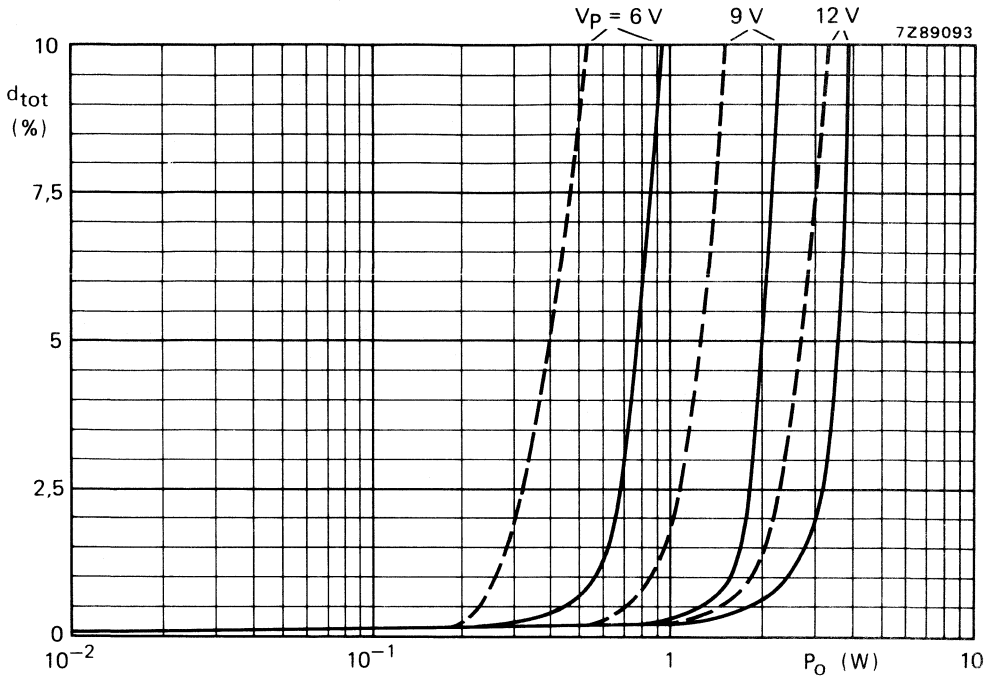


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

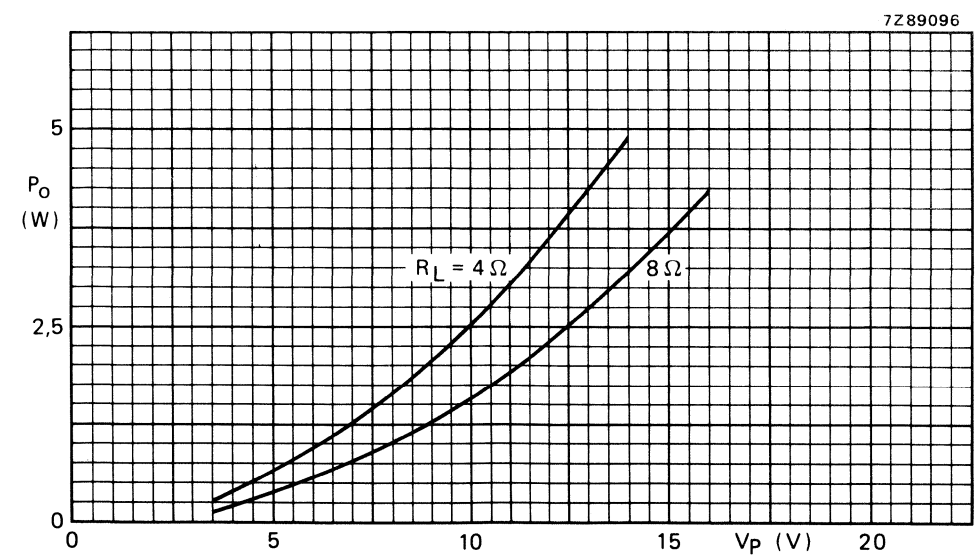


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

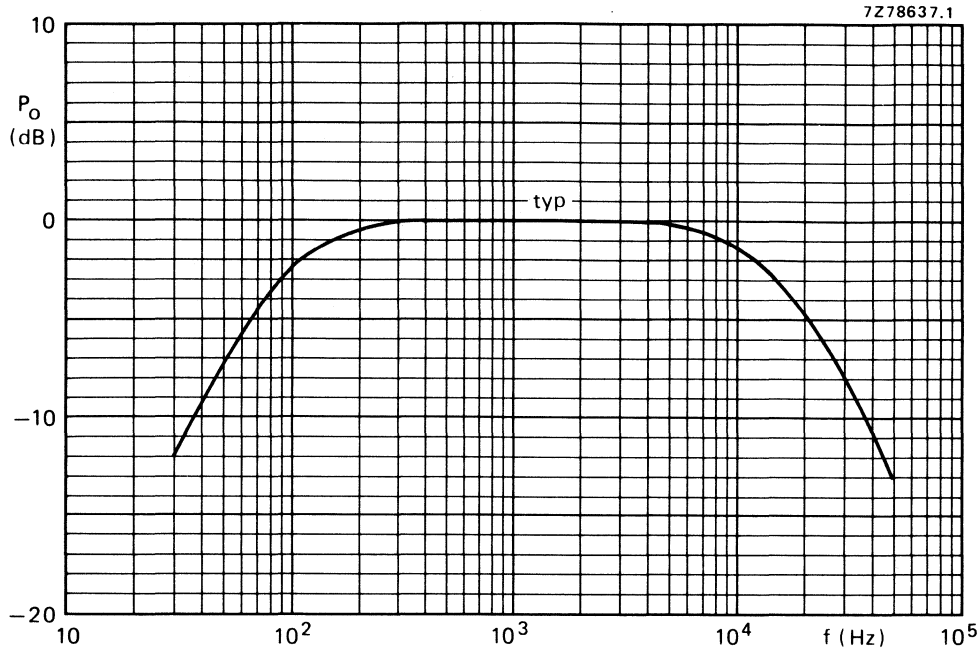


Fig. 8 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

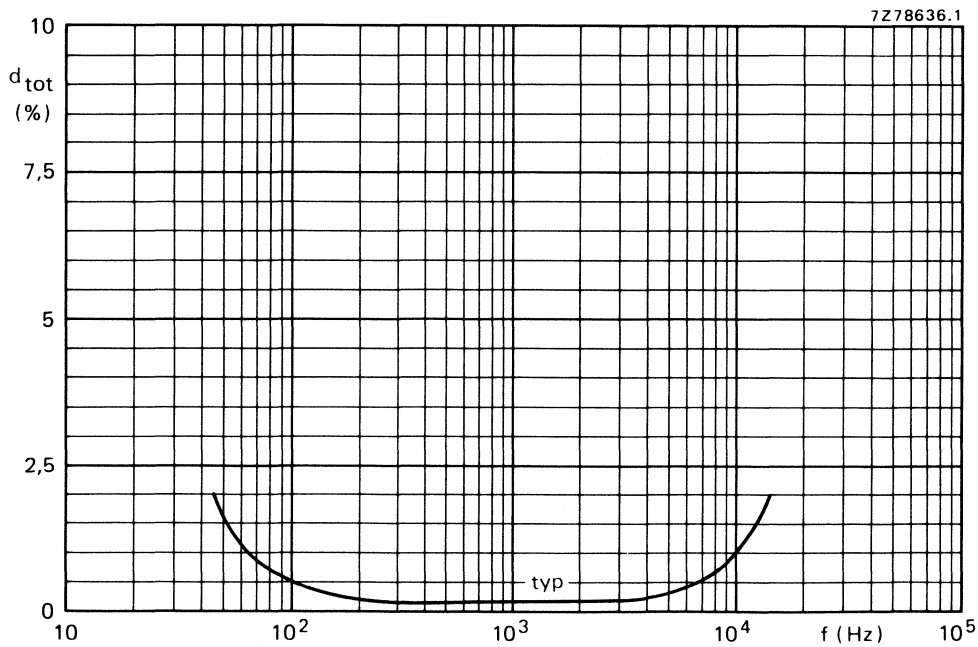


Fig. 9 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

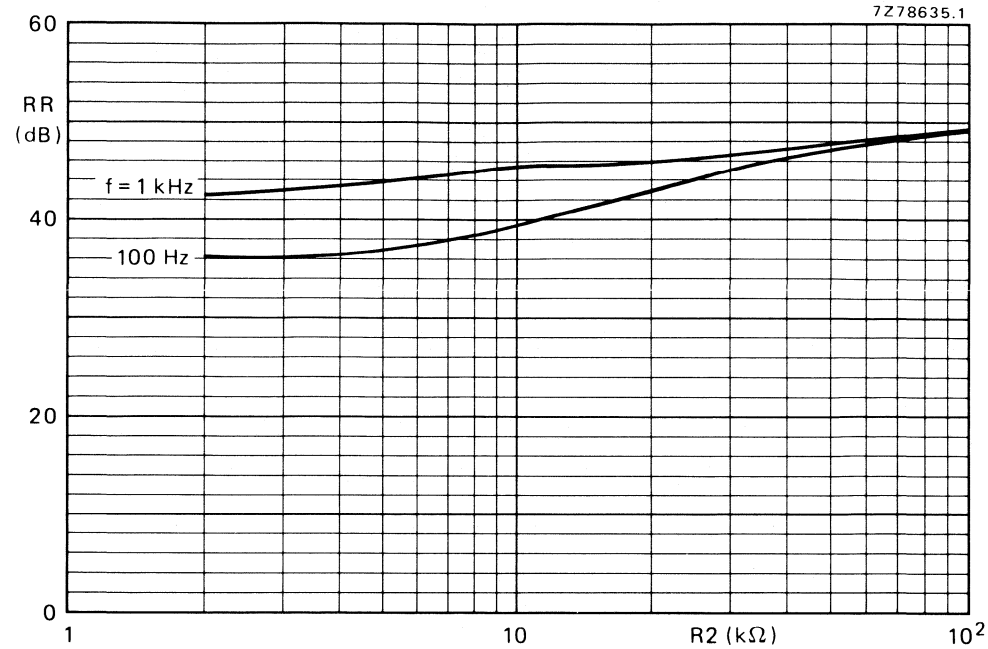


Fig. 10 Ripple rejection as a function of R2 (see Fig. 4); R_S = 0; typical values.

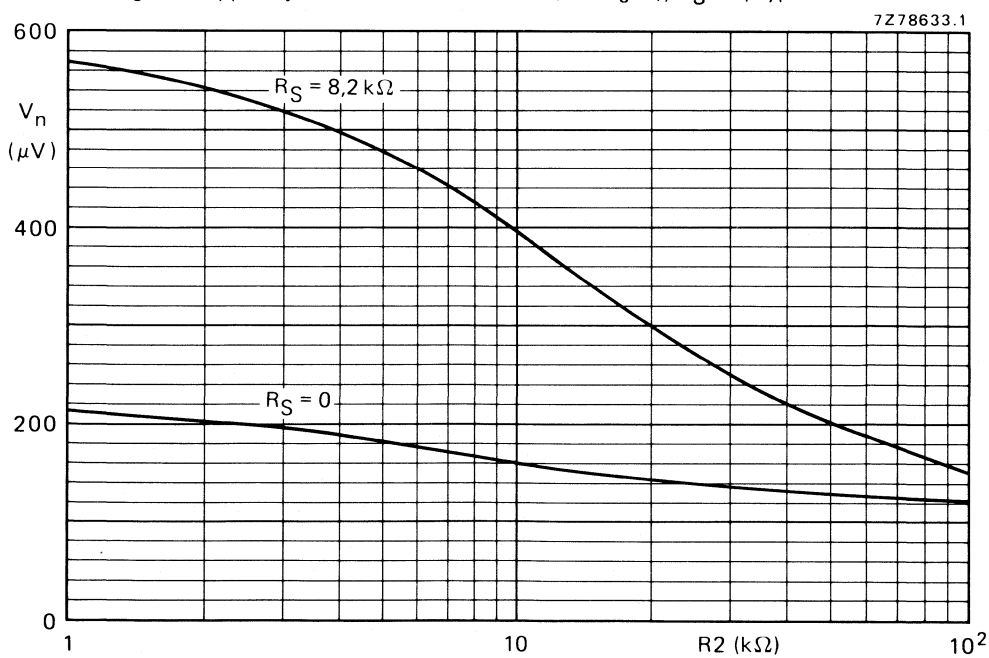


Fig. 11 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

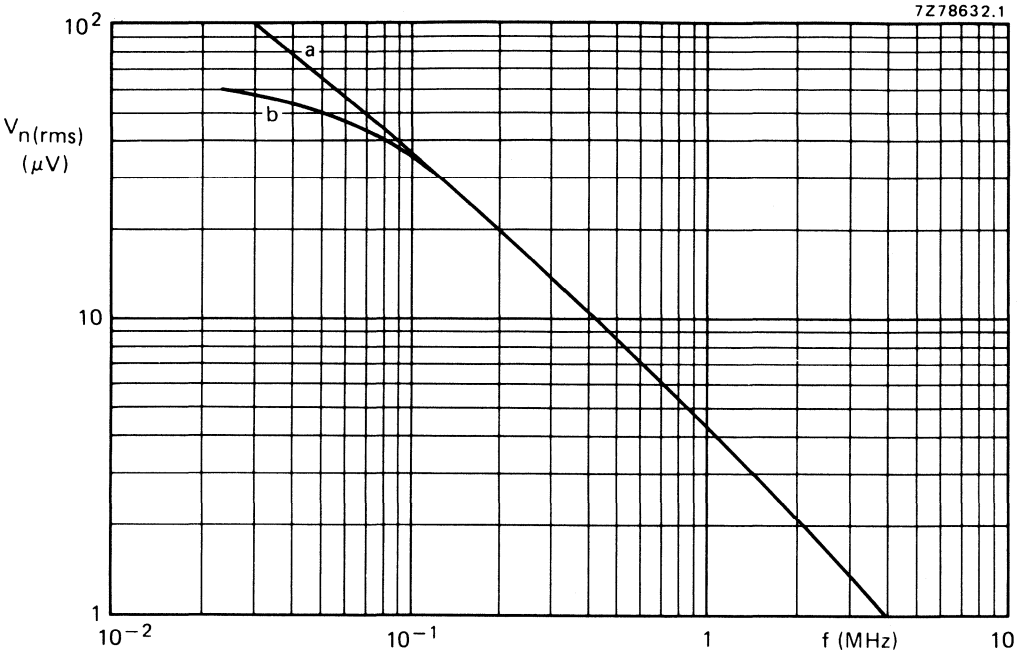


Fig. 12 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

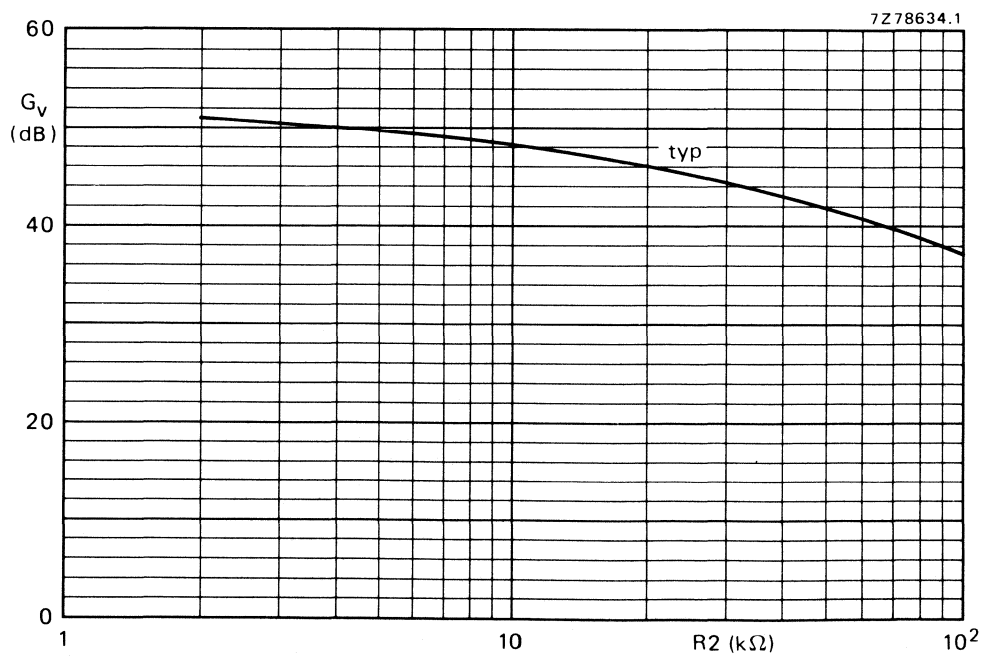


Fig. 13 Voltage gain as a function of R2 (see Fig. 4).

0,5 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1015T is a low-cost audio amplifier which can deliver up to 0,5 W output power into a 16 Ω load impedance at a supply voltage of 9 V. The amplifier is specially designed for portable applications such as radios and recorders. The IC has a very low supply voltage requirement (3,6 V min.).

Features

- High input impedance
- Separated preamplifier and power amplifier
- Limited noise behaviour at radio frequencies
- Short-circuit protected
- Miniature encapsulation

QUICK REFERENCE DATA

Supply voltage range	V_P	3,6 to 12	V
Peak output current	I_{OM}	max. 1	A
Output power	P_o	typ. 0,5	W
Voltage gain power amplifier	G_{v1}	typ. 29	dB
Voltage gain preamplifier	G_{v2}	typ. 23	dB
Total quiescent current	I_{tot}	max. 22	mA
Operating ambient temperature range	T_{amb}	−25 to +150	°C
Storage temperature range	T_{stg}	−55 to +150	°C

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO-8; SOT-96A).

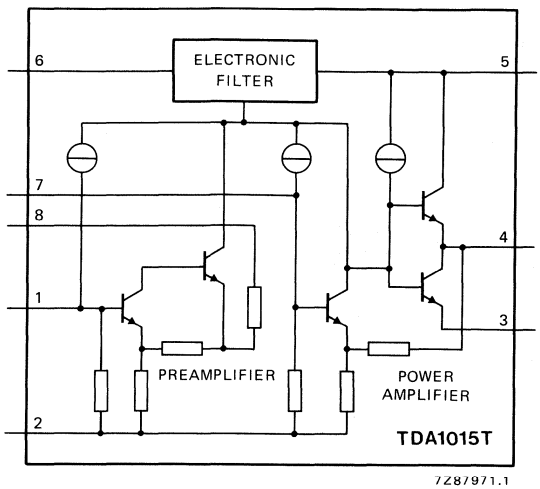


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	12 V
Peak output current	I_{OM}	max.	1 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range			−55 to +150 °C
A.C. short-circuit duration of load during sine-wave drive at V_P = 9 V	t_{sc}	max.	1 hour

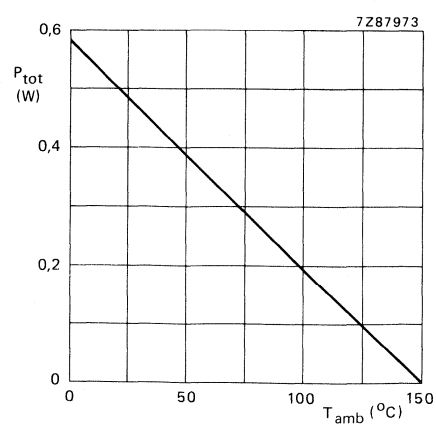


Fig. 2 Power derating curve.

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 9 V; R_L = 16 Ω; f = 1 kHz; see Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_P	3,6	9	12	V
Repetitive peak output current	I_{ORM}	–	–	1	A
Total quiescent current	I_{tot}	–	12	22	mA
A.F. output power at d_{tot} = 10% (note 1)					
V_P = 9 V; R_L = 16 Ω	P_o	–	0,5	–	W
V_P = 6 V; R_L = 8 Ω	P_o	–	0,3	–	W
Voltage gain power amplifier	G_{v1}	–	29	–	dB
Voltage gain preamplifier (note 2)	G_{v2}	–	23	–	dB
Total voltage gain	G_{tot}	49	52	55	dB
Frequency response at −3 dB (note 3)	B	–	60 to 15 000	–	Hz
Input impedance power amplifier	$\|Z_{i1}\|$	–	20	–	kΩ
Input impedance preamplifier (note 4)	$\|Z_{i2}\|$	100	200	–	kΩ
Output impedance preamplifier	$\|Z_{o2}\|$	0,5	1	1,5	kΩ
Output voltage preamplifier (r.m.s. value) $d_{tot} < 1\%$ (note 2)	$V_{o2(rms)}$	–	0,7	–	V
Noise output voltage (r.m.s. value) (note 5)					
R_S = 0 Ω	$V_{n(rms)}$	–	0,2	–	mV
R_S = 10 kΩ	$V_{n(rms)}$	–	0,5	–	mV
Noise output voltage (r.m.s. value) f = 500 kHz; B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	–	8	–	μV
Ripple rejection at f = 100 Hz; C2 = 1 μF (note 6)	RR	–	38	–	dB

Notes to the characteristics

1. Output power is measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistance of 20 kΩ.
3. The frequency response is mainly determined by the capacitors, C1, C3 (low frequency) and C4 (high frequency).
4. Independent of load impedance of preamplifier.
5. Effective unweighted r.m.s. noise voltage measured in a bandwidth from 60 Hz to 15 kHz (slopes 12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude of 2 V).

APPLICATION INFORMATION

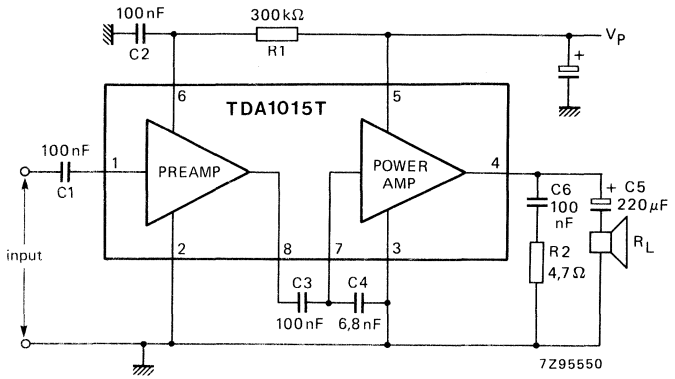


Fig. 3 Test circuit.

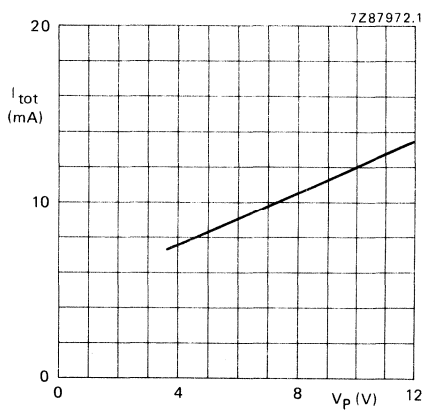


Fig. 4 Total quiescent current as a function of supply voltage.

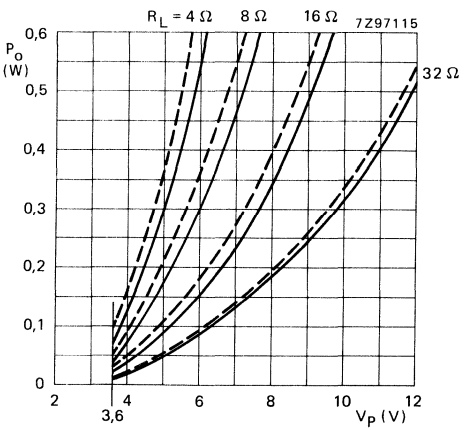


Fig. 5 Output power as a function of supply voltage; d_{tot} = 10%; f = 1 kHz.
——— measured in Fig. 3
– – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

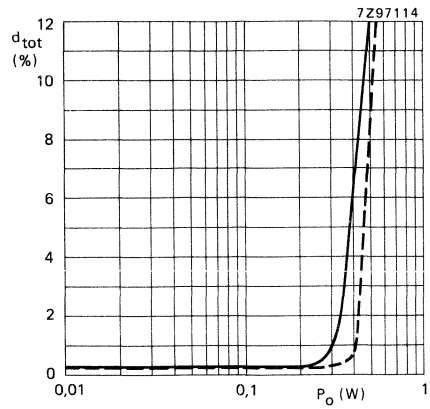


Fig. 6 Total distortion as a function of output power; V_P = 9 V; R_L = 16 Ω; f = 1 kHz.
——— measured in Fig. 3
– – – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

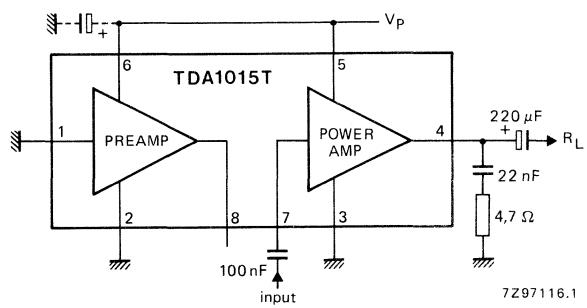


Fig. 7 Application circuit for power stage only and battery power supply; G_{v1} = 29 dB; $|Z_{i1}|$ = 20 kΩ.

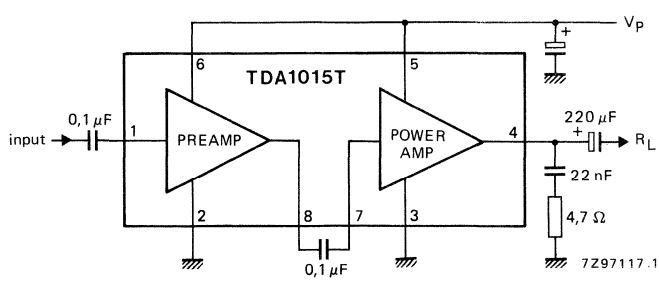


Fig. 8 Application circuit for preamplifier and power amplifier stages and battery power supply; $G_{v\,tot}$ = 52 dB; $|Z_{i2}|$ = 200 kΩ.

SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 14)	V_P		6 to 23	V
Operating ambient temperature	T_{amb}		−30 to + 80	°C
Supply voltage (pin 14)	V_P	typ.	20	V
Current consumption	I_{14}	typ.	3,5	mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6	V
Voltage gain	G_v	typ.	1	
Total harmonic distortion	d_{tot}	typ.	0,01	%
Crosstalk	α	typ.	70	dB
Signal-to-noise ratio	S/N	typ.	120	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

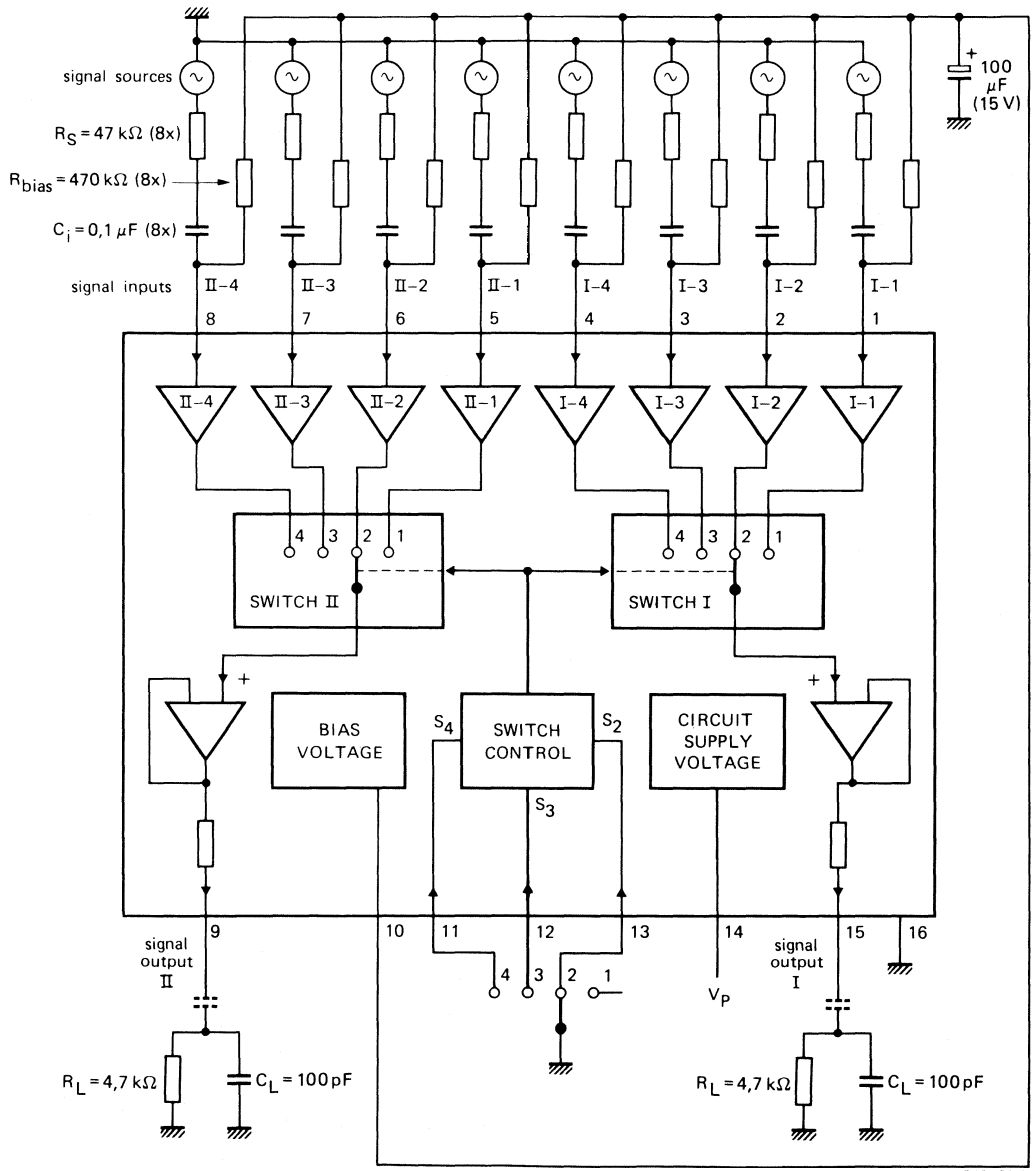


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	V_P	max.	23	V
Input voltage (pins 1 to 8)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

V_P = 20 V; T_{amb} = 25 °C; unless otherwise specified

Current consumption				
without load; $I_g = I_{15} = 0$	I_{14}	typ.	3,5	mA
			2 to 5	mA
Supply voltage range (pin 14)	V_P		6 to 23	V
Signal inputs				
Input offset voltage of switched-on inputs $R_S \leqslant 1$ kΩ	V_{io}	typ.	2	mV
		<	10	mV
Input offset current of switched-on inputs	I_{io}	typ.	20	nA
		<	200	nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	I_{io}	typ.	20	nA
		<	200	nA
Input bias current independent of switch position	I_i	typ.	250	nA
		<	950	nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ	SVRR	typ.	100	μV/V
Equivalent input noise voltage $R_S = 0$; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	μV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at R_S = 1 kΩ; f = 1 kHz	α	typ.	100	dB

CHARACTERISTICS (continued)

Signal amplifier

Voltage gain of a switched-on input at $I_9 = I_{15} = 0$; $R_L = \infty$	G_v	typ.	1
Current gain of a switched-on amplifier	G_i	typ.	10^5

Signal outputs

Output resistance (pins 9 and 15)	R_o	typ.	400 Ω
Output current capability at V_P = 6 to 23 V	$\pm I_9$; $\pm I_{15}$	typ.	5 mA
Frequency limit of the output voltage $V_{i(p-p)}$ = 1 V; R_S = 1 kΩ; R_L = 10 MΩ; C_L = 10 pF	f	typ.	1,3 MHz
Slew rate (unity gain); $\Delta V_{9\text{-}16}/\Delta t$; $\Delta V_{15\text{-}16}/\Delta t$ R_L = 10 MΩ; C_L = 10 pF	S	typ.	2 V/μs

Bias voltage

D.C. output voltage	$V_{10\text{-}16}$	typ. 10,2 to 11,8	11 V * V
Output resistance	$R_{10\text{-}16}$	typ.	8,2 kΩ

Switch control

switched-on inputs	interconnected pins	control voltages		
		$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1{,}5$ V.

Control inputs (pins 11, 12 and 13)

Required voltage			
HIGH	V_{SH}	>	3,3 V **
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 μA
LOW (control current)	$-I_{SL}$	<	250 μA

* $V_{10\text{-}16}$ is typically $0{,}5 \cdot V_{14\text{-}16} + 1{,}5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5	dB
Output voltage variation when switching the inputs	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	typ. <	10 100	mV mV
Total harmonic distortion				
over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01	%
V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02	%
V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03	%
Output signal handling				
d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	> typ.	5,0 5,3	V V
Noise output voltage (unweighted)				
f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5	μV
Noise output voltage (weighted)				
f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12	μV
Amplitude response				
V_i = 5 V; f = 20 Hz to 20 kHz; C_i = 0,22 μF	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	<	0,1	dB *
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75	dB **
Crosstalk between switched-on inputs and the outputs of the other channels	α	typ.	90	dB **

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

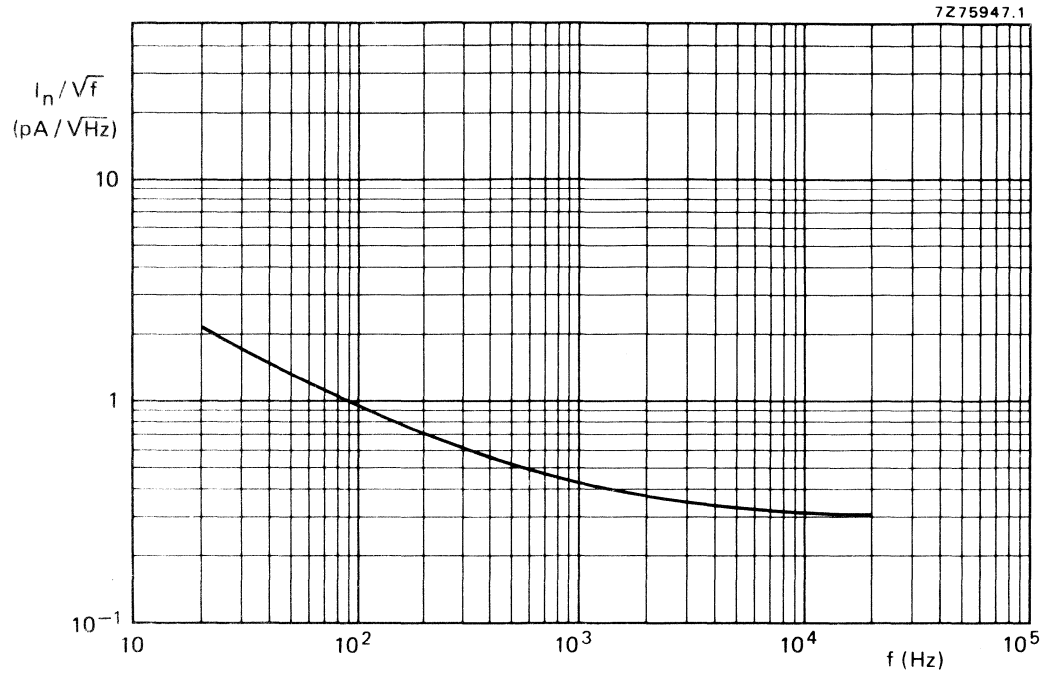


Fig. 2 Equivalent input noise current.

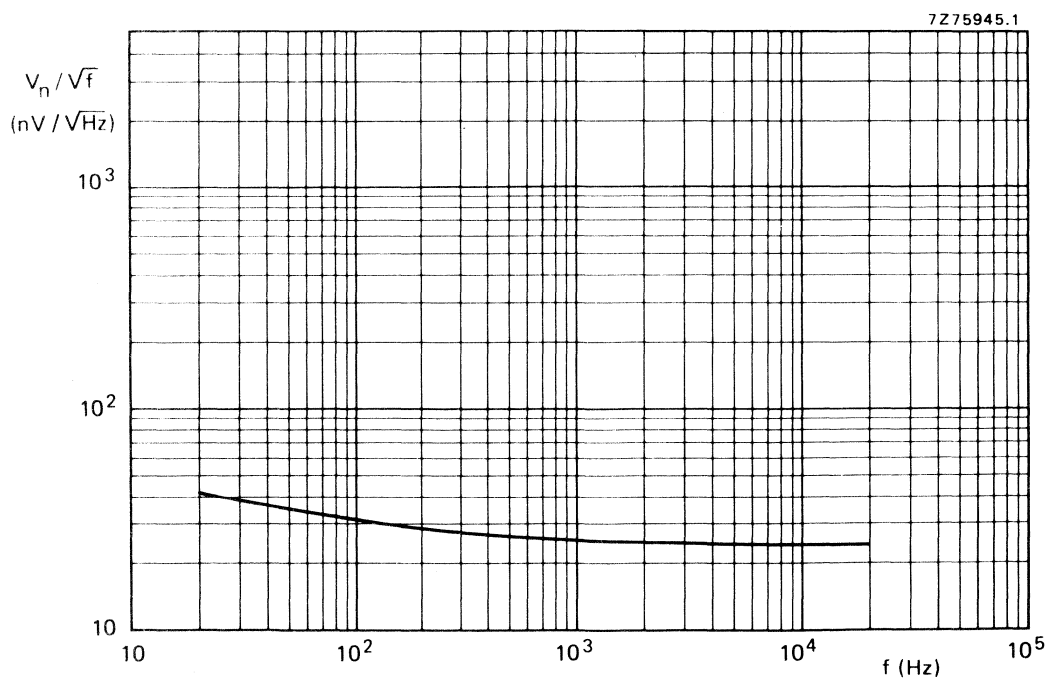


Fig. 3 Equivalent input noise voltage.

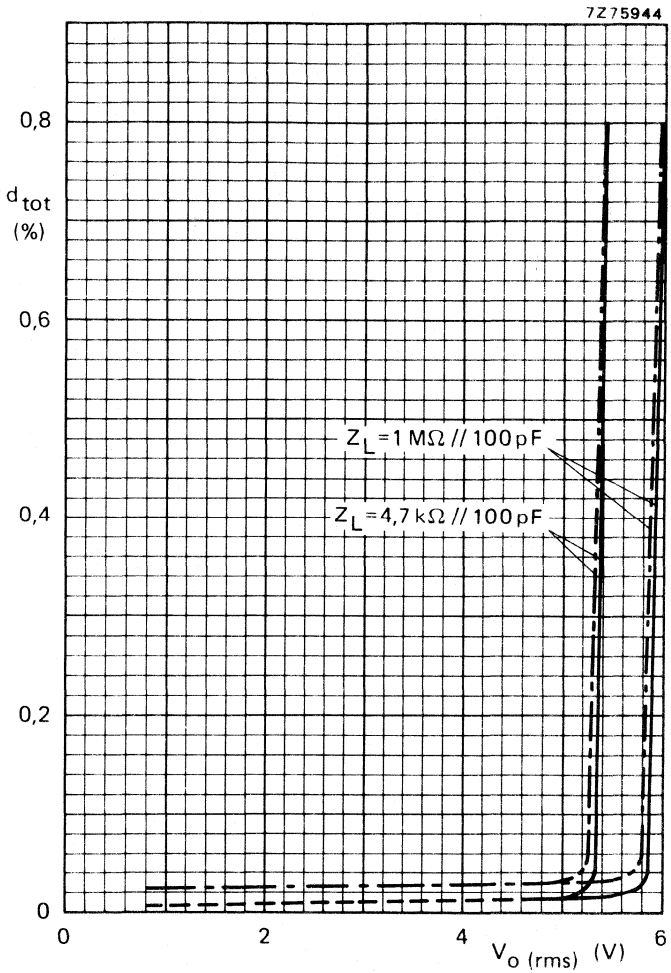


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; —— - —— - f = 20 kHz.

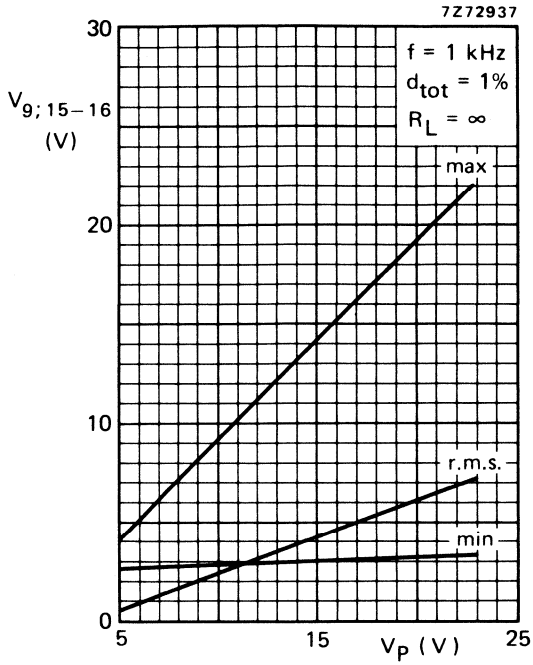


Fig. 5 Output voltage as a function of supply voltage.

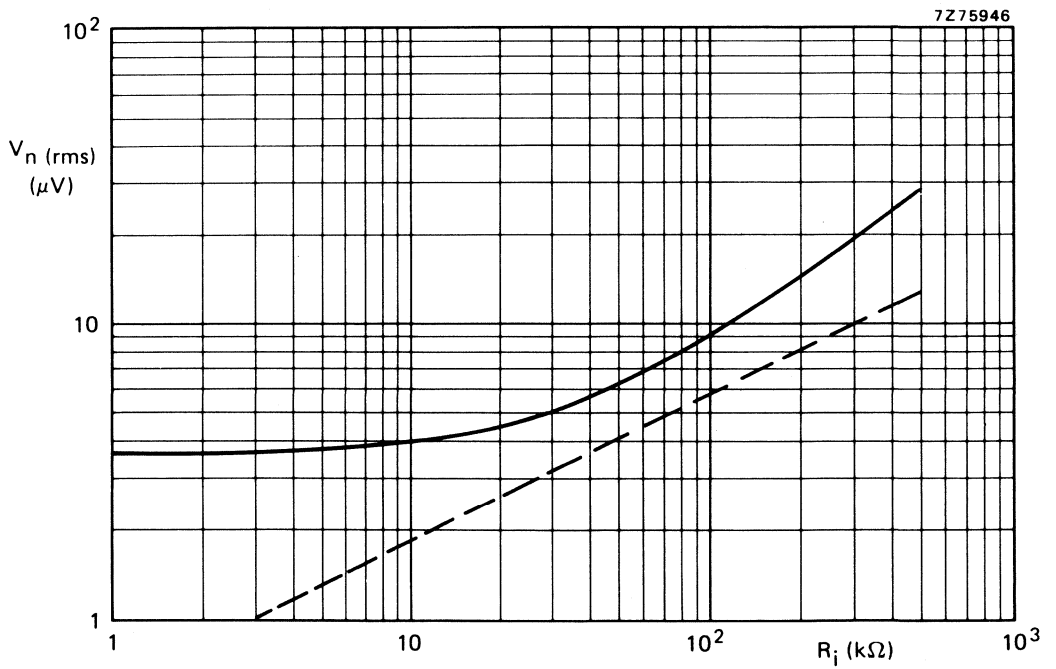


Fig. 6 Noise output voltage as a function of input resistance; G_v = 1; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

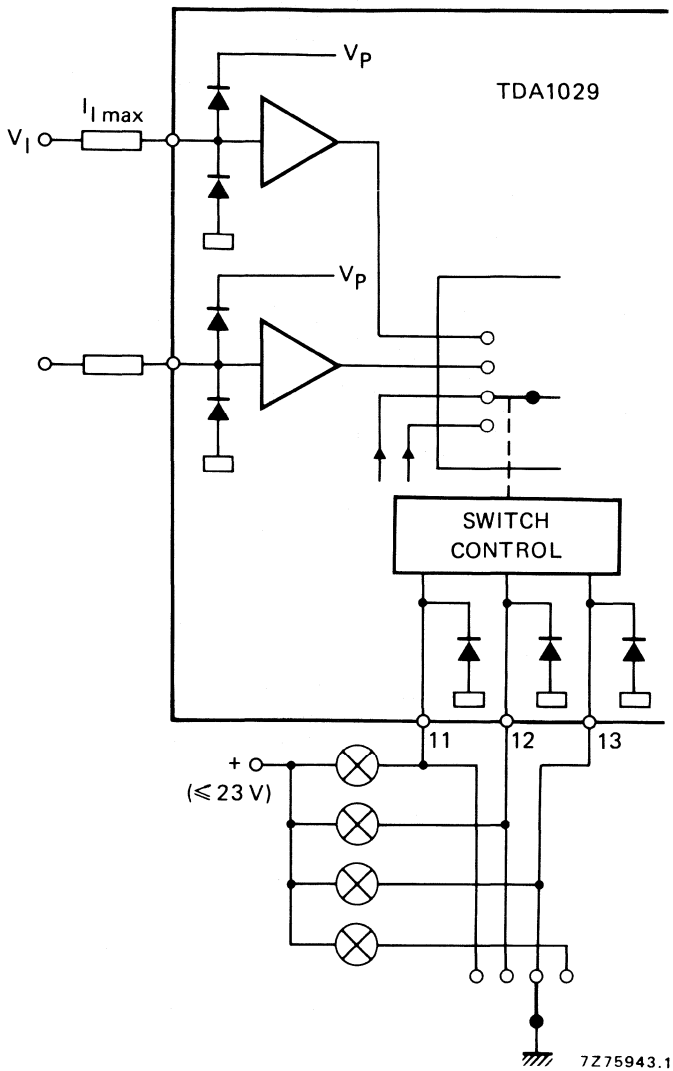


Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1\ \mu A$), as well as, when the supply voltage (pin 14) is switched off.

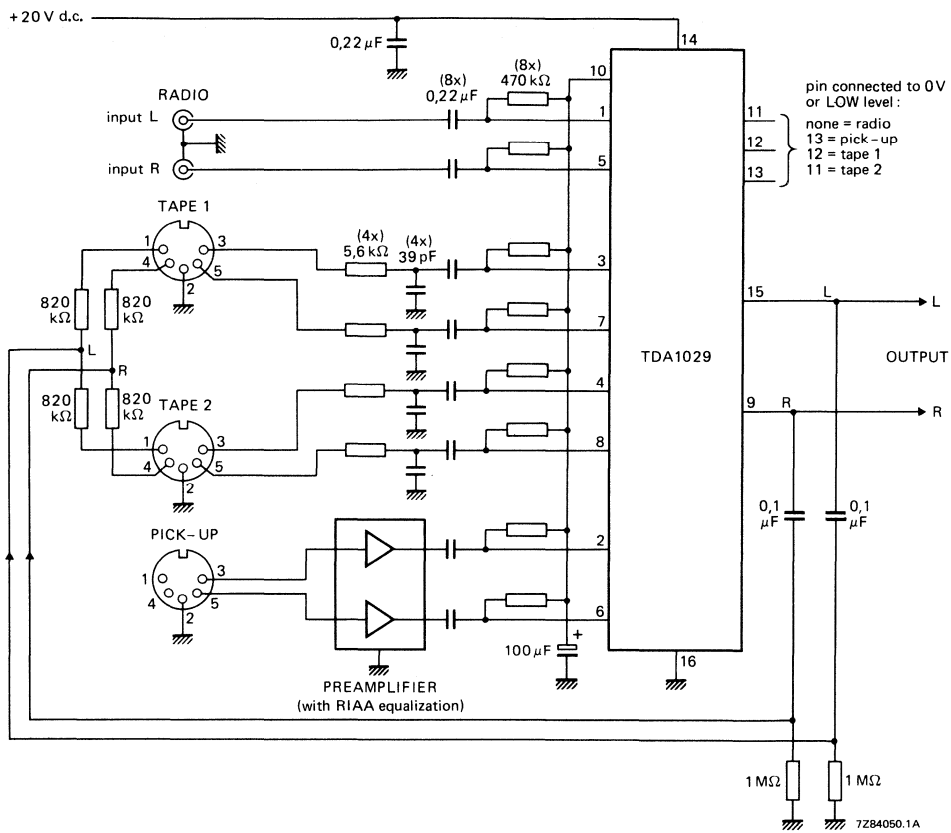


Fig. 8 TDA1029 connected as a four input stereo source selector.

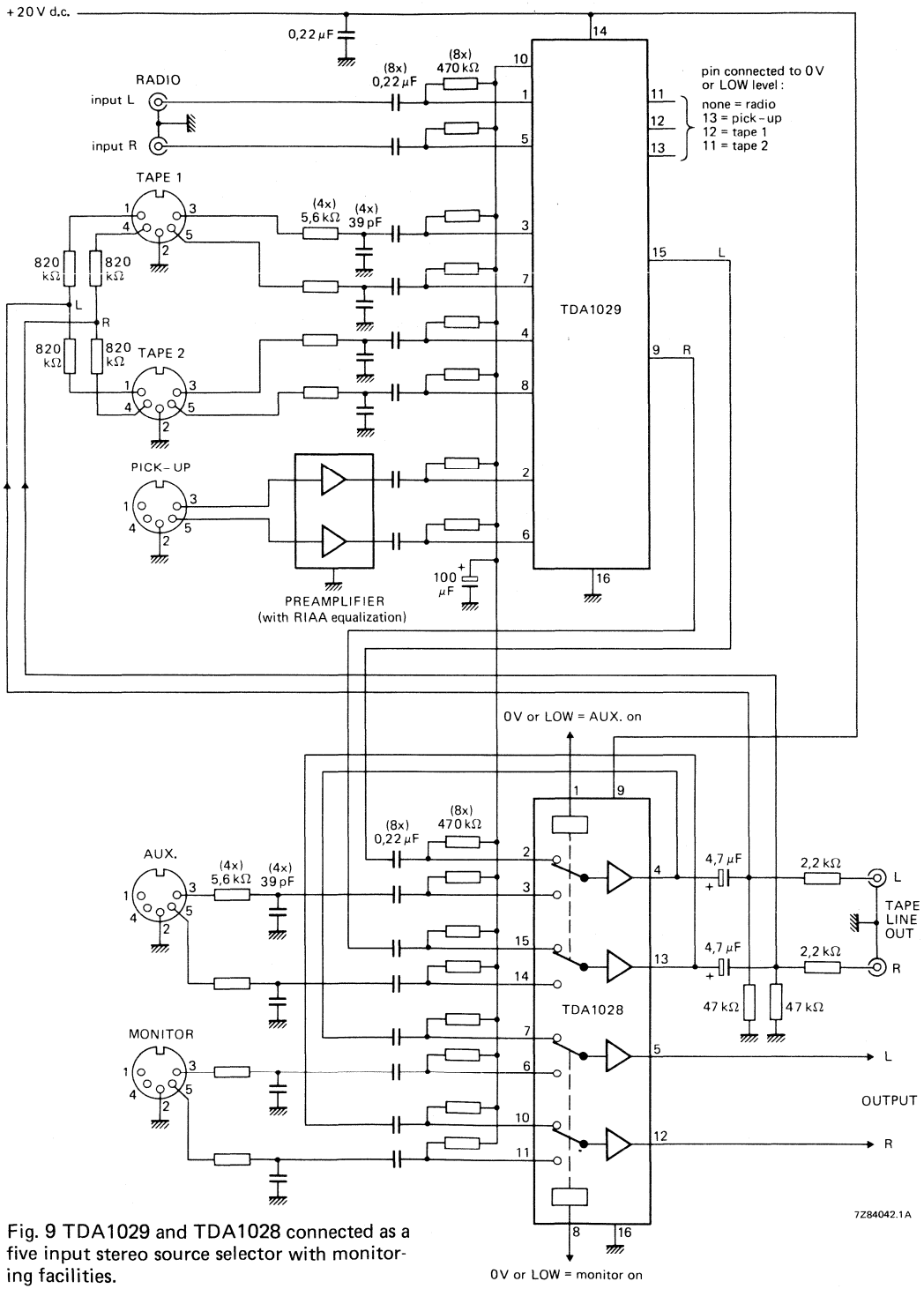


Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

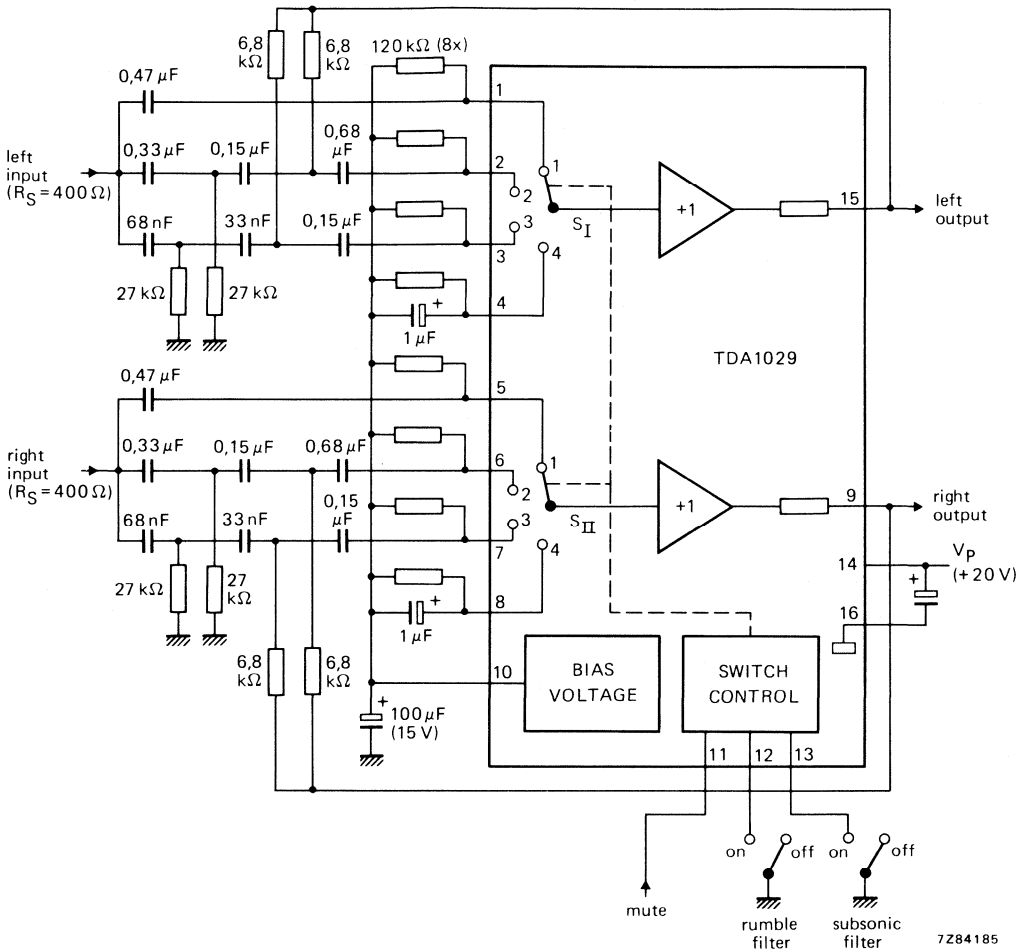


Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

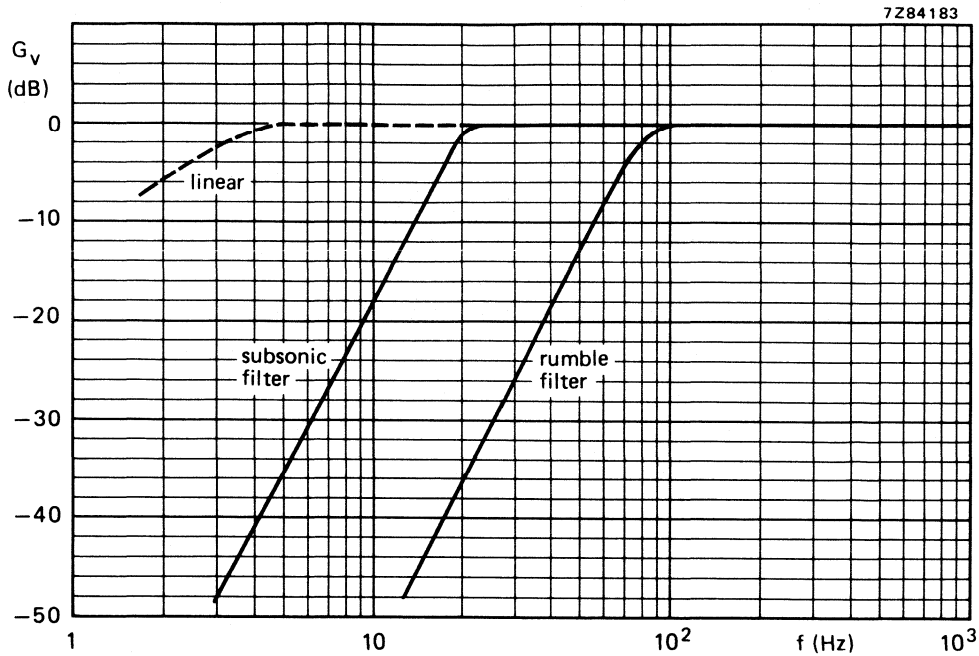


Fig. 11 Frequency response curves for the circuit of Fig. 10.

EAST-WEST CORRECTION DRIVER CIRCUIT

The TDA1082 is a monolithic integrated circuit driving east-west correction of colour tubes in television receivers. The circuit can be used for class-A and class-D operation and incorporates the following functions:

- differential input amplifier
- squaring stage
- differential output amplifier with driver stage
- protection stage with threshold
- switching off the correction during flyback
- voltage stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 1)	V_P	typ.	12	V
Current consumption	I_P	typ.	17	mA
Total power dissipation	P_{tot}	max.	600	mW
Operating ambient temperature range	T_{amb}		0 to + 70	°C
Collector voltage drift external transistor	ΔV_C	typ.	0,7	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

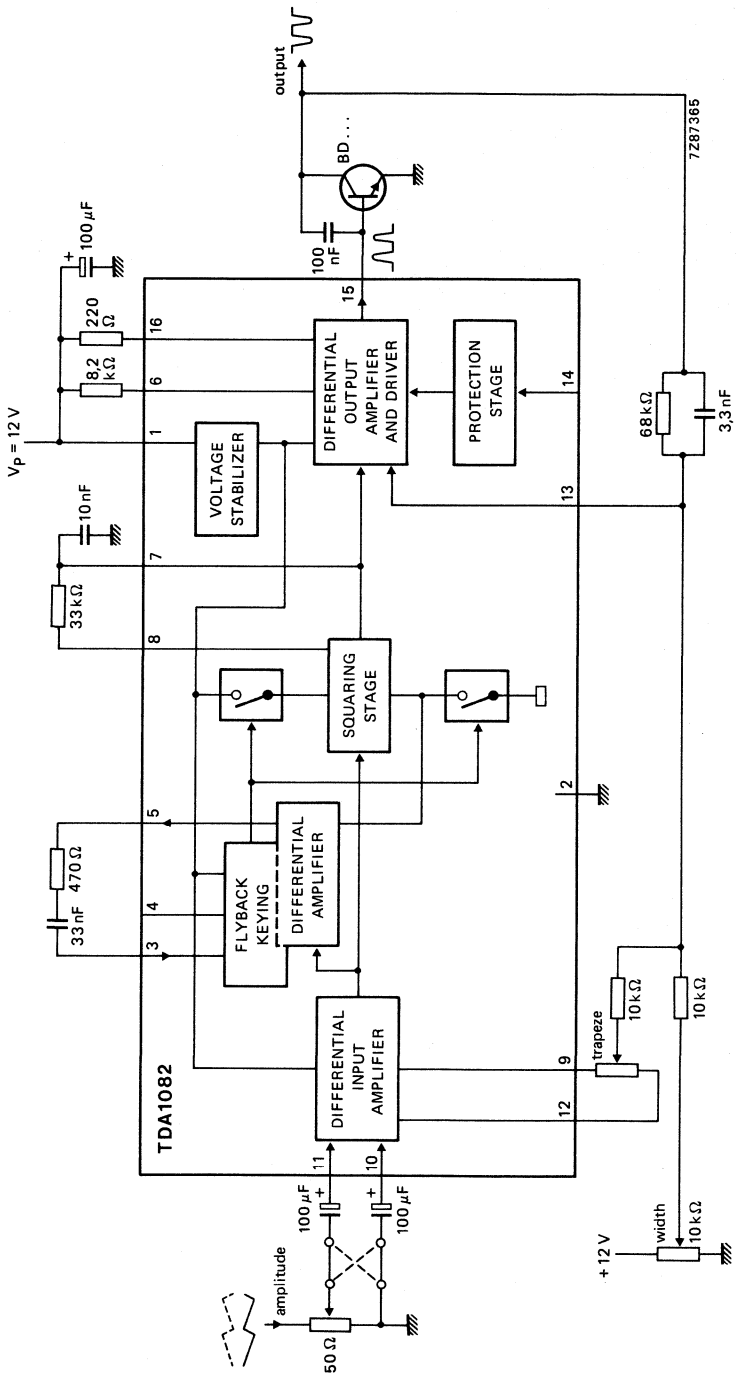


Fig. 1 Block diagram with external components (class-A operation). Also used as test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	V_P	max.	16 V
Output current (pin 15)	$-I_O$	max.	50 mA
Total power dissipation	P_{tot}	max.	600 mW
Storage temperature range	T_{stg}	−25 to +150	°C
Operating ambient temperature range	T_{amb}	0 to +70	°C ←

Voltages

with respect to ground (pin 2)	min.	max.
Pins 1, 5, 7, 8, 9, 12, 13 and 16	0	16 V
Pins 3 and 4	0	− V
Pins 10, 11 and 15	0	5 V

Currents

Pins 3, 4 and 6	−	5 mA
Pin 14	0	1,5 mA
Pins 15 and 16 ($-I_{15}$ and $+I_{16}$)	0	50 mA

CHARACTERISTICS

V_P = 12 V (range 10,5 to 14 V); T_{amb} = 25; measured in circuit Fig. 1 with colour tube A66-500X; unless otherwise specified

Supply

Voltage range	V_P	10,5 to	14 V
Voltage peak value	V_{PM}	max.	15 V
Current range	I_P	11 to	30 mA
Current typical value	I_P	typ.	17 mA

Sawtooth signal (pin 10 or 11)

Input voltage d.c. value	V_i	typ.	2,5 V
Input resistance	R_i	typ. <	5,6 kΩ 7,0 kΩ

Correcting signals (pin 13)

Input voltage d.c. value	V_{13}	typ.	0,6 V
Input current	I_{13}	typ.	0,5 mA

Flyback keying (pin 3)

Input current range	I_3	0,05 to	5 mA
Peak value, d = 5%	I_3	typ.	20 mA

Threshold (pin 14)

Input voltage at I_{14} = 200 μA for switching off the driver stage	V_i	typ. 7,2 to	8 V 8,8 V

Output stage (pin 6)			
Generator current	I_6	typ.	1 mA
Flyback differential amplifier (pin 5)			
D.C. value output voltage	V_5	typ.	6 V
Output resistance	R_5	typ.	5,6 kΩ
Squaring stage (pin 7)			
D.C. value output voltage	V_7	typ.	6 V
Peak to peak value output voltage	$V_{7(p-p)}$	typ.	1,5 V
Output resistance	R_7	5,6 to typ.	9,4 kΩ 7,5 kΩ
Correction trapezoidal deformation (pins 9 and 12)			
D.C. voltage	$V_{9,12}$	typ.	5 V
Output resistance	$R_{9,12}$	typ.	7,5 kΩ
Driver output (pin 15)			
Output current	$-I_{15}$	<	50 mA
Drift of d.c. collector voltage			
Of external transistor in closed loop T_{amb} = 15 to 70 °C; V_{CO} = 8 V	ΔV_C	typ.	0,7 V

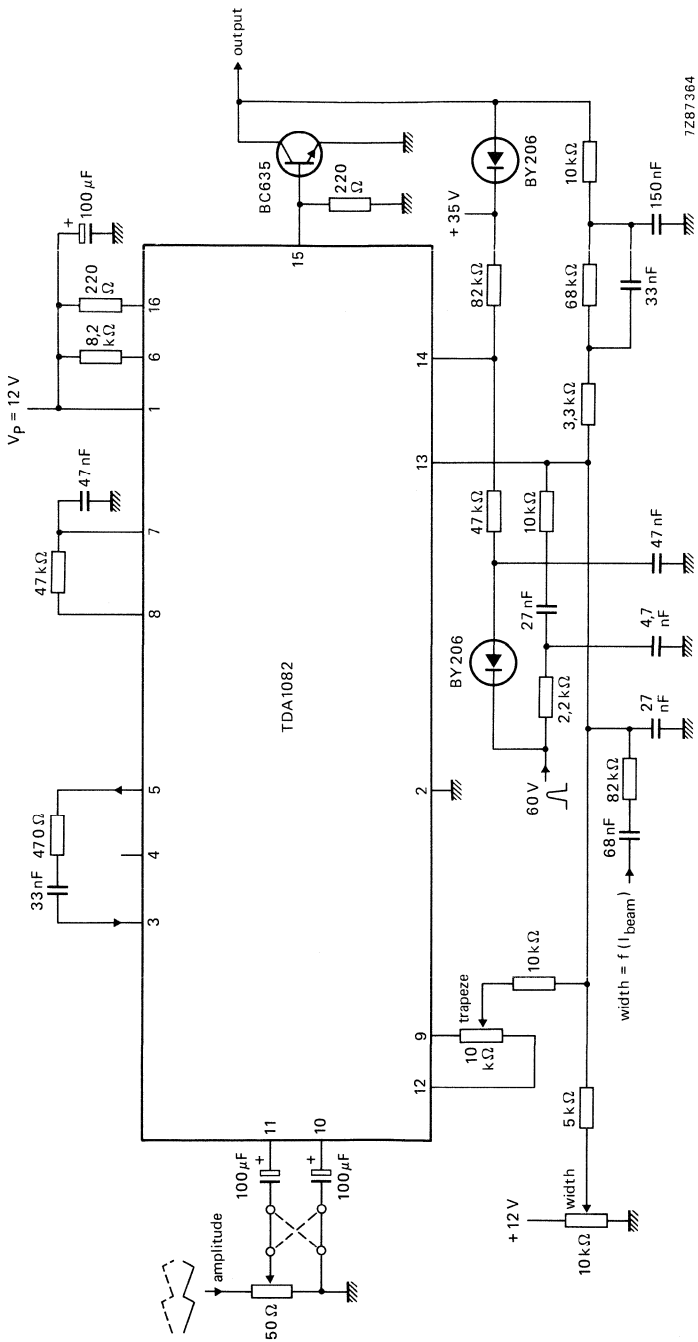


Fig. 2 Application circuit E-W-correction (class-D operation).

12 to 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35	V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65	mA
Output power at d_{tot} = 0,7%				
sine-wave power				
V_P = 25 V; R_L = 4 Ω	P_o	typ.	13	W
V_P = 25 V; R_L = 8 Ω	P_o	typ.	7	W
music power				
V_P = 32 V; R_L = 4 Ω	P_o	typ.	21	W
V_P = 32 V; R_L = 8 Ω	P_o	typ.	12	W
Closed-loop voltage gain (externally determined)	G_c	typ.	30	dB
Input resistance (externally determined)	R_i	typ.	20	kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ.	72	dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	50	dB

PACKAGE OUTLINES

TDA1512: 9-lead SIL; plastic power (SOT-131B).
TDA1512Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157B).

PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Ground potential
5. Output
6. Positive supply (V_P)
7. Externally connected to pin 6
8. Ripple rejection
9. Inverting input (feedback)

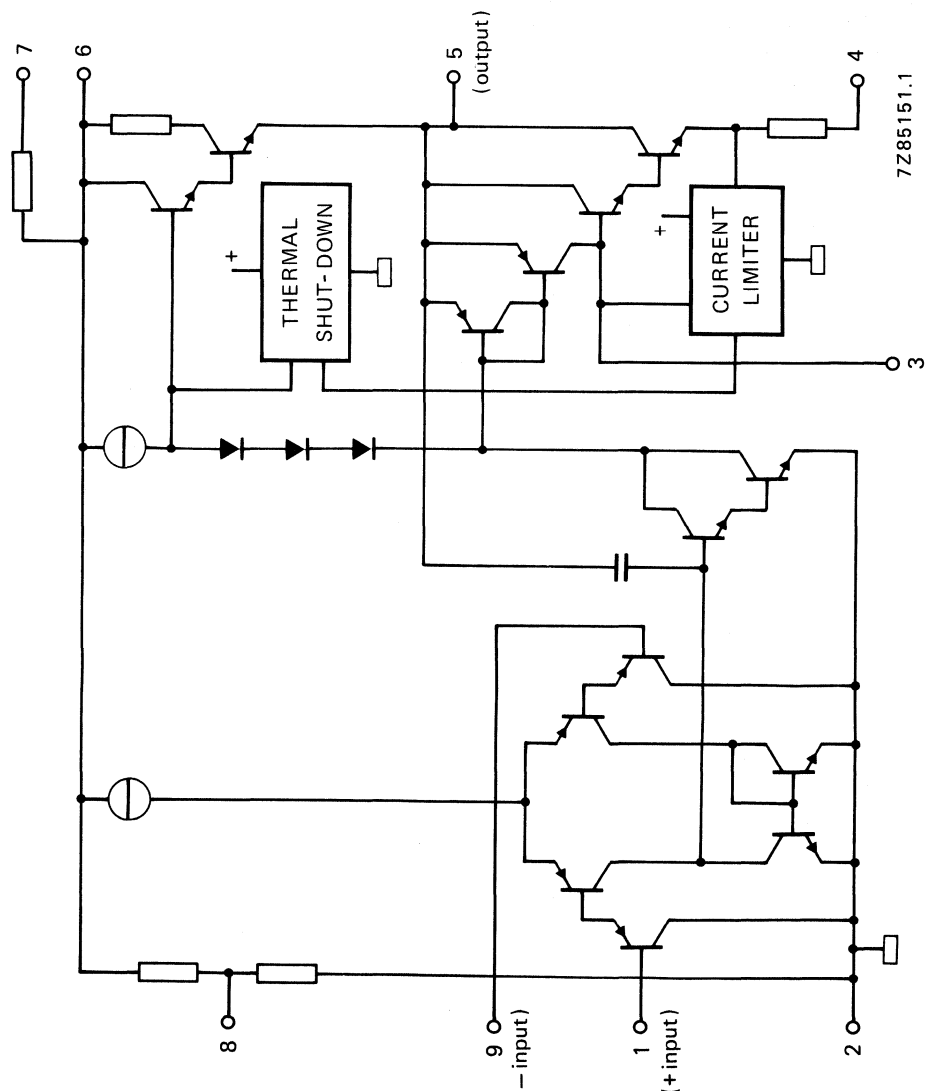
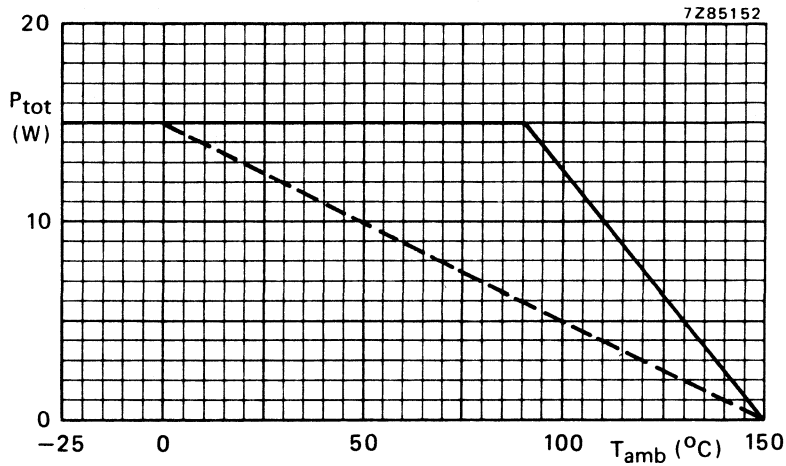


Fig. 1 Simplified internal circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Repetitive peak output current	I_{ORM}	max.	3,2 A
Non-repetitive peak output current	I_{OSM}	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 30$ V with $R_i = 4\ \Omega$	t_{sc}	max.	100 hours



——— mounted on infinite heatsink.

– – – – mounted on heatsink of 6 K/W.

Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	typ.	3 K/W
		⩽	4 K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA

A.C. CHARACTERISTICS

V_P = 25 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power			
sine-wave power at d_{tot} = 0,7 %			
R_L = 4 Ω	P_o	typ.	13 W
R_L = 8 Ω	P_o	typ.	7 W
music power at V_P = 32 V			
R_L = 4 Ω; d_{tot} = 0,7 %	P_o	typ.	21 W
R_L = 4 Ω; d_{tot} = 10 %	P_o	typ.	25 W
R_L = 8 Ω; d_{tot} = 0,7 %	P_o	typ.	12 W
R_L = 8 Ω; d_{tot} = 10 %	P_o	typ.	15 W
Power bandwidth; −1,5 dB; d_{tot} = 0,7%	B		40 Hz to 16 kHz
Voltage gain			
open-loop	G_o	typ.	74 dB
closed-loop	G_c	typ.	30 dB
Input resistance (pin 1)	R_i	>	100 kΩ
Input resistance of test circuit (Fig. 3)	R_i	typ.	20 kΩ
Input sensitivity			
for P_o = 50 mW	V_i	typ.	16 mV
for P_o = 10 W	V_i	typ.	210 mV
Signal-to-noise ratio			
at P_o = 50 mW; R_S = 2 kΩ; f = 20 Hz to 20 kHz; unweighted	S/N	>	68 dB
weighted; measured according to IEC 173 (A-curve)	S/N	typ.	76 dB
Ripple rejection at f = 100 Hz	RR	typ.	50 dB
Total harmonic distortion at P_o = 10 W	d_{tot}	typ. <	0,1 % 0,3 %
Output resistance (pin 5)	R_o	typ.	0,1 Ω

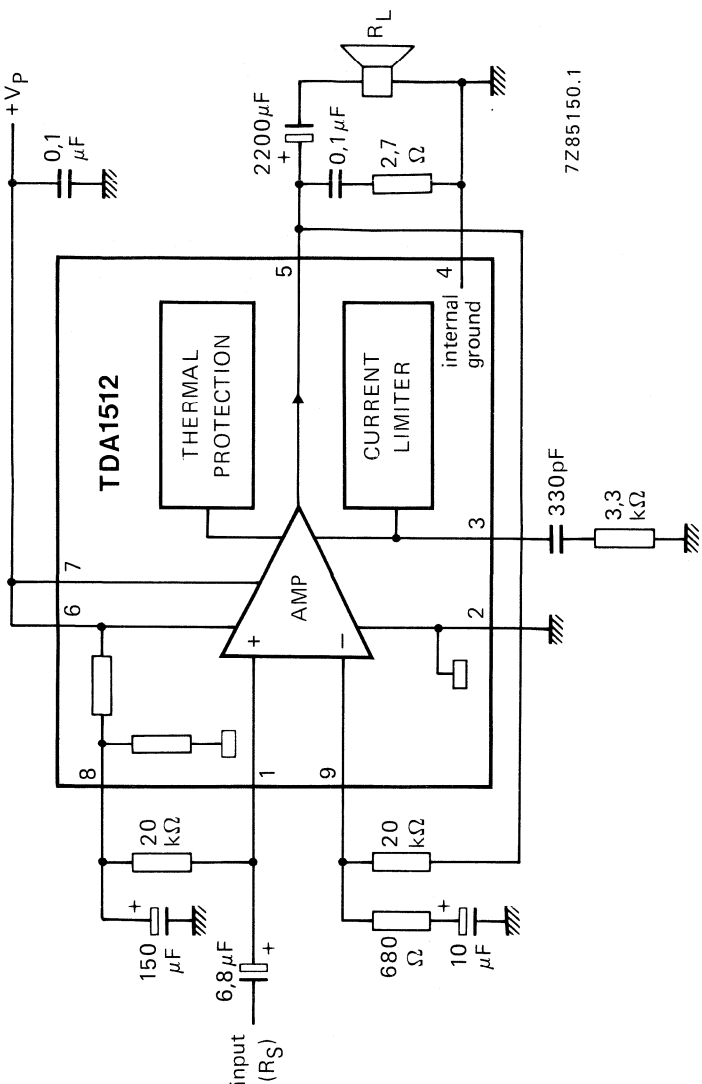


Fig. 3 Test circuit.

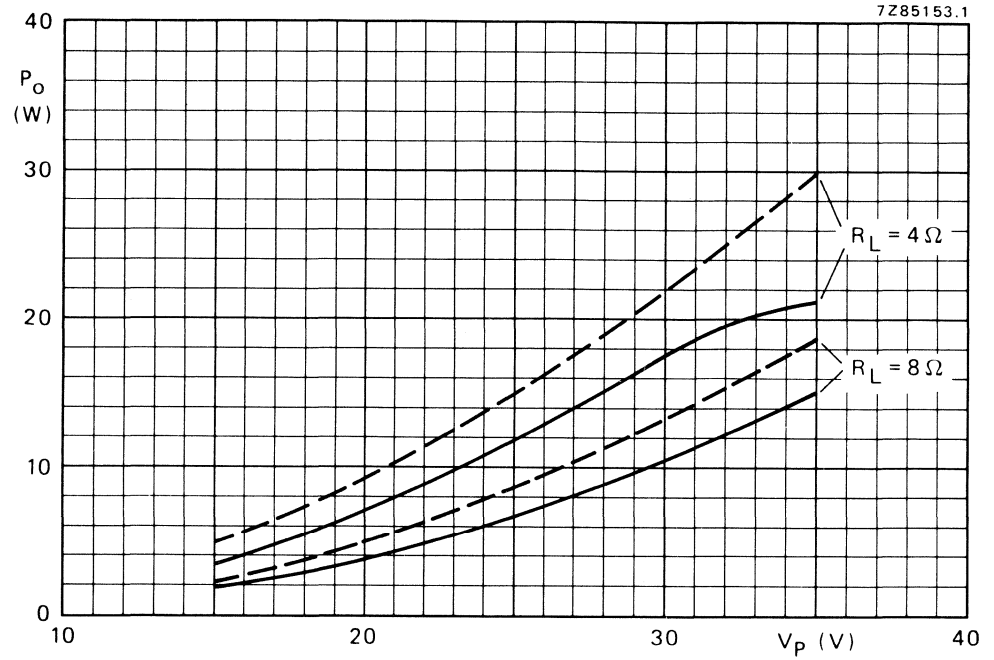


Fig. 4 Output power as a function of the supply voltage; f = 1 kHz;
——— d_{tot} = 0,7 %; – – – d_{tot} = 10 %.

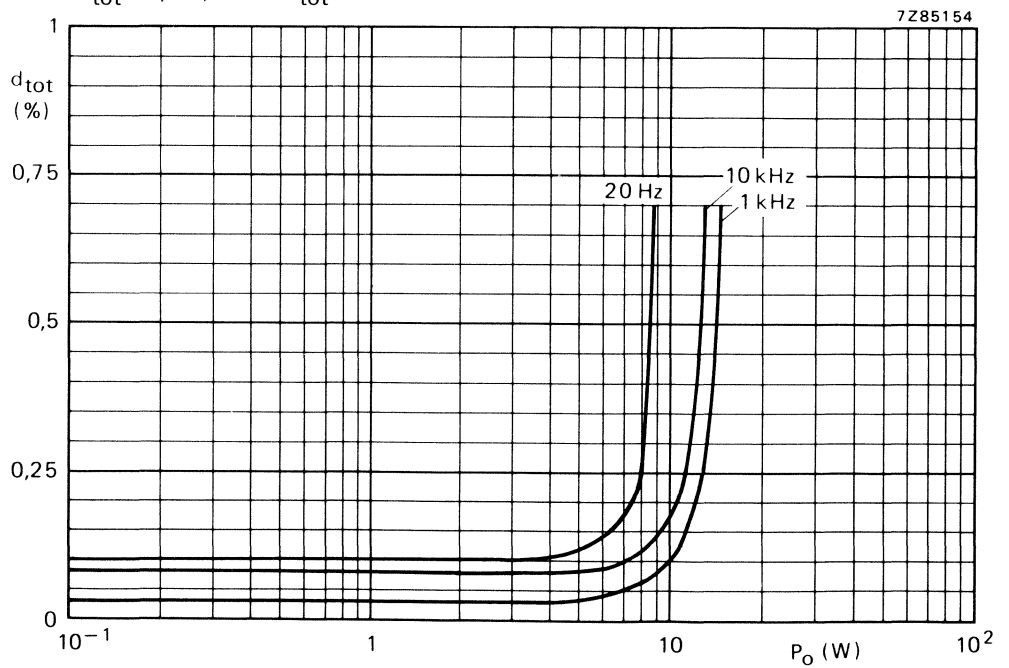


Fig. 5 Total harmonic distortion as a function of the output power.

40 W HIGH-PERFORMANCE HI-FI AMPLIFIER

The TDA1514 integrated circuit is a hi-fi power amplifier for use as a building block in radio, tv and audio recorder applications. The high performance of the IC meets the requirements of digital sources (e.g. Compact Disc equipment).

The circuit is totally protected, the two output transistors both having thermal and SOAR protection. The circuit also has a mute function that can be arranged to operate for a period after power-on with a delay time fixed by external components.

The device is intended for symmetrical power supplies but an asymmetrical supply may also be used.

The theoretical maximum power dissipation with a stabilized power supply is $(V_P - V_N)^2/2\pi^2 R_L = 19$ W, where $V_P = +27{,}5$ V, $V_N = -27{,}5$ V and $R_L = 8\ \Omega$. Considering, for example, a maximum ambient temperature of 50 °C and a maximum junction temperature of 150 °C, the total thermal resistance $R_{th\ j\text{-}a}$ is (150 - 50)/19 = 5,3 K/W. Since the thermal resistance of the SOT-131A encapsulation is $< 1{,}5$ K/W, the thermal resistance required of the heatsink is $< 3{,}8$ K/W. Thus the maximum output power, and therefore the music power output, is limited only by the supply voltage and not by the heatsink.

QUICK REFERENCE DATA

Supply voltage range (pin 6 to pin 4)	$V_P - V_N$		15 to 60 V
Total quiescent current at $V_P - V_N = 55$ V	I_{tot}	typ.	60 mA
Output power at THD = −60 dB; $V_P - V_N = 55$ V; $R_L = 8\ \Omega$	P_o	typ.	40 W
Closed loop voltage gain (determined externally)	G_c	typ.	30 dB
Input resistance (determined externally)	R_I	typ.	20 kΩ
Signal-to-noise ratio at $P_o = 50$ mW	(S+N)/N	typ.	82 dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	72 dB

PACKAGE OUTLINE

9-lead SIL; plastic power (SOT-131A).

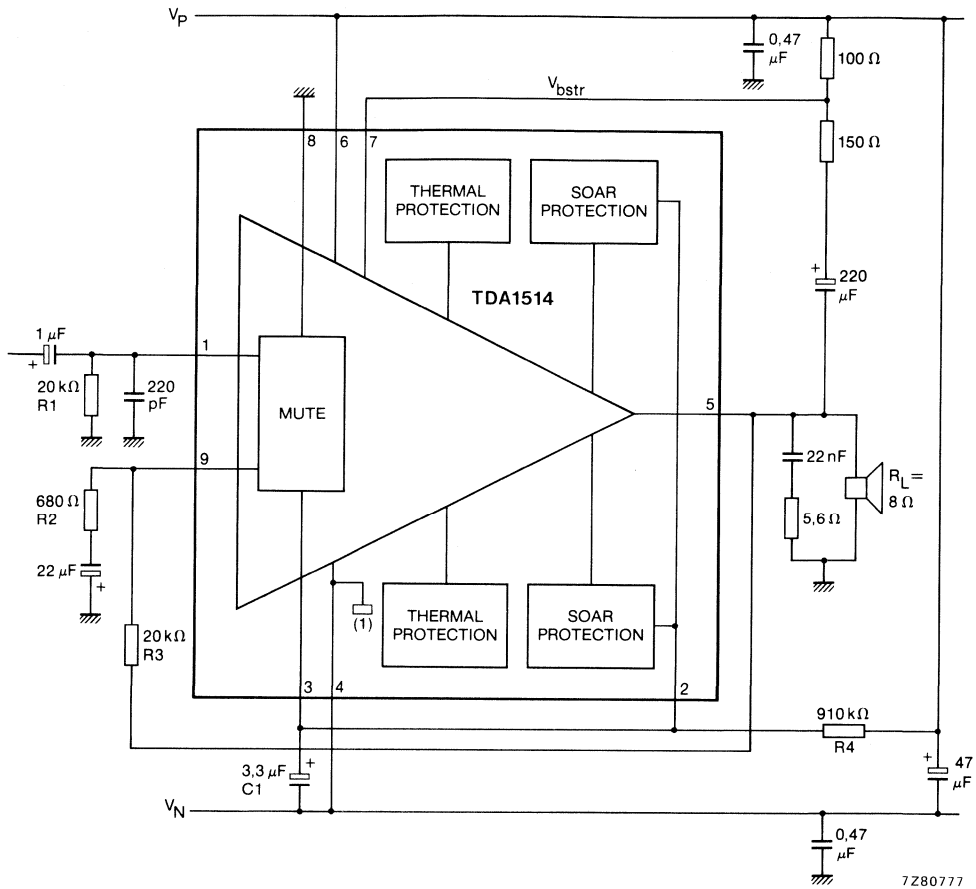


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage (pin 6 to pin 4)	$V_P - V_N$	60 V
Bootstrap voltage (pin 7 to pin 4)	V_{bstr}	70 V
Output current (repetitive peak)	I_o	4,0 A
Operating ambient temperature range	T_{amb}	−25 to + 150 °C
Storage temperature range	T_{stg}	−55 to + 150 °C
Power dissipation	See Fig. 2	
Thermal shut-down protection time	t_{pr}	1 hour
Short-circuit protection time*	t_{sc}	10 min
Mute voltage (pin 3 to pin 4)	V_M	7 V

* Driven by a pink-noise voltage.
Symmetrical power supply: a.c. and d.c. short-circuit protected.
Asymmetrical power supply: a.c. short-circuit protected.

THERMAL RESISTANCE

From junction to case $R_{th\ j\text{-}c}$ max. 1,5 K/W

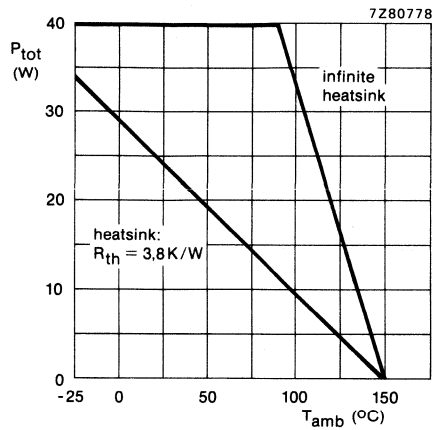


Fig. 2 Power derating curve.

DEVELOPMENT DATA

CHARACTERISTICS

V_P = +27,5 V; V_N = −27,5 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified; test circuit as per Fig. 1.

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6 to pin 4)	$V_P - V_N$	15	–	60	V
Maximum output current (peak value)	I_{OMmax}	3,2	–	–	A
Total quiescent current	I_{tot}	30	60	90	mA
Output power with THD = −60 dB:					
at $V_P - V_N$ = 55 V	P_o	37	40	–	W
at $V_P - V_N$ = 44 V	P_o	–	25	–	W
at $V_P - V_N$ = 32 V	P_o	–	–	12,5	W
Total harmonic distortion at P_o = 32 W	THD	–	−90	−80	dB
Intermodulation distortion at P_o = 32 W (note 1)	d_{im}	–	−80	–	dB
Power bandwidth (−3 dB) at THD = −60 dB	B	–	20 to 25k	–	Hz
Slew rate	dV/dt	–	15	–	V/μs
Closed loop voltage gain (note 2)	G_c	29,2	29,7	30,2	dB
Open loop voltage gain	G_o	–	85	–	dB
Input impedance (note 3)	Z_i	1	–	–	MΩ
S/N related to P_o = 4 mW (note 4)	(S+N)/N	80	–	–	dB
Input offset voltage	$\pm V_{io}$	–	3	–	mV
Input offset bias current	$\pm I_{io(b)}$	–	0,2	1	μA
Input bias current	$+ I_{ib}$	–	1	5	μA
Output impedance	Z_o	–	–	0,1	Ω
Supply voltage ripple rejection at ripple frequency = 100 Hz; ripple voltage (r.m.s. value) = 500 mV; source resistance = 2 kΩ	RR	70	–	–	dB
Mute time (note 5)	t_M	–	1,25	–	s
Mute-on voltage (pin 3 to pin 4)	$V_{M(on)}$	0	–	5	V
Mute-off voltage (pin 3 to pin 4)	$V_{M(off)}$	6	–	7	V
Quiescent current into pin 2 (note 6)	$I_{2\,tot}$	tbf	20	tbf	μA

Notes to the characteristics

1. Measured with two superimposed signals of 50 Hz and 7 kHz with an amplitude relationship of 4 : 1.
2. The closed loop gain is determined by external resistors (Fig. 1, R2 and R3) and is variable between 20 and 46 dB.
3. The input impedance in the test circuit (Fig. 1) is determined by the bias resistor R1.
4. The noise voltage at the output is measured in the band 20 Hz to 20 kHz and source resistance $R_S = 2\ k\Omega$.
5. Determined by R4 and C1.
6. The quiescent current into pin 2 determines (with the value of R4) the minimum power supply voltage at which the mute function remains in operation:

   $V_P - V_N = I_{2\,tot} \times R4 + V_{m(on)max}$.

DEVELOPMENT DATA

20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1520 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Very low intermodulation distortion
- Very low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package
- A.C. short-circuit protected

QUICK REFERENCE DATA

Supply voltage range	V_P	15 to 40	V
Total quiescent current at V_P = 33 V	I_{tot}	typ. 54	mA
Output power at d_{tot} = 0,5% sine-wave power			
V_P = 33 V; R_L = 4 Ω	P_o	typ. 22	W
V_P = 33 V; R_L = 4 Ω	P_o	> 16	W
V_P = 33 V; R_L = 8 Ω	P_o	typ. 11	W
Closed-loop voltage gain (externally determined)	G_c	typ. 30	dB
Input resistance (externally determined by R_{8-1})	R_i	typ. 20	kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ. 75	dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ. 60	dB

PACKAGE OUTLINE

TDA1520 : 9-lead SIL; plastic power (SOT-131A).
TDA1520Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157A).

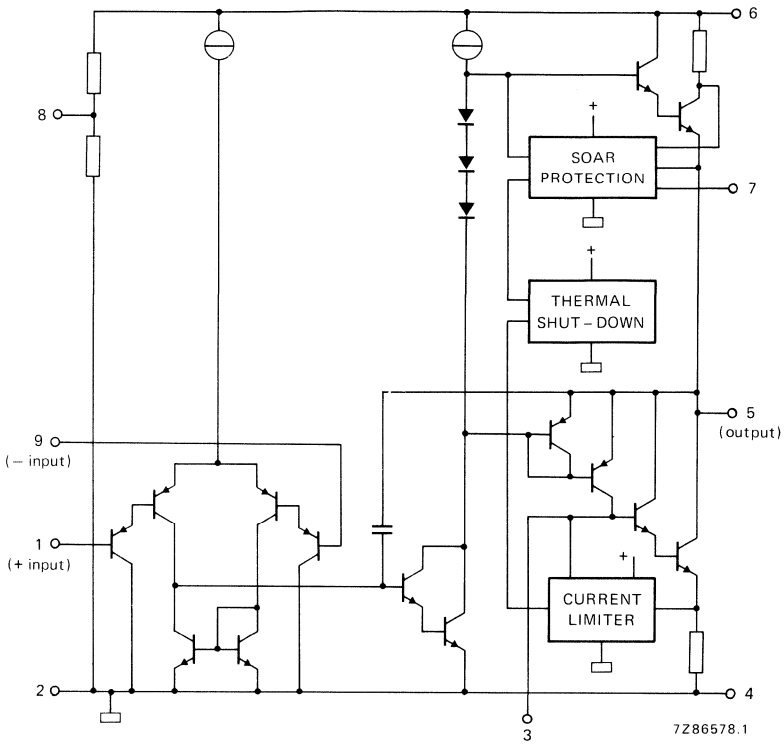


Fig. 1 Simplified internal circuit diagram.

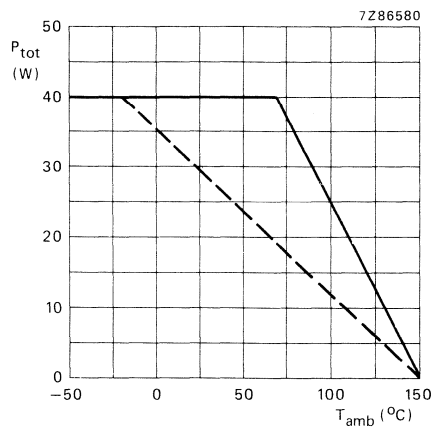
PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Negative supply (ground)
5. Output
6. Positive supply (V_P)
7. Internally connected
8. Ripple rejection
9. Inverting input (feedback)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	44 V
Repetitive peak output current	I_{ORM}	max.	4 A
Non-repetitive peak output current	I_{OSM}	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 28$ V with $R_i = 4\ \Omega$ and $f > 20$ Hz	t_{sc}	max.	1 hour



——— mounted on infinite heatsink.
– – – mounted on heatsink of 2,3 K/W.

Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	⩽	2 K/W

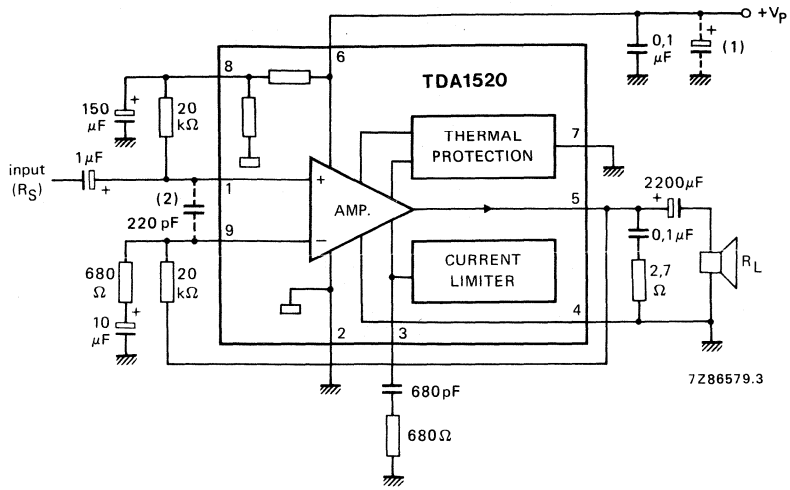
D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 40	V
Total quiescent current at V_P = 33 V	I_{tot}		22 to 105	mA
		typ.	54	mA

A.C. CHARACTERISTICS

V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power				
sine-wave power at d_{tot} = 0,5%				
R_L = 4 Ω	P_o	typ.	22	W
R_L = 4 Ω	P_o	>	16	W
R_L = 8 Ω	P_o	typ.	11	W
Power bandwidth; −3 dB; d_{tot} = 0,5%	B	20 Hz to	20	kHz
Voltage gain				
open-loop	G_o	typ.	74	dB
closed-loop	G_c	typ.	30	dB
Input resistance (pin 1)	R_i	>	1	MΩ
Input resistance of test circuit (Fig. 3)	R_i	typ.	20	kΩ
Input sensitivity				
for P_o = 50 mW	V_i	typ.	16	mV
for P_o = 16 W	V_i	typ.	260	mV
Signal-to-noise ratio				
at P_o = 50 mW; R_S = 2 kΩ; f = 20 Hz to 20 kHz; unweighted	S/N	typ.	75	dB
weighted; measured according to IEC 179 (A-curve)	S/N	typ.	80	dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	65	dB
Total harmonic distortion at P_o = 16 W	d_{tot}	typ.	0,01	%
Output resistance (pin 5)	R_o	typ.	0,01	Ω
	R_o	<	0,1	Ω



(1) Belongs to power supply.
(2) In application to improve radio interference suppression.

Fig. 3 Test circuit/basic application circuit.

20 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1520A is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.

Features

- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package
- A.C. short-circuit protected
- Very low internal thermal resistance
- Thermal protection
- Very low intermodulation distortion
- Very low transient intermodulation distortion
- Complete SOAR protection

QUICK REFERENCE DATA

Supply voltage range	V_P	15 to 50	V
Total quiescent current at V_P = 33 V	I_{tot}	typ. 70	mA
Output power at d_{tot} = 0,5% sine-wave power			
V_P = 33 V; R_L = 4 Ω	P_o	typ. 22	W
V_P = 33 V; R_L = 4 Ω	P_o	> 20	W
V_P = 42 V; R_L = 8 Ω	P_o	typ. 20	W
Closed-loop voltage gain (externally determined)	G_c	typ. 30	dB
Input resistance (externally determined by R_{8-1})	R_i	typ. 20	kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ. 76	dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ. 60	dB

PACKAGE OUTLINE

TDA1520A : 9-lead SIL; plastic power (SOT-131A).
TDA1520AQ: 9-lead SIL-bent-to-DIL; plastic power (SOT-157A).

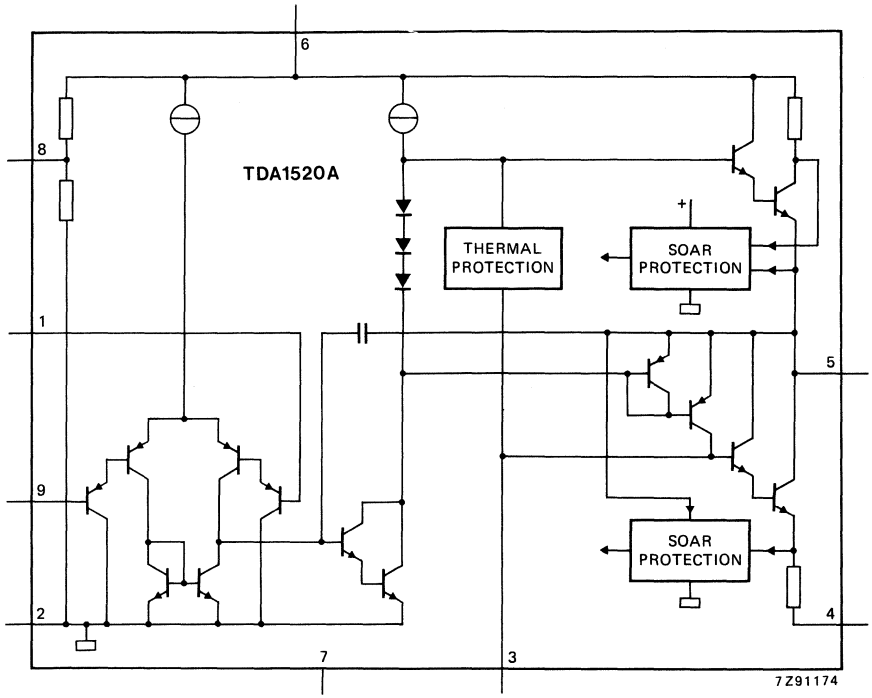


Fig. 1 Simplified internal circuit diagram.

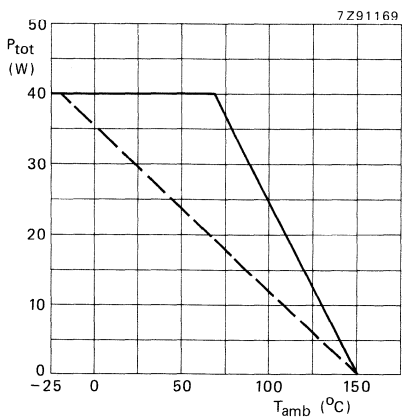
PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Negative supply (ground)
5. Output
6. Positive supply (V_P)
7. Not connected
8. Ripple rejection
9. Inverting input (feedback)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	50 V
Repetitive peak output current	I_{ORM}	max.	4 A
Non-repetitive peak output current	I_{OSM}	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Duration of a.c. short-circuit of load ($R_L = 0\ \Omega$) during full-load sine-wave drive at: $V_S = \pm 20$ V (symmetrical) and $R_{supply} = 0\ \Omega$; or $V_S = 35$ V (asymmetrical) and $R_{supply} \geqslant 4\ \Omega$	t_{sc}	max.	100 hours



——— mounted on infinite heatsink.
— — — mounted on heatsink of 2,3 K/W.

Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	⩽	2 K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 50	V
Total quiescent current at V_P = 33 V	I_{tot}	typ.	70	mA
		$\leqslant$	105	mA
Minimum guaranteed output current (peak value)	I_{ORM}	$\geqslant$	3,2	A

A.C. CHARACTERISTICS

V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power				
sine-wave power at d_{tot} = 0,5%				
R_L = 4 Ω	P_o	typ.	22	W
R_L = 4 Ω (Fig. 4)	P_o	>	20	W
R_L = 8 Ω; V_P = 42 V	P_o	typ.	20	W
Power bandwidth at d_{tot} = 0,5% from P_o = 50 mW to 10 W	B	20 Hz to	20	kHz
Voltage gain				
open-loop	G_o	typ.	74	dB
closed-loop	G_c	typ.	30	dB
Internal resistance of pin 1 (at $R_{1-8} = \infty$)	R_i	>	1	MΩ
Input resistance of test circuit at pin 1 (Fig. 3)	R_i	typ.	20	kΩ
Input sensitivity				
for P_o = 16 W	V_i	typ.	260	mV
Signal-to-noise ratio				
at P_o = 50 mW; R_{source} = 2 kΩ				
f = 20 Hz to 20 kHz; unweighted	S/N	typ.	76	dB
weighted; measured according to IEC 179 (A-curve)	S/N	typ.	80	dB
Ripple rejection at f = 100 Hz; R_S = 0 Ω	RR	typ.	60	dB
Total harmonic distortion at P_o = 16 W	d_{tot}	typ.	0,01	%
Output resistance (pin 5)	R_o	typ.	0,01	Ω
Input offset voltage	V_{5-8}	typ.	1	mV
		<	100	mV
Transient intermodulation distortion				
at P_o = 10 W	d_{TIM}	typ.	0,01	%
Intermodulation distortion at P_o = 10 W	d_{IM}	typ.	0,01	%
Slew rate	SR	typ.	9	V/μs

APPLICATION INFORMATION

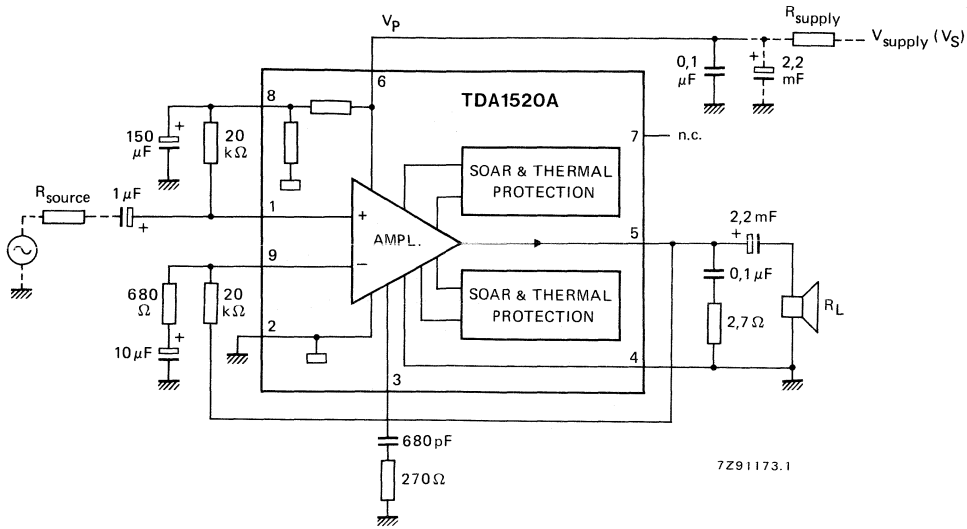


Fig. 3 Test and application circuit.

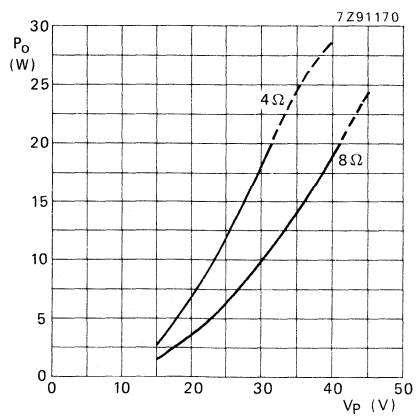


Fig. 4 Output power (P_o) versus supply voltage (V_p) at f = 1 kHz, d_{tot} = 0,5%, G_v = 30 dB.

APPLICATION INFORMATION (continued)

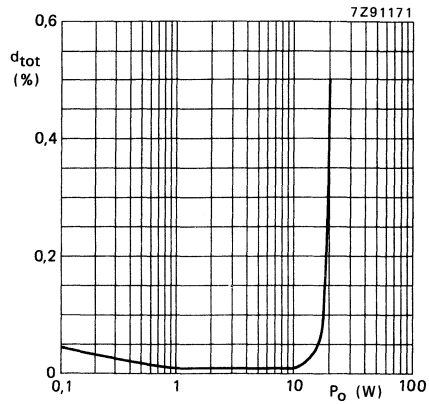


Fig. 5 Total harmonic distortion (d_{tot}) versus output power (P_o) at V_p = 33 V, R_L = 4 Ω, f = 1 kHz.

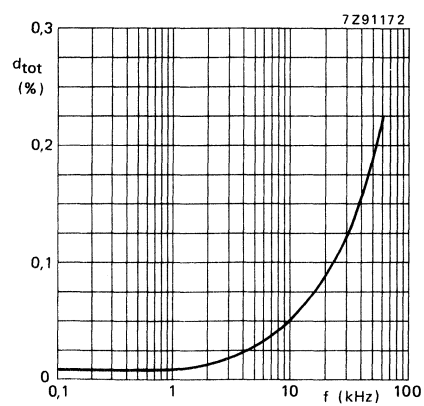


Fig. 6 Total harmonic distortion (d_{tot}) versus operating frequency (f) at V_p = 33 V, R_L = 4 Ω, P_o = 10 W (constant).

2 x 12 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521 is a dual hi-fi audio power amplifier in a 9-lead single in-line (SIL-9) plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off sounds)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	±7,5 to ±20	V
Output power at THD = 0,5%, V_P = ± 16 V	P_O	typ. 12	W
Voltage gain	G_V	typ. 30	dB
Gain balance between channels	ΔG_V	typ. 0,2	dB
Ripple rejection	RR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINE

9-lead SIL; plastic power (SOT-131B).

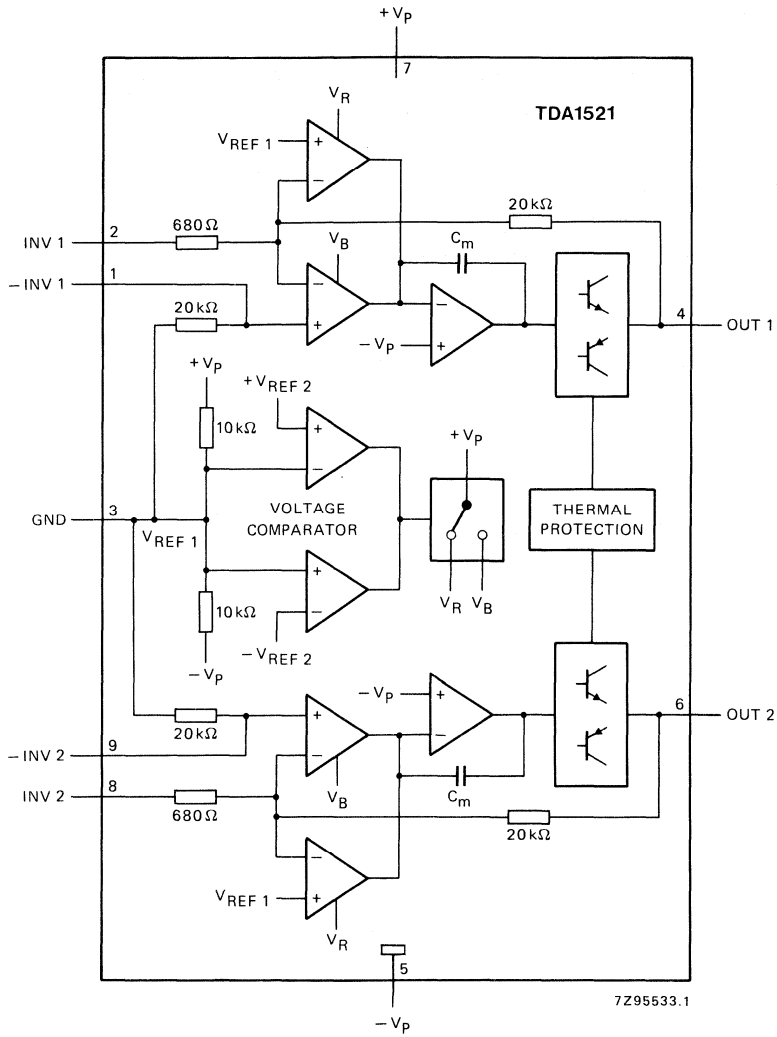


Fig. 1 Block diagram.

PINNING

1.	–INV1	non-inverting input 1	6.	OUT2	output 2
2.	INV1	inverting input 1	7.	+VP	positive supply
3.	GND	ground	8.	INV2	inverting input 2
4.	OUT1	output 1	9.	–INV2	non-inverting input 2
5.	–VP	negative supply			

FUNCTIONAL DESCRIPTION

This hi-fi stereo power amplifier is designed for mains fed applications. The circuit is optimal for symmetrical power supplies but it is also well suited to asymmterical power supply systems. An output power of 2 x 12 watts (THD = 0,5%) can be delivered into an 8 Ω load with a symmetrical power supply of ±16 V.

The gain is fixed internally at 30 dB, but can be changed externally if required. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0,2 dB).

A special feature is an input mute circuit which provides suppression of unwanted signals at the inputs during switching-on and off. This circuit disconnects the non-inverting inputs when the supply voltage is below ±6 V, whilst allowing the amplifiers to remain in their d.c. operating condition.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pins 5 and 7	$V_P = V_{5,7-3}$	–	+20	V
Non-repetitive peak output current	pins 4 and 6	I_{OSM}	–	4	A
Total power dissipation		P_{tot}	see Fig. 2		
Storage temperature range		T_{stg}	−65	+150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground	symmetrical power supply	t_{sc}	–	1	hour
	asymmetrical power supply; $V_P <$ * V (unloaded); $R_i \geqslant$ * Ω	t_{sc}	–	1	hour

DEVELOPMENT DATA

* Value under investigation.

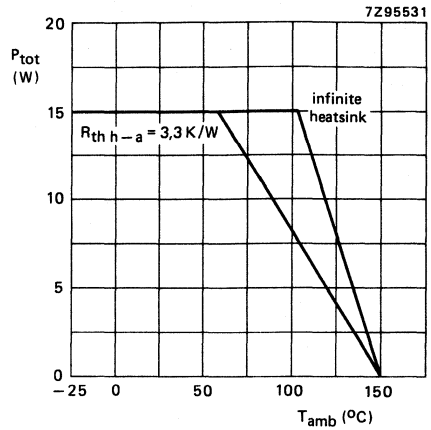


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j\text{-}c}$ = 2,5 K/W

HEATSINK DESIGN EXAMPLE

With derating of 2,5 K/W, the value of heatsink thermal resistance is calculated as follows:

given R_L = 8 Ω and V_P = ±16 V, the measured maximum dissipation is 14,6 W; then, for a maximum ambient temperature of 65 °C, the required thermal resistance of the heatsink is

$$R_{th\ h\text{-}a} = \frac{150 - 65}{14,6} - 2,5 = 3,3\ K/W$$

DEVELOPMENT DATA

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	–	±16	±20	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: symmetrical power supply; test circuit as per Fig. 3; V_P = ± 16 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Supply voltage range		V_P	±7,5	±16	±20	V
Total quiescent current	without R_L	I_{tot}	–	50	*	mA
Output power	THD = 0,5%	P_o	10	12	–	W
	THD = 10%	P_o	–	15	–	W
Total harmonic distortion	P_o = 6 W	THD	–	*	0,2	%
Power bandwidth	THD = 0,5% note 1	B		20 Hz to 20 kHz		
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	–	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection	note 2	RR	40	60	–	dB
Channel separation	R_S = 0 Ω	α	46	70	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
D.C. output offset voltage	w.r.t. GND	V_{OFF}	–	20	200	mV
Input mute mode: symmetrical power supply; test circuit as per Fig. 3; V_P = ± 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Supply voltage		V_P	±2	–	±5,8	V
Total quiescent current	without R_L	I_{tot}	–	30	*	mA
Output voltage	V_i = 600 mV	V_{out}	–	–	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Ripple rejection	note 2	RR	35	–	–	dB
D.C. output offset voltage	w.r.t. GND	V_{OFF}	–	20	200	mV

* Value under investigation.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: asymmetrical power supply; test circuit as per Fig. 4; V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	–	50	*	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	–	8,5	–	W
Total harmonic distortion	P_o = 4 W	THD	–	*	0,2	%
Power bandwidth	THD = 0,5% note 1	B	40 Hz to 20 kHz			
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	–	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection	note 2	RR	40	50	–	dB
Channel separation	R_S = 0 Ω	α	40	–	–	dB

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ −3 dB.
2. Ripple rejection at R_S = 0 Ω, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

* Value under investigation.

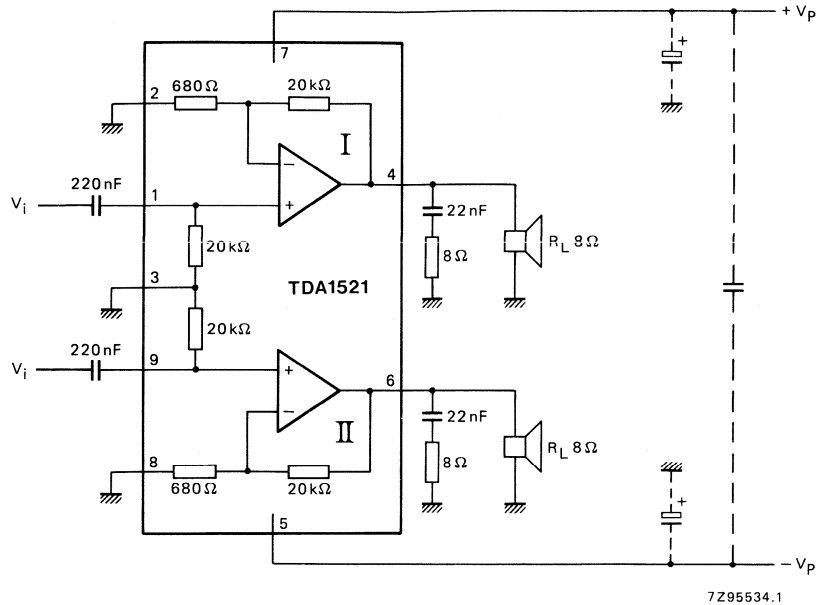


Fig. 3 Test and application circuit; symmetrical power supply.

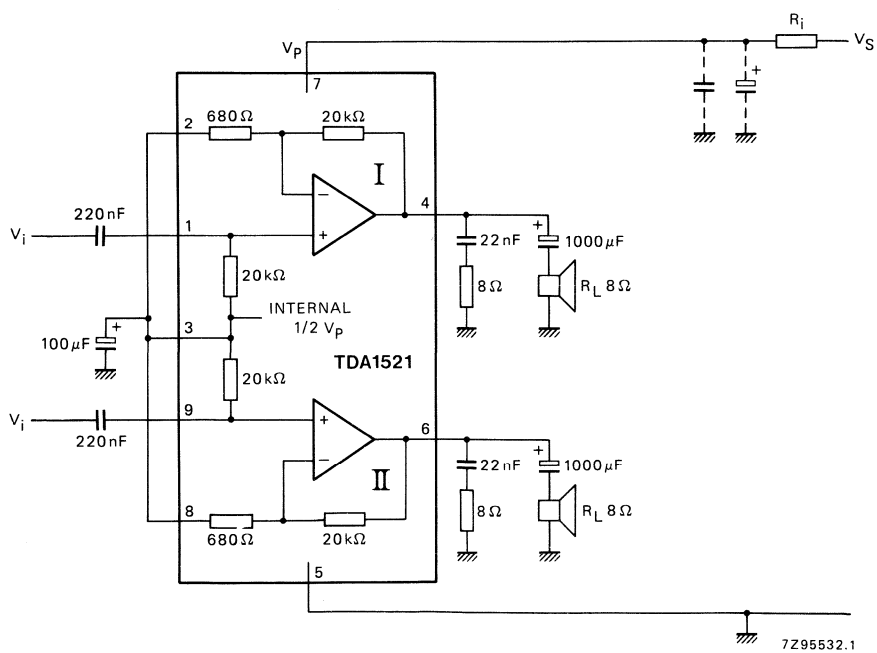


Fig. 4 Test and application circuit; asymmetrical power supply.

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